L-1215XB

T-41-39

- 480 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830
- Color tone: Yellowgreen

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 110H x 11.5T (max.) mm
Effective display area	242W x 69H mm
Number of dots	480W x 128H dot
Dot size	0.43W x 0.43H mm
Dot pitch	0.48W x 0.48H mm
Weight	about 320 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V, V_{EE} = −13.5 V ± 0.5 V

Input "high" voltage (V_{IH}) (Note 1) . 0.7 x V_{DD} ~ V_{DD} V

Input "low" voltage (V_{IL}) (Note 1) .... 0 ~ 0.3 x V_{DD} V

Clock frequency (f_{CL2}) ..... 1.08 MHz min.
1.15 MHz typ.
1.23 MHz max.

Power supply current (I_{DD}) ..... 6 mA typ.
(I_{EE}) ..... 3 mA typ.

(D_1 ~ D_4 = GND) (f_{CL2} = 1.15 MHz)

$V_{DD} - V_0$ = 14.5 V

Power supply for LCD drive (Recommended)($V_{DD} - V_0$)
Duty = 1/64

Ta = 0°C ..... 15.5 V typ.
Ta = 25°C ..... 14.5 V typ.
Ta = 40°C ..... 14.0 V typ.

OPTICAL DATA ..... See page 5

Notes 1. Applied to CL1, CL2, D1 ~ D4, M, FLM.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (upper left half)
2	D2	H/L	Serial row data (lower left half)
3	FLM	H	The FLM signal indicates the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H→L	The CL1 latches the serial data in the shift registers
6	CL2	H→L	Clock signal for shifting the serial data
7	D3	H/L	Serial row data (upper right half)
8	D4	H/L	Serial row data (lower right half)
9	V_{DD}(+5V)	–	Power supply for logic circuit
10	V_{SS} (0V)	–	Ground
11	VEE(−10V)	–	Power supply for LC driving
12	V_O	–	Operating voltage for LC driving

Unit: mm

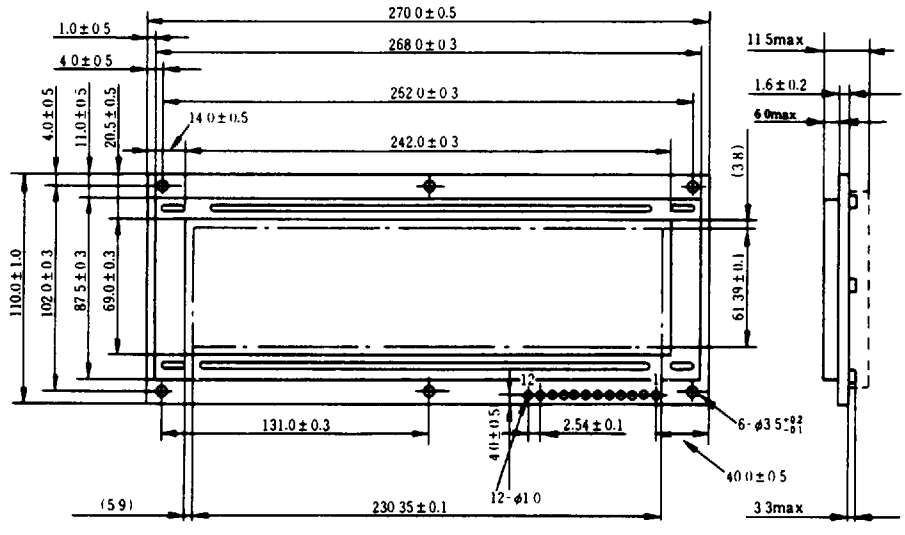


Fig. 1 Display pattern

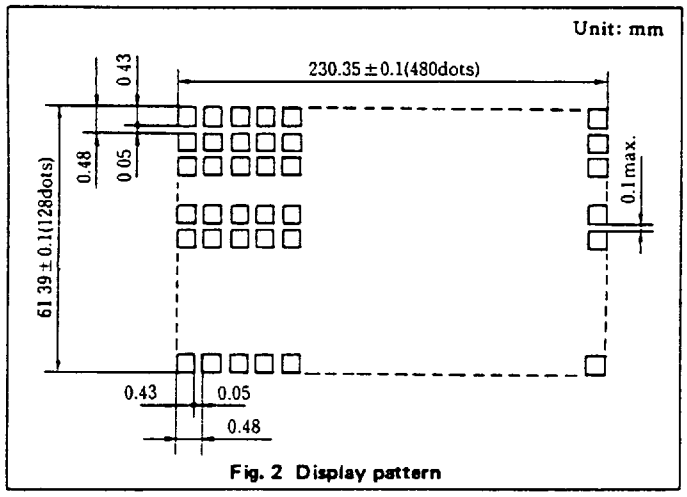


Fig. 2 Display pattern

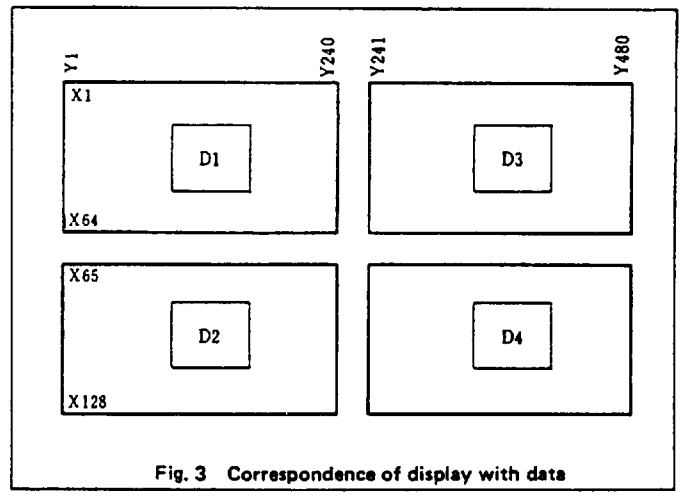
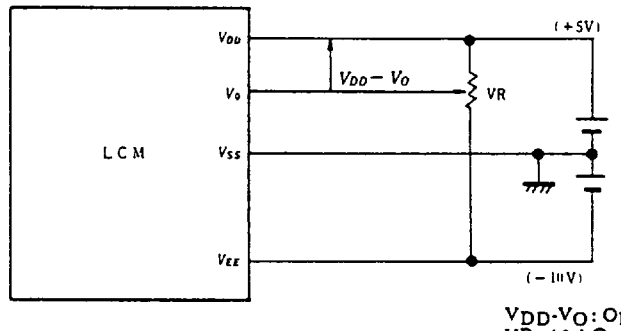
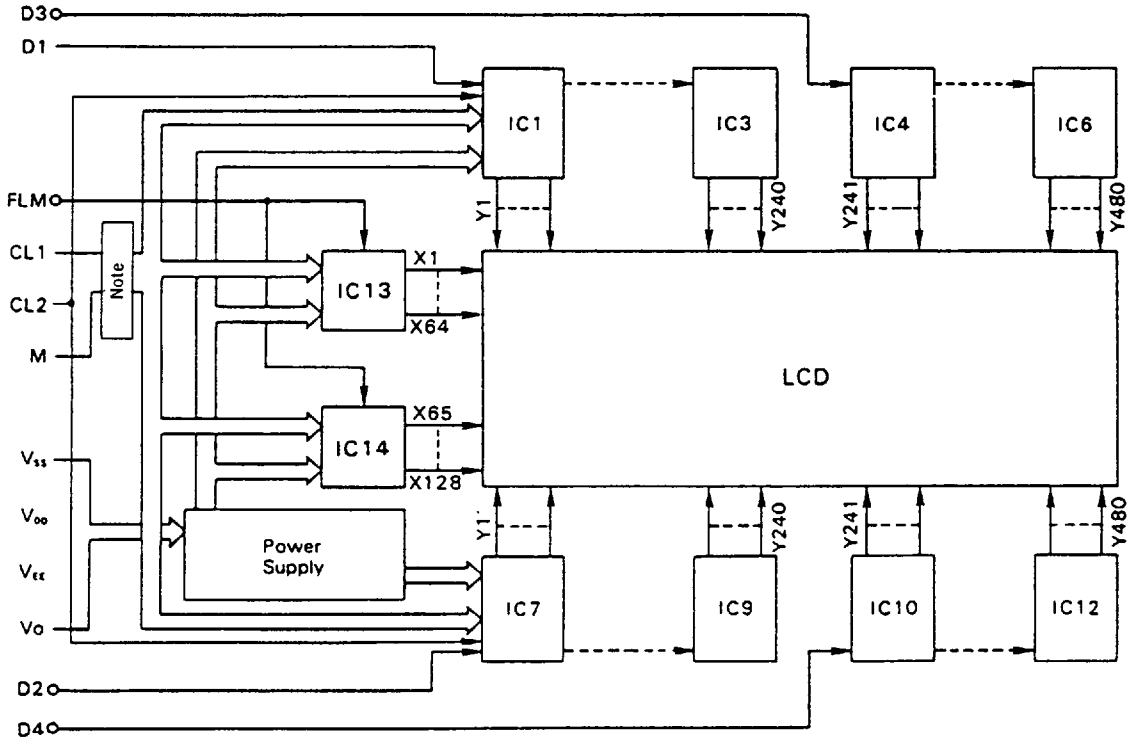


Fig. 3 Correspondence of display with data



V_{DD}-V_O: Operating voltage for LC driving
VR: 10 kΩ ~ 20 kΩ

Fig. 4 Power supply



Note: Interface timing circuit

Fig. 5 Block diagram

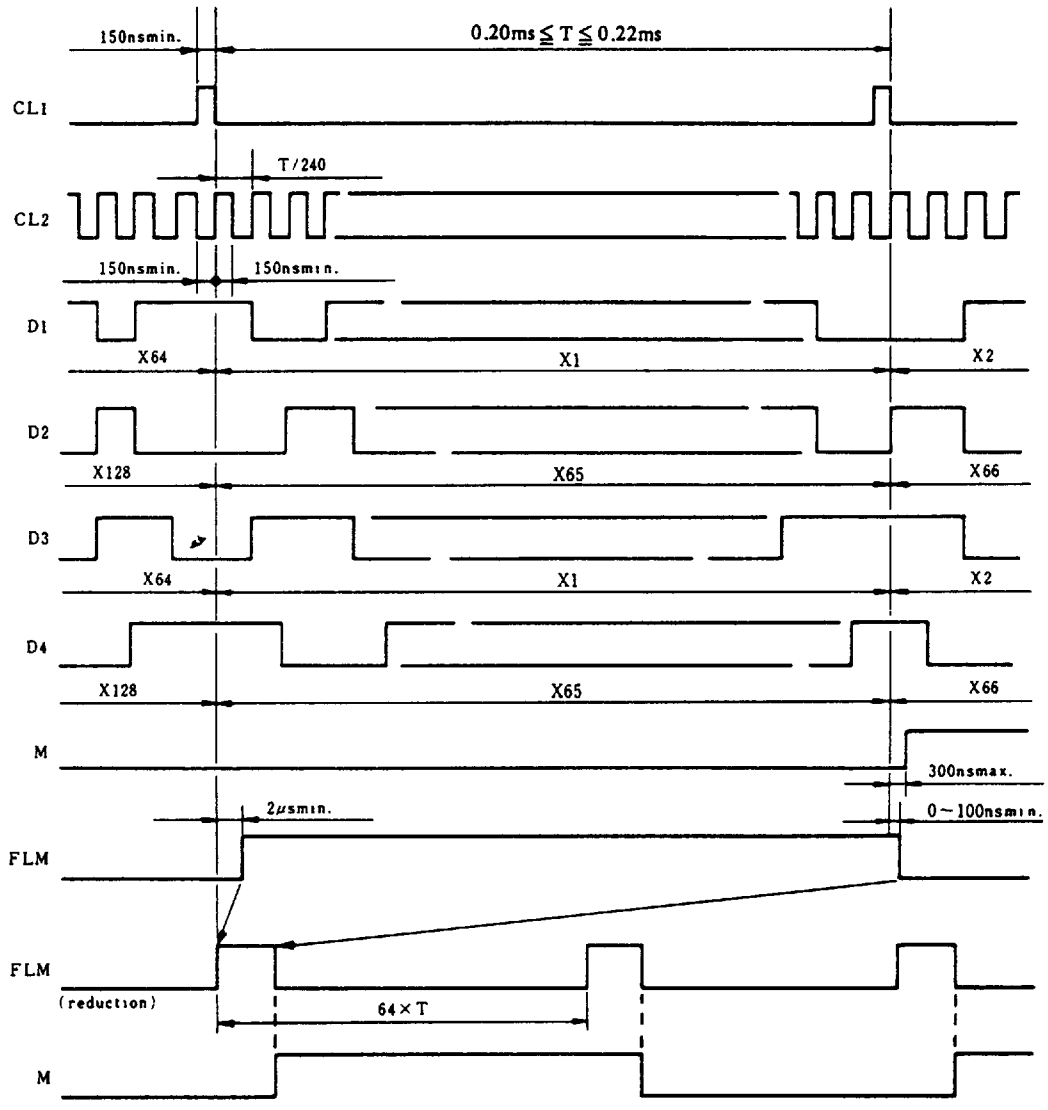


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	810	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	100	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

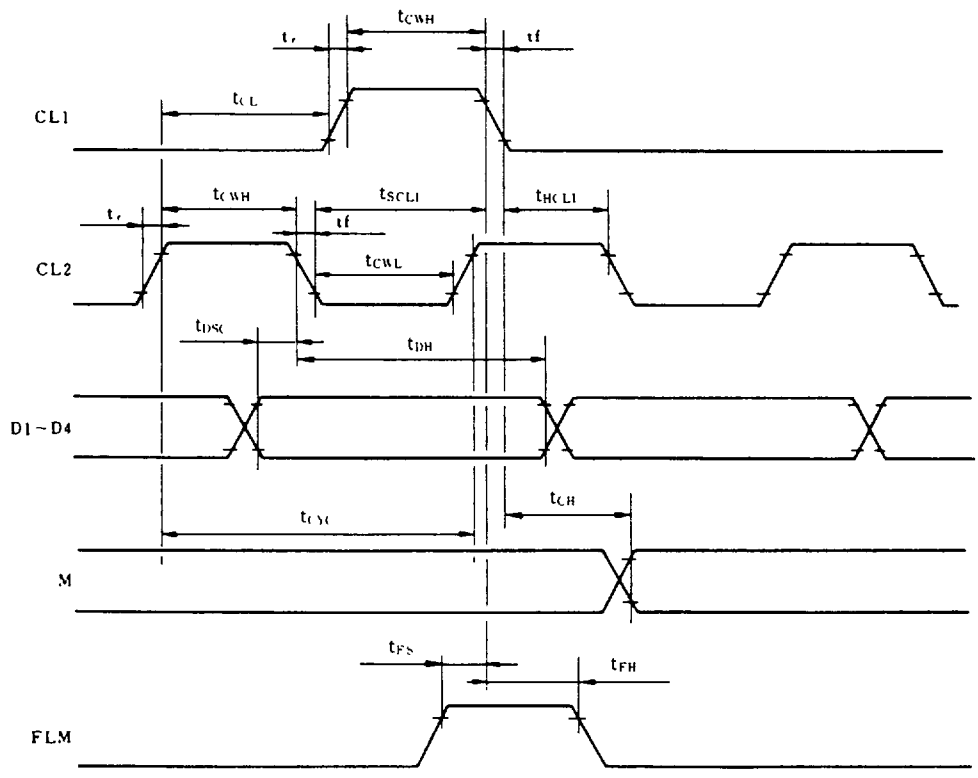


Fig. 7 Interface timing