K1602TE Series

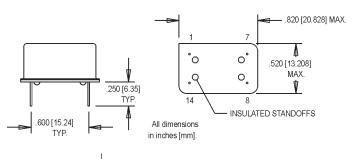
14 pin DIP, 5.0 Volt, CMOS/TTL, TCVCXO

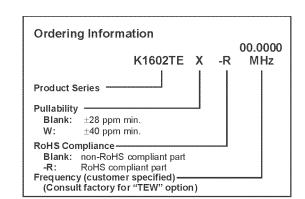






- Former Champion Product
- Phase-Locked Loops Clocking "Sync" to NTSC Video Standards, Reference Signal, Signal Tracking





M6034Sxxx - Contact factory for datasheet.

	.400 [10.16] MAX.
TT	<u> </u>
	.018 [0.46] DIA. TYP.
->	.300 [7.62] TYP.

Pin Connections

PIN	FUNCTION				
1	Control Voltage				
7	Ground/Case Gnd				
8	Output				
14	+Vdd				

	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition/Notes			
	Frequency Range	F	2.0 to 35.0, 38.88 to 40.0			MHz				
	Operating Temperature	TA	-40		+85	°C				
	Storage Temperature	Ts	-40		+85	°C				
	Frequency Stability	ÄF/F			±7.0	ppm	See Note 1			
	Aging (10 Year)		-2		+2	ppm				
	Control Voltage	Vc	0.5	2.5	4.5	V	Positive Monotonic Slope			
ns	Tuning Range		±28 ("TI	±28 ("TEW" model ±40)			See Ordering Information			
유	Modulation Bandwidth	fm	20			kHz	±3dB			
cifications	Input Impedance	Zin	50k			Ohms	@ 10 kHz			
Ç.	Input Voltage	Vdd	4.75	5.0	5.25	V				
Spe	Input Current	ldd			20	mA				
	Output Type						HCMOS/TTL			
Electrical	Load		5 TTL or 15 pF HCMOS max.			S max.	See Note 2			
당	Symmetry (Duty Cycle)						See Note 3			
 📺	< 14 M Hz		45		55	%				
	≥ 14 MHz		40		60	%				
	Logic "1" Level	Voh	4.5			V				
	Logic "0" Level	Vol			0.5	V				
	Rise/Fall Time	Tr/Tf		3.5	9.0	ns				
	Start Up Time				20	ms				
	Phase Noise (typical)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier			
	@ 20 MHz	-80	-108	-125	-132	-155	dBc/Hz			
<u>=</u>	Mechanical Shock		Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave)							
Environmental	Vibration		Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)							
۱ĕ	Hermeticity	Per MIL-ST	Per MIL-STD-202, Method 112, (1x10-8 atm. cc/s of Helium)							
Į.	Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles)								
N	Solderability	Per EIAJ-STD-002								
	Max Wave Soldering Conditions	See solder profile, Figure 2								

- 1. Inclusive of calibration, temperature, voltage, load and aging.
- 2. TTL Load see load circuit diagram #1. HCMOS load see load circuit diagram #2.
- 3. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.

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