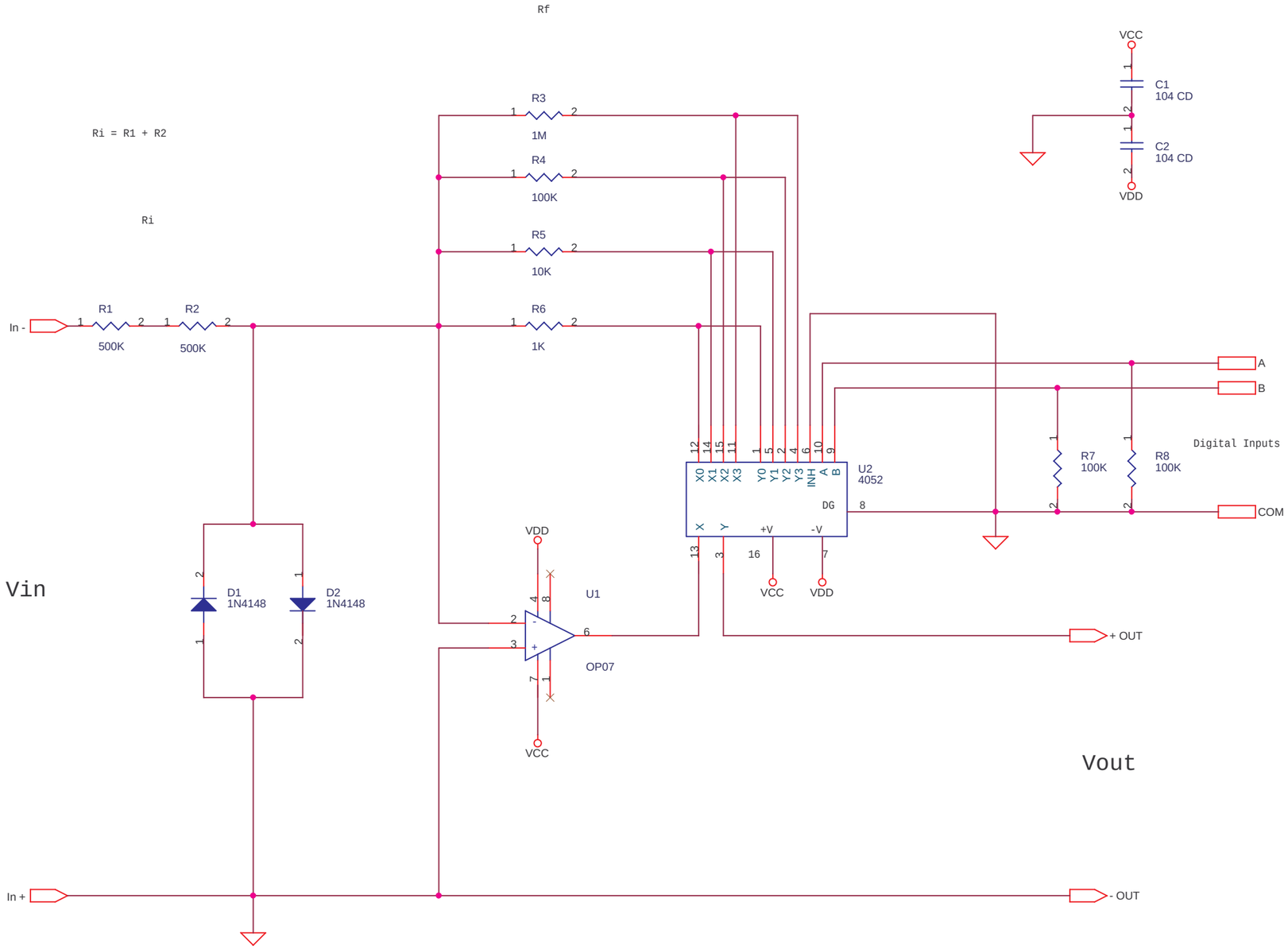

Vout = -(Rf/Ri) * Vin

Gain = Av = Rf/Ri

Design Background

a. Input 500 V max

1/4 W Rresistor can withstand 250V
hence R1 and R2 in Series for 1M/500V
R1 and R2 Limit the current also.

D1 and D2 Clamps the voltage to +/-0.5V
therby protecting OpAmp.

b. Output

Output connect to DPM 7107/7135 or any
other A/D Convertor or OpAmp Stage

Use a buffer at output if output has
to be loaded by a value less than 1Meg.

Use an inverting buffer if input leads
have to have polarity where gnd is -In.
See DACT0009.SCH for details.

c. 4052 CMOS Switch

The 4052/51/53 Analog Multiplexers
have an on Resistance of around 100E
the highlight of the circuit is that
the CMOS on resistance comes in series
with the opamp output source resistance.
which produces no error at output.

Caution !!!

Circuit does not isolate only attenuates.
When high voltage is present at input
any part of circuit is a danger to touch.

Digital Control Options

A and B can be controlled by I/O port of uC
like 80C31 so that the uC can Control gain.

A and B can be given to Counters like
4029/4518 to scroll gain digitally.

A and B can be connected to DIP switch.

A and B can be connected to a thumbwheel
switch.

Digital Inputs Logic 0 is 0V Logic 1 is 5V

X Y Value	(2) B	(1) A	Gain Av Attenuation
0	0	0	1/1000
1	0	1	1/100
2	1	0	1/10
3	1	1	1

VCC = +5V (7805) VDD = -5V (7905)

ALL RESISTORS MFR 1% UNLESS SPECIFIED

CD is Ceramic Disc 104 = 0.1uF = 100n

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Title
PRECISION ATTENUATOR WITH DIGITAL CONTROL

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B	DACT0008.SCH	00

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