TDA9983B

HDMI transmitter up to 150 MHz pixel rate with 3 × 8-bit video inputs and 4 × I²S-bus with S/PDIF

Rev. 01 — 20 May 2008 Product data sheet

1. General description

The TDA9983B is an HDMI transmitter (which also supports DVI) that enables a 3 × 8-bit RGB or YC_BC_R video stream (with a pixel rate up to 150 MHz for the TDA9983BHW/15 version), up to 4 I²S-bus audio streams (with an audio sampling rate up to 192 kHz) and the additional information required by all the HDMI 1.2a standards.

A programmable upscaling block enables a 720p/1080i output from a standard definition input. An intrafield deinterlacer is included in the scaler.

In order to be compatible with most applications, the TDA9983B integrates a full programmable input formatter and color space conversion block. The video input formats accepted are YC_BC_R 4 : 4 : 4 (up to 3 × 8-bit), YC_BC_R 4 : 2 : 2 semi-planar (up to 2 × 12-bit), YC_BC_R 4 : 2 : 2 compliant with ITU656 and ITU656-like (up to 1 × 12-bit).

For ITU656-like formats, double edges are supported so that data can be sampled on rising and falling edges.

The device can be controlled via an I²C-bus interface.

2. Features

- 3 × 8-bit video data input bus, CMOS and LV-TTL compatible
- Horizontal synchronization, vertical synchronization and Data Enable (DE) inputs or VREF, HREF and FREF could be used for input data synchronization
- Pixel rate clock input can be made active on one or both edges (selectable by I²C-bus)
- The TDA9983B has 4 I²S-bus audio input channels and 1 S/PDIF channel; audio sampling rate up to 192 kHz
- 250 MHz to 1.50 GHz HDMI transmitter operation
- Programmable input formatter and upsampler/interpolator allows input of any of the 4 : 4 : 4, 4 : 2 : 2 semi-planar, 4 : 2 : 2 ITU656 and ITU656-like formats
- Programmable color space converter:
  - RGB to YC_BC_R
  - YC_BC_R to RGB
- The upscaler enables a 720p/1080i output from a standard definition input using intelligent edge interpolation
- Controllable via I²C-bus
- Low power dissipation
- 1.8 V and 3.3 V power supplies
- Power-down mode

- Hard reset

3. Applications

- DVD players and recorders
- Set-Top Box (STB)
- AV receivers and amplifiers (repeater)
- Camcorders
- Digital still cameras
- Media players
- PVRs
- Media centers PCs, graphics add-in boards, notebook PCs
- Switches

4. Quick reference data

Table 1. Quick reference data

$V_{DDA(FRO\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(PLL\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(3V3)}$ = 3.0 V to 3.6 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; V_{PP} = 0 V; T_{amb} = 0 °C to 70 °C. Typical values are measured at $V_{DDA(FRO\_3V3)}$ = $V_{DDA(PLL\_3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V; $V_{DDC(1V8)}$ = 1.8 V; V_{PP} = 0 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TDA9983BHW/8 and TDA9983BHW/15							
$V_{DDA(FRO\_3V3)}$	free running oscillator 3.3 V analog supply voltage			3.0	3.3	3.6	V
$V_{DDA(PLL\_3V3)}$	PLL 3.3 V analog supply voltage			3.0	3.3	3.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)		[1]	3.0	3.3	3.6	V
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		[1]	1.65	1.8	1.95	V
T_{amb}	ambient temperature			0	-	70	°C
TDA9983BHW/8; up to 81 MHz							
$f_{clk(max)}$	maximum clock frequency		[2]	81	-	-	MHz
P_{cons}	power consumption		[2]	-	322	-	mW
		worst case	[3]	-	338	503	mW
P_{tot}	total power dissipation		[2]	-	458	-	mW
		worst case	[3]	-	472	651	mW
P_{pd}	power dissipation in power-down mode			-	13.5	38.4	mW

Table 1. Quick reference data *...continued*

$V_{DDA(FRO\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(PLL\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(3V3)}$ = 3.0 V to 3.6 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; V_{PP} = 0 V; T_{amb} = 0 °C to 70 °C. Typical values are measured at $V_{DDA(FRO\_3V3)}$ = $V_{DDA(PLL\_3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V; $V_{DDC(1V8)}$ = 1.8 V; V_{PP} = 0 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TDA9983BHW/15; up to 150 MHz							
$f_{clk(max)}$	maximum clock frequency		[4]	150	-	-	MHz
P_{cons}	power consumption		[4]	-	361	583	mW
P_{tot}	total power dissipation		[4]	-	495	732	mW
P_{pd}	power dissipation in power-down mode			-	13.5	38.4	mW

[1] The $V_{DDD(3V3)}$ and $V_{DDC(1V8)}$ power supplies must always follow the sequence shown in Figure 14 to ensure proper power-up conditions.

[2] Video format:
- a) Input 480p (ITU656 embedded sync, rising edge)
- b) Output 1080i (YC_BC_R 4 : 2 : 2)

[3] Worst case video format:
- a) Input 480p (YC_BC_R 4 : 2 : 2 semi-planar)
- b) Output 720p (YC_BC_R 4 : 2 : 2)

[4] Video format:
- a) Input 1080p (RGB 4 : 4 : 4 external sync, rising edge)
- b) Output 1080p (RGB 4 : 4 : 4)

5. Ordering information

Table 2. Ordering information

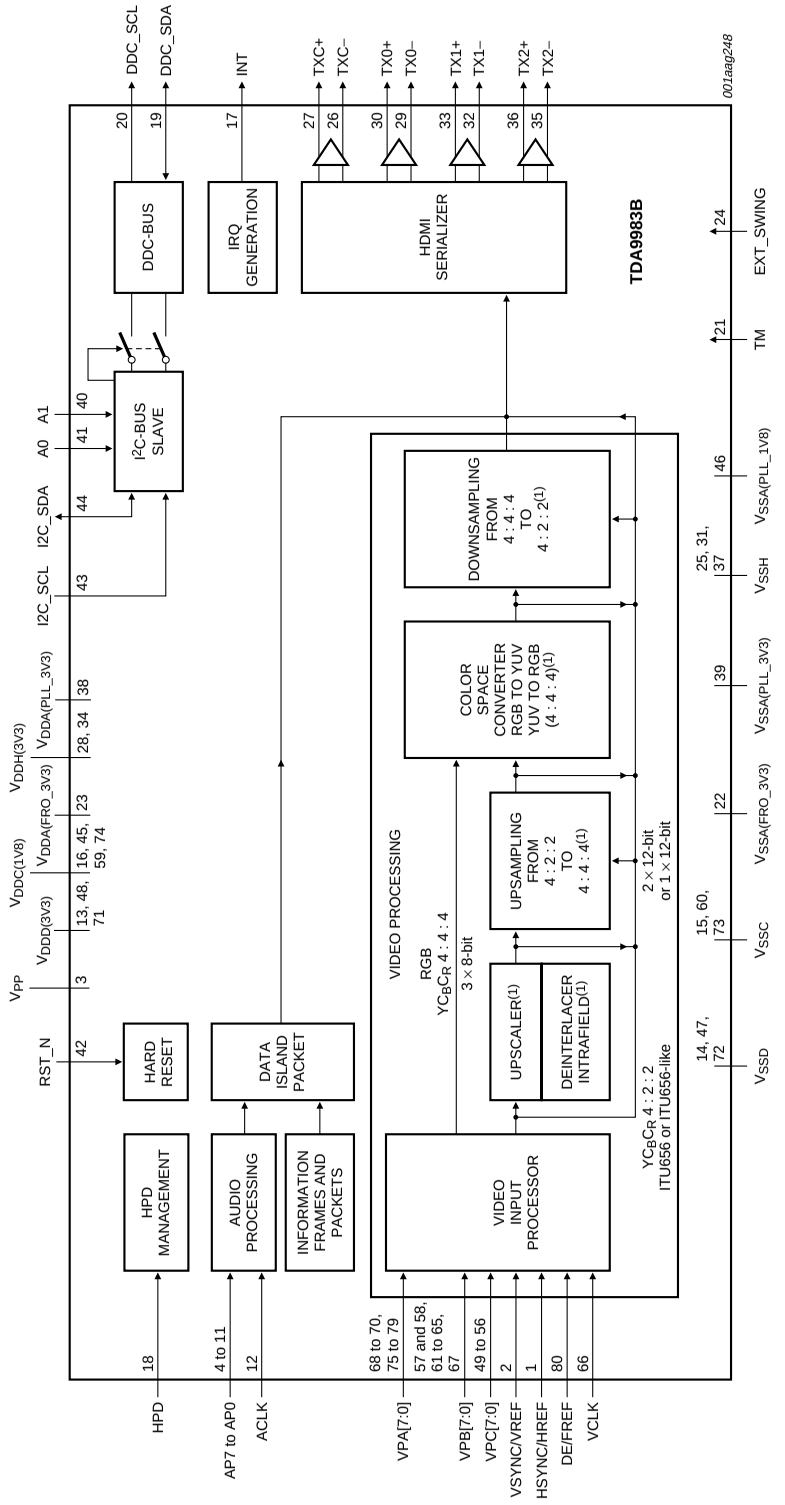
Type number	Package		
	Name	Description	Version
TDA9983BHW	HTQFP80	plastic thermal enhanced thin quad flat package; 80 leads; body 12 × 12 × 1 mm; exposed die pad	SOT841-4

5.1 Ordering options

Table 3. Survey of type numbers

Extended type number	Sampling frequency (Msample/s)	Application
TDA9983BHW/8/C1	81	customer specific version
TDA9983BHW/15/C1	150	customer specific version

6. Block diagram



(1) Block can be bypassed.

Fig 1. Block diagram

7. Pinning information

7.1 Pinning

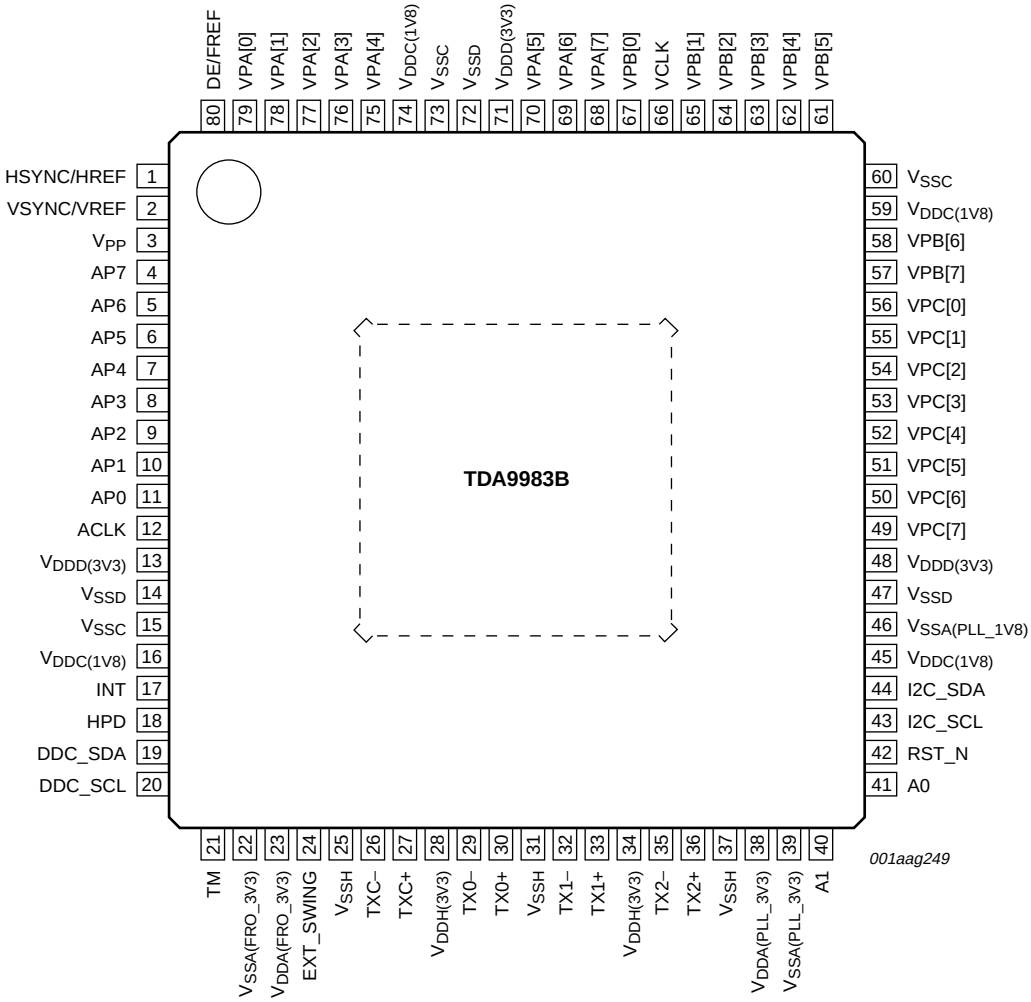


Fig 2. Pin configuration

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1]	Description
HSYNC/HREF	1	I	horizontal synchronization or reference input
VSYNC/VREF	2	I	vertical synchronization or reference input
V_{PP}	3	P	programming voltage (must be connected to the ground of the digital core in normal operation)
AP7	4	I	audio port 7 input; auxiliary (AUX)
AP6	5	I	audio port 6 input; S/PDIF stream
AP5	6	I	audio port 5 input; optional master clock MCLK for S/PDIF

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
AP4	7	I	audio port 4 input; I^2S-bus 3
AP3	8	I	audio port 3 input; I^2S-bus 2
AP2	9	I	audio port 2 input; I^2S-bus 1
AP1	10	I	audio port 1 input; I^2S-bus 0
AP0	11	I	audio port 0 input; word select WS for I^2S-bus
ACLK	12	I	audio clock input; clock SCK for I^2S-bus
$V_{DDD(3V3)}$	13	P	supply voltage for input ports (3.3 V)
V_{SSD}	14	G	ground for input ports
V_{SSC}	15	G	ground for digital core
$V_{DDC(1V8)}$	16	P	supply voltage for digital core (1.8 V)
INT	17	O	interrupt output (open drain); warns the external microprocessor that a special event has occurred; must be connected to a pull-up resistor; 5 V tolerant
HPD	18	I	hot plug detect input; 5 V tolerant
DDC_SDA	19	I/O	DDC-bus data input/output (open drain); must be connected to a pull-up resistor; 5 V tolerant
DDC_SCL	20	O	DDC-bus clock output (open drain); must be connected to a pull-up resistor; 5 V tolerant
TM	21	I	internal test mode input (must be connected to the ground of the digital core in normal operation)
$V_{SSA(FRO\_3V3)}$	22	G	analog ground for free running oscillator
$V_{DDA(FRO\_3V3)}$	23	P	analog supply voltage for free running oscillator (3.3 V)
EXT_SWING	24	I	external swing adjust input; a fixed resistor must be connected between this pin and $V_{DDH(3V3)}$ to set the HDMI output swing (see Section 8.14.1)
V_{SSH}	25	G	ground for HDMI transmitter
TXC–	26	O	negative clock channel for HDMI output
TXC+	27	O	positive clock channel for HDMI output
$V_{DDH(3V3)}$	28	P	supply voltage for HDMI transmitter (3.3 V)
TX0–	29	O	negative data channel 0 for HDMI output
TX0+	30	O	positive data channel 0 for HDMI output
V_{SSH}	31	G	ground for HDMI transmitter
TX1–	32	O	negative data channel 1 for HDMI output
TX1+	33	O	positive data channel 1 for HDMI output
$V_{DDH(3V3)}$	34	P	supply voltage for HDMI transmitter (3.3 V)
TX2–	35	O	negative data channel 2 for HDMI output
TX2+	36	O	positive data channel 2 for HDMI output
V_{SSH}	37	G	ground for HDMI transmitter
$V_{DDA(PLL\_3V3)}$	38	P	analog supply voltage for PLL (3.3 V)
$V_{SSA(PLL\_3V3)}$	39	G	analog ground reference for PLL
A1	40	I	I^2C-bus slave address input 1; bit 1
A0	41	I	I^2C-bus slave address input 0; bit 0
RST_N	42	I	hard reset input; active LOW

Table 4. Pin description *…continued*

Symbol	Pin	Type[1]	Description
I2C_SCL	43	I	I^2C-bus clock input of device (open drain); must be connected to a pull-up resistor; 5 V tolerant
I2C_SDA	44	I/O	I^2C-bus data input/output of device; open drain; must be connected to a pull-up resistor; 5 V tolerant
$V_{DDC(1V8)}$	45	P	supply voltage for digital core (1.8 V)
$V_{SSA(PLL\_1V8)}$	46	G	analog ground reference for PLL
V_{SSD}	47	G	ground for input ports
$V_{DDD(3V3)}$	48	P	supply voltage for input ports (3.3 V)
VPC[7]	49	I	video port C input bit 7
VPC[6]	50	I	video port C input bit 6
VPC[5]	51	I	video port C input bit 5
VPC[4]	52	I	video port C input bit 4
VPC[3]	53	I	video port C input bit 3
VPC[2]	54	I	video port C input bit 2
VPC[1]	55	I	video port C input bit 1
VPC[0]	56	I	video port C input bit 0
VPB[7]	57	I	video port B input bit 7
VPB[6]	58	I	video port B input bit 6
$V_{DDC(1V8)}$	59	P	supply voltage for digital core (1.8 V)
V_{SSC}	60	G	ground for digital core
VPB[5]	61	I	video port B input bit 5
VPB[4]	62	I	video port B input bit 4
VPB[3]	63	I	video port B input bit 3
VPB[2]	64	I	video port B input bit 2
VPB[1]	65	I	video port B input bit 1
VCLK	66	I	video pixel clock input
VPB[0]	67	I	video port B input bit 0
VPA[7]	68	I	video port A input bit 7
VPA[6]	69	I	video port A input bit 6
VPA[5]	70	I	video port A input bit 5
$V_{DDD(3V3)}$	71	P	supply voltage for input ports (3.3 V)
V_{SSD}	72	G	ground for input ports
V_{SSC}	73	G	ground for digital core
$V_{DDC(1V8)}$	74	P	supply voltage for digital core (1.8 V)
VPA[4]	75	I	video port A input bit 4
VPA[3]	76	I	video port A input bit 3
VPA[2]	77	I	video port A input bit 2
VPA[1]	78	I	video port A input bit 1
VPA[0]	79	I	video port A input bit 0
DE/FREF	80	I	video data enable input or field reference input
Exposed die pad	central	G	exposed die pad; must be connected to the ground of the HDMI transmitter (V_{SSH})

[1] P = power supply; G = ground; I = input; O = output.

8. Functional description

The TDA9983B is designed to convert digital data (video and audio) into an HDMI or a DVI stream. This HDMI stream can handle RGB, YC_BC_R 4 : 4 : 4 and YC_BC_R 4 : 2 : 2. The TDA9983B can accept at its inputs any of the following video modes:

- RGB
- YC_BC_R 4 : 4 : 4
- YC_BC_R 4 : 2 : 2 semi-planar
- YC_BC_R 4 : 2 : 2 ITU656 and ITU656-like

It can also handle audio. The TDA9983B can accept at its inputs any of the following audio buses:

- I^2S-bus (4 lines): up to 8 audio channels
- S/PDIF (1 channel): L-PCM (IEC 60958) or compressed audio (IEC 61937)

8.1 System clock

The clock management is based on a set of 3 PLLs that generate the different clocks required inside the chip. This includes:

- PLL double edge can generate a clock at twice the VCLK input frequency to capture the data at the video input formatter
- PLL scaling can create a new video processing scaled clock taking into account the scaling ratio programmed in the scaler
- PLL serializer is a system clock generator, which enables the stream produced by the encoder to be transmitted on the HDMI data channel at ten times the sampling rate or more; see Section 8.14.2

8.2 Video input processor

The TDA9983B has three video input ports VPA[7:0], VPB[7:0] and VPC[7:0]. The TDA9983B can reallocate and swap each of the 3 ports input channels by inverting the bus and swapping each port.

The TDA9983B can be set to latch data at either the rising or falling edge or both.

The video input formats accept (see Table 5):

- RGB
- YC_BC_R 4 : 4 : 4 (up to 3 × 8-bit)
- YC_BC_R 4 : 2 : 2 semi-planar (up to 2 × 12-bit)
- YC_BC_R 4 : 2 : 2 compliant with ITU656 and ITU656-like (up to 1 × 12-bit)

Table 5. Inputs of video input formatter

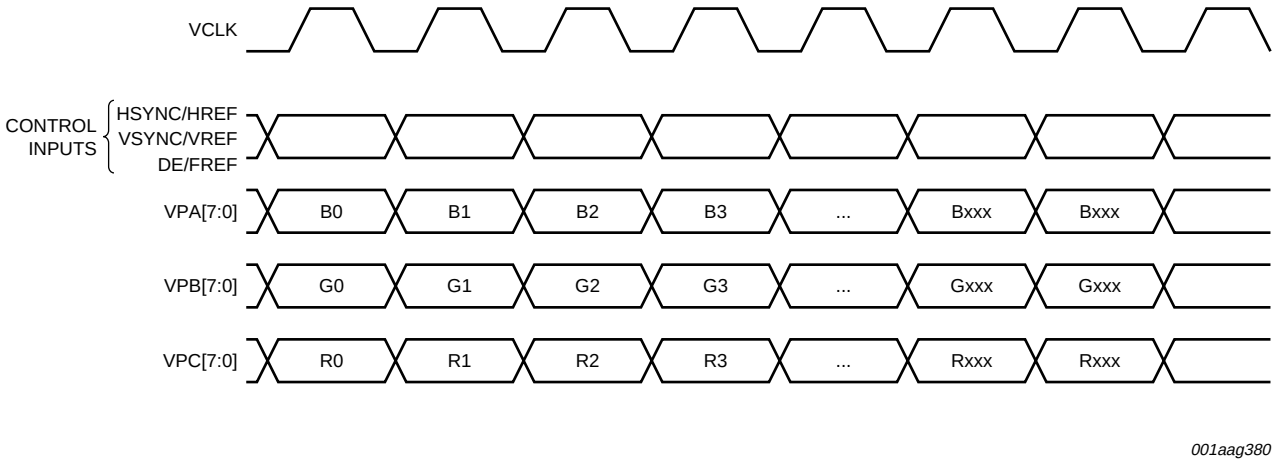
Color space	Format	Channels	Sync	Rising edge	Falling edge	Double edge[1]	Transmission input format	Max. pixel clock on pin VCLK (MHz)	Max. input format	Reference
RGB	4 : 4 : 4	3 × 8-bit	external	X				150		Table 6
			external		X			150		
			embedded	X				150		
			embedded		X			150		
YC_BC_R	4 : 4 : 4	3 × 8-bit	external	X				150		Table 7
			external		X			150		
			embedded	X				150		
			embedded		X			150		
YC_BC_R	4 : 2 : 2	up to 1 × 12-bit ITU656-like	external	X			ITU656-like	54.054	480p/576p	Table 8
			external		X		ITU656-like	54.054	480p/576p	
			external			X	ITU656-like	27.027	480p/576p	Table 9
			embedded	X			ITU656-like	54.054	480p/576p	Table 10
			embedded		X		ITU656-like	54.054	480p/576p	
			embedded			X	ITU656-like	27.027	480p/576p	Table 11
		up to 2 × 12-bit semi-planar	external	X				148.5	1080p	Table 12
			external		X			148.5	1080p	
			embedded	X			SMPTE293M	148.5	1080p	Table 13
			embedded		X		SMPTE293M	148.5	1080p	

[1] Double edge means both rising and falling edges.

Table 6. RGB 4 : 4 : 4 mappings

RGB 4 : 4 : 4 (3× 8-bit) external synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**
VPA[0]	B[0]	VPB[0]	G[0]	VPC[0]	R[0]	HSYNC/HREF	used
VPA[1]	B[1]	VPB[1]	G[1]	VPC[1]	R[1]	VSYNC/VREF	used
VPA[2]	B[2]	VPB[2]	G[2]	VPC[2]	R[2]	DE/FREF	used
VPA[3]	B[3]	VPB[3]	G[3]	VPC[3]	R[3]		
VPA[4]	B[4]	VPB[4]	G[4]	VPC[4]	R[4]		
VPA[5]	B[5]	VPB[5]	G[5]	VPC[5]	R[5]		
VPA[6]	B[6]	VPB[6]	G[6]	VPC[6]	R[6]		
VPA[7]	B[7]	VPB[7]	G[7]	VPC[7]	R[7]		



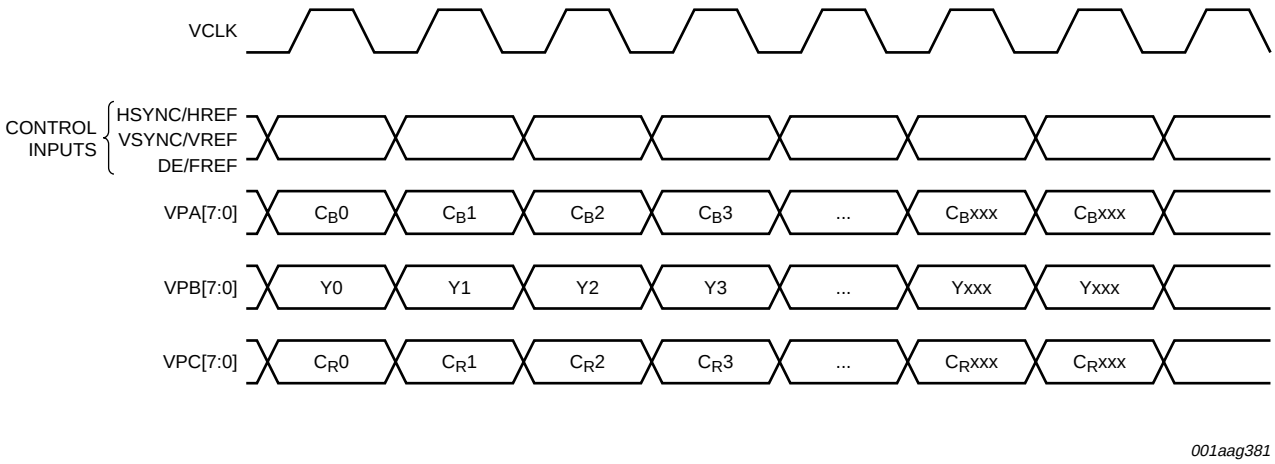
DE could also be generated from HSYNC/HREF and VSYNC/VREF

Fig 3. Pixel encoding in RGB 4 : 4 : 4 (rising edge) input

Table 7. YC_BC_R 4 : 4 : 4 mappings

YC_BC_R 4 : 4 : 4 (3× 8-bit) external synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**YC_BC_R 4 : 4 : 4**	**Pin**	**YC_BC_R 4 : 4 : 4**	**Pin**	**YC_BC_R 4 : 4 : 4**	**Pin**	**YC_BC_R 4 : 4 : 4**
VPA[0]	C_B[0]	VPB[0]	Y[0]	VPC[0]	C_R[0]	HSYNC/HREF	used
VPA[1]	C_B[1]	VPB[1]	Y[1]	VPC[1]	C_R[1]	VSYNC/VREF	used
VPA[2]	C_B[2]	VPB[2]	Y[2]	VPC[2]	C_R[2]	DE/FREF	used
VPA[3]	C_B[3]	VPB[3]	Y[3]	VPC[3]	C_R[3]		
VPA[4]	C_B[4]	VPB[4]	Y[4]	VPC[4]	C_R[4]		
VPA[5]	C_B[5]	VPB[5]	Y[5]	VPC[5]	C_R[5]		
VPA[6]	C_B[6]	VPB[6]	Y[6]	VPC[6]	C_R[6]		
VPA[7]	C_B[7]	VPB[7]	Y[7]	VPC[7]	C_R[7]		



DE could also be generated from HSYNC/HREF and VSYNC/VREF

Fig 4. Pixel encoding in YC_BC_R 4 : 4 : 4 (rising edge) input

Table 8. YC_BC_R 4 : 2 : 2 ITU656-like external synchronization single edge mappings

YC_BC_R 4 : 2 : 2 ITU656-like external synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2
VPA[0]	$C_B[0]$	$Y_0[0]$	$C_R[0]$	$Y_1[0]$	VPB[0]	$C_B[4]$	$Y_0[4]$	$C_R[4]$	$Y_1[4]$	HSYNC/HREF	used
VPA[1]	$C_B[1]$	$Y_0[1]$	$C_R[1]$	$Y_1[1]$	VPB[1]	$C_B[5]$	$Y_0[5]$	$C_R[5]$	$Y_1[5]$	VSYNC/VREF	used
VPA[2]	$C_B[2]$	$Y_0[2]$	$C_R[2]$	$Y_1[2]$	VPB[2]	$C_B[6]$	$Y_0[6]$	$C_R[6]$	$Y_1[6]$	DE/FREF	used
VPA[3]	$C_B[3]$	$Y_0[3]$	$C_R[3]$	$Y_1[3]$	VPB[3]	$C_B[7]$	$Y_0[7]$	$C_R[7]$	$Y_1[7]$		
VPA[4]	-	-	-	-	VPB[4]	$C_B[8]$	$Y_0[8]$	$C_R[8]$	$Y_1[8]$		
VPA[5]	-	-	-	-	VPB[5]	$C_B[9]$	$Y_0[9]$	$C_R[9]$	$Y_1[9]$		
VPA[6]	-	-	-	-	VPB[6]	$C_B[10]$	$Y_0[10]$	$C_R[10]$	$Y_1[10]$		
VPA[7]	-	-	-	-	VPB[7]	$C_B[11]$	$Y_0[11]$	$C_R[11]$	$Y_1[11]$		

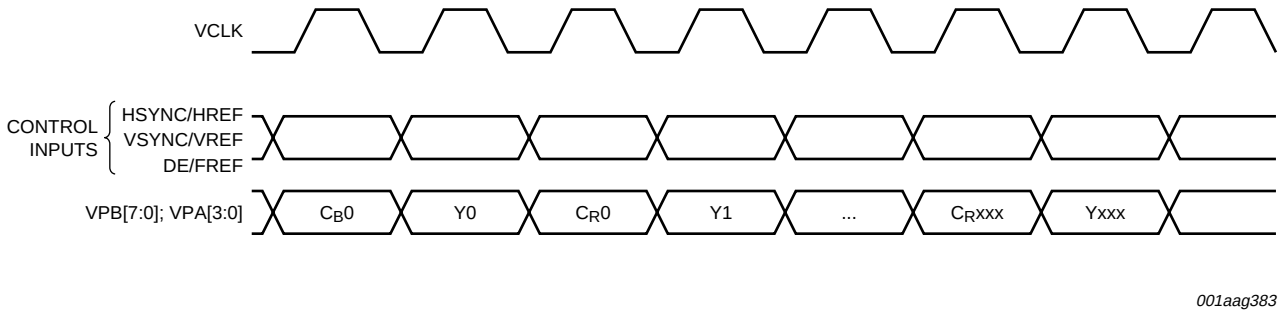


Fig 5. Pixel encoding YC_BC_R 4 : 2 : 2 ITU656-like external synchronization single edge (rising edge) input

Table 9. YC_BC_R 4 : 2 : 2 ITU656-like external synchronization double edge mappings

YC_BC_R 4 : 2 : 2 ITU656-like external synchronization double edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2
VPA[0]	$C_B[0]$	$Y_0[0]$	$C_R[0]$	$Y_1[0]$	VPB[0]	$C_B[4]$	$Y_0[4]$	$C_R[4]$	$Y_1[4]$	HSYNC/HREF	used
VPA[1]	$C_B[1]$	$Y_0[1]$	$C_R[1]$	$Y_1[1]$	VPB[1]	$C_B[5]$	$Y_0[5]$	$C_R[5]$	$Y_1[5]$	VSYNC/VREF	used
VPA[2]	$C_B[2]$	$Y_0[2]$	$C_R[2]$	$Y_1[2]$	VPB[2]	$C_B[6]$	$Y_0[6]$	$C_R[6]$	$Y_1[6]$	DE/FREF	used
VPA[3]	$C_B[3]$	$Y_0[3]$	$C_R[3]$	$Y_1[3]$	VPB[3]	$C_B[7]$	$Y_0[7]$	$C_R[7]$	$Y_1[7]$		
VPA[4]	-	-	-	-	VPB[4]	$C_B[8]$	$Y_0[8]$	$C_R[8]$	$Y_1[8]$		
VPA[5]	-	-	-	-	VPB[5]	$C_B[9]$	$Y_0[9]$	$C_R[9]$	$Y_1[9]$		
VPA[6]	-	-	-	-	VPB[6]	$C_B[10]$	$Y_0[10]$	$C_R[10]$	$Y_1[10]$		
VPA[7]	-	-	-	-	VPB[7]	$C_B[11]$	$Y_0[11]$	$C_R[11]$	$Y_1[11]$		

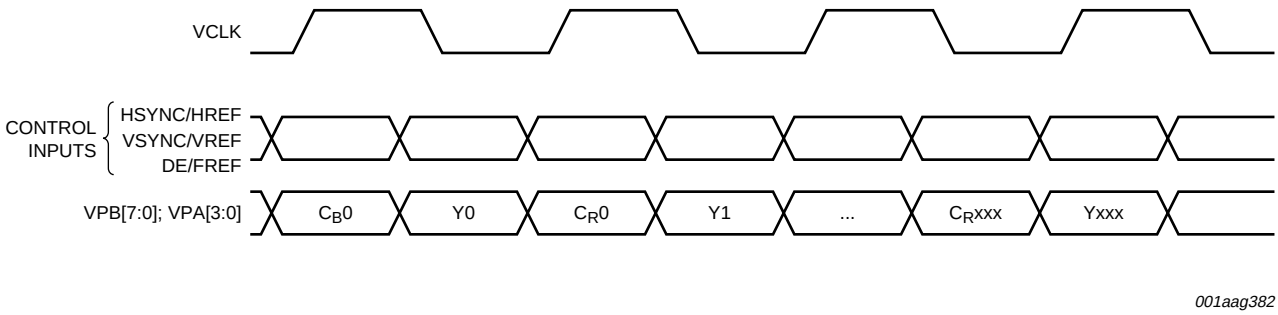


Fig 6. Pixel encoding YC_BC_R 4 : 2 : 2 ITU656-like external synchronization double edge (rising and falling) input

Table 10. YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization single edge mappings

YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2
VPA[0]	C_B[0]	Y_0[0]	C_R[0]	Y_1[0]	VPB[0]	C_B[4]	Y_0[4]	C_R[4]	Y_1[4]	HSYNC/HREF	not used
VPA[1]	C_B[1]	Y_0[1]	C_R[1]	Y_1[1]	VPB[1]	C_B[5]	Y_0[5]	C_R[5]	Y_1[5]	VSYNC/VREF	not used
VPA[2]	C_B[2]	Y_0[2]	C_R[2]	Y_1[2]	VPB[2]	C_B[6]	Y_0[6]	C_R[6]	Y_1[6]	DE/FREF	not used
VPA[3]	C_B[3]	Y_0[3]	C_R[3]	Y_1[3]	VPB[3]	C_B[7]	Y_0[7]	C_R[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	C_B[8]	Y_0[8]	C_R[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	C_B[9]	Y_0[9]	C_R[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	C_B[10]	Y_0[10]	C_R[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	C_B[11]	Y_0[11]	C_R[11]	Y_1[11]		

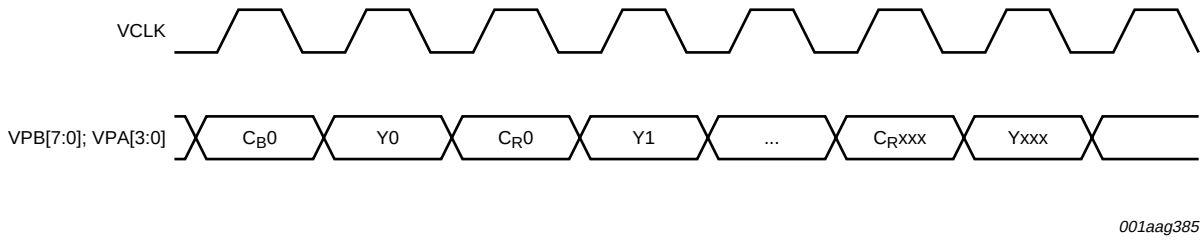


Fig 7. Pixel encoding YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization single edge (rising edge) input

Table 11. YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization double edge mappings

YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization double edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2
VPA[0]	$C_B[0]$	$Y_0[0]$	$C_R[0]$	$Y_1[0]$	VPB[0]	$C_B[4]$	$Y_0[4]$	$C_R[4]$	$Y_1[4]$	HSYNC/HREF	not used
VPA[1]	$C_B[1]$	$Y_0[1]$	$C_R[1]$	$Y_1[1]$	VPB[1]	$C_B[5]$	$Y_0[5]$	$C_R[5]$	$Y_1[5]$	VSYNC/VREF	not used
VPA[2]	$C_B[2]$	$Y_0[2]$	$C_R[2]$	$Y_1[2]$	VPB[2]	$C_B[6]$	$Y_0[6]$	$C_R[6]$	$Y_1[6]$	DE/FREF	not used
VPA[3]	$C_B[3]$	$Y_0[3]$	$C_R[3]$	$Y_1[3]$	VPB[3]	$C_B[7]$	$Y_0[7]$	$C_R[7]$	$Y_1[7]$		
VPA[4]	-	-	-	-	VPB[4]	$C_B[8]$	$Y_0[8]$	$C_R[8]$	$Y_1[8]$		
VPA[5]	-	-	-	-	VPB[5]	$C_B[9]$	$Y_0[9]$	$C_R[9]$	$Y_1[9]$		
VPA[6]	-	-	-	-	VPB[6]	$C_B[10]$	$Y_0[10]$	$C_R[10]$	$Y_1[10]$		
VPA[7]	-	-	-	-	VPB[7]	$C_B[11]$	$Y_0[11]$	$C_R[11]$	$Y_1[11]$		

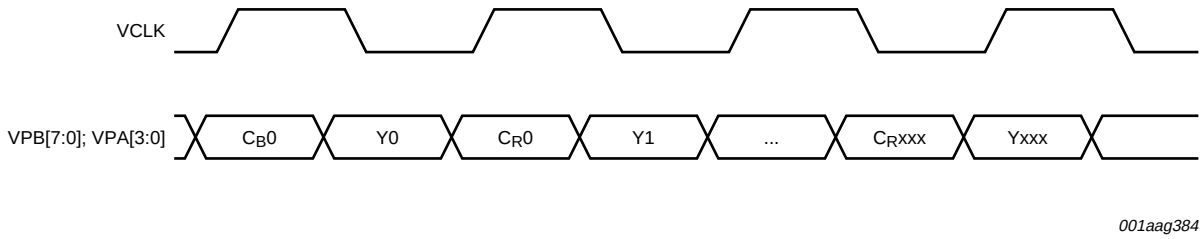


Fig 8. Pixel encoding YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization double edge (rising and falling) input

Table 12. YC_BC_R 4 : 2 : 2 semi-planar external synchronization mappings

YC_BC_R 4 : 2 : 2 semi-planar external synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YC_BC_R 4 : 2 : 2 semi-planar		Pin	YC_BC_R 4 : 2 : 2 semi-planar		Pin	YC_BC_R 4 : 2 : 2 semi-planar		Pin	YC_BC_R 4 : 2 : 2
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	C_B[4]	C_R[4]	HSYNC/HREF	used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	C_B[5]	C_R[5]	VSYNC/VREF	used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	C_B[6]	C_R[6]	DE/FREF	used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	C_B[7]	C_R[7]		
VPA[4]	C_B[0]	C_R[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	C_B[8]	C_R[8]		
VPA[5]	C_B[1]	C_R[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	C_B[9]	C_R[9]		
VPA[6]	C_B[2]	C_R[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	C_B[10]	C_R[10]		
VPA[7]	C_B[3]	C_R[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	C_B[11]	C_R[11]		

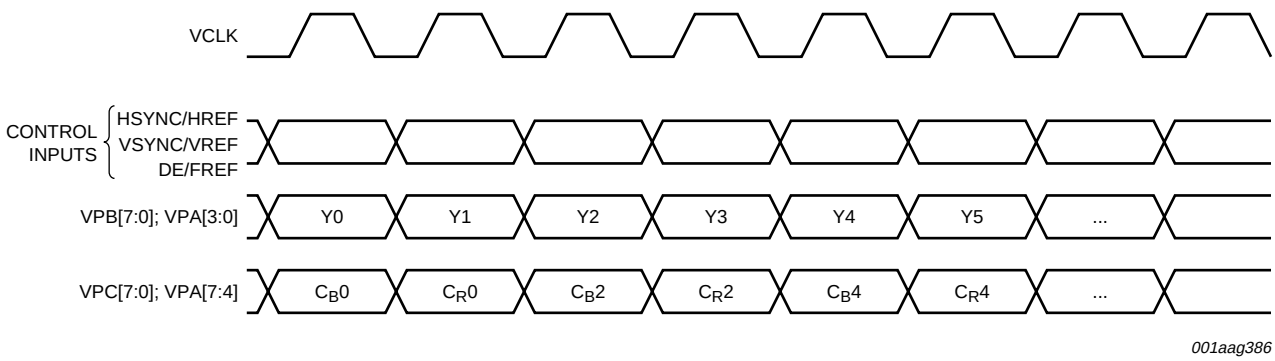


Fig 9. Pixel encoding YC_BC_R 4 : 2 : 2 semi-planar external synchronization (rising edge) input

Table 13. YC_BC_R 4 : 2 : 2 semi-planar embedded synchronization mappings

YC_BC_R 4 : 2 : 2 semi-planar embedded synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	**YC_BC_R 4 : 2 : 2 semi-planar**		**Pin**	**YC_BC_R 4 : 2 : 2 semi-planar**		**Pin**	**YC_BC_R 4 : 2 : 2 semi-planar**		**Pin**	**YC_BC_R 4 : 2 : 2**
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	C_B[4]	C_R[4]	HSYNC/HREF	not used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	C_B[5]	C_R[5]	VSYNC/VREF	not used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	C_B[6]	C_R[6]	DE/FREF	not used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	C_B[7]	C_R[7]		
VPA[4]	C_B[0]	C_R[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	C_B[8]	C_R[8]		
VPA[5]	C_B[1]	C_R[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	C_B[9]	C_R[9]		
VPA[6]	C_B[2]	C_R[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	C_B[10]	C_R[10]		
VPA[7]	C_B[3]	C_R[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	C_B[11]	C_R[11]		

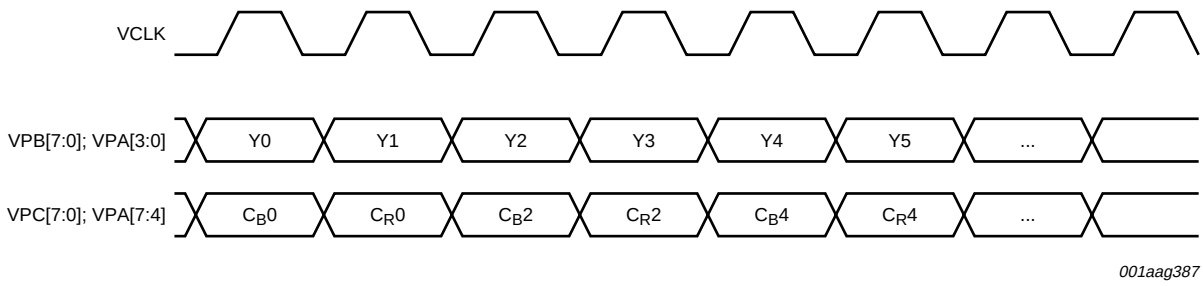


Fig 10. Pixel encoding YC_BC_R 4 : 2 : 2 semi-planar embedded synchronization (rising edge) input

8.3 Synchronization

The TDA9983B can be synchronized with Hsync/Vsync external inputs or with extraction of the sync information from embedded sync (SAV/EAV) codes inside the video stream.

8.3.1 Timing extraction generator

This block can extract the synchronization signals Href, Vref and Fref from Start Active Video (SAV) and End Active Video (EAV) in case of embedded synchronization in the data stream. Synchronization signals can be embedded in RGB, YC_BC_R 4 : 4 : 4, YC_BC_R 4 : 2 : 2 semi-planar (up to 2 × 12-bit), YC_BC_R 4 : 2 : 2 ITU656 and ITU656-like (up to 1 × 12-bit).

8.3.2 Data enable generator

The TDA9983B contains a Data Enable (DE) generator; this can generate an internal DE signal for a system which does not provide one.

8.4 Input and output video format

Due to the flexible video input formatter, the TDA9983B can accept a large range of input formats. This flexibility allows the TDA9983B to be compatible with the maximum possible number of MPEG decoders. Moreover, these input formats may be changed in many ways (color space converter, upsampler, downsampler and scaler) to be transmitted across the HDMI link. Table 14 gives the possible inputs and outputs.

Table 14. Use of color space converter, upsampler, downsampler and scaler

Input			Scaler	Output		
Color space	Format	Channels		Color space	Format	Channels
RGB	4 : 4 : 4	3 × 8-bit	no scaling	RGB	4 : 4 : 4	3 × 8-bit
			no scaling	YC_BC_R	4 : 2 : 2	2 × 12-bit
			no scaling	YC_BC_R	4 : 4 : 4	3 × 8-bit
YC_BC_R	4 : 4 : 4	3 × 8-bit	no scaling	RGB	4 : 4 : 4	3 × 8-bit
			no scaling	YC_BC_R	4 : 2 : 2	2 × 12-bit
			no scaling	YC_BC_R	4 : 4 : 4	3 × 8-bit
YC_BC_R	4 : 2 : 2	up to 1 × 12-bit	scalable	YC_BC_R	4 : 2 : 2	2 × 12-bit
			scalable	YC_BC_R	4 : 4 : 4	3 × 8-bit
			scalable	RGB	4 : 4 : 4	3 × 8-bit
		up to 2 × 12-bit	scalable	YC_BC_R	4 : 2 : 2	2 × 12-bit
			scalable	YC_BC_R	4 : 4 : 4	3 × 8-bit
			scalable	RGB	4 : 4 : 4	3 × 8-bit

8.5 Upsampler

The incoming YC_BC_R 4 : 2 : 2 (2 × 12-bit) data stream format could be upsampled into a 12-bit YC_BC_R 4 : 4 : 4 (3 × 12-bit) data stream by repeating or linearly interpolating the chrominance pixels.

8.6 Color space converter

The color space converter is used to convert input video data from one type to another color space (RGB to YC_BC_R and YC_BC_R to RGB). This block can be bypassed and each coefficient is programmable via the I²C-bus register.

$$\begin{bmatrix} Y\backslash G \\ C_B\backslash R \\ C_R\backslash B \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left(\begin{bmatrix} G\backslash Y \\ R\backslash C_B \\ B\backslash C_R \end{bmatrix} + \begin{bmatrix} Oin_{G\backslash Y} \\ Oin_{R\backslash C_B} \\ Oin_{B\backslash C_R} \end{bmatrix} \right) + \begin{bmatrix} Oout_{Y\backslash G} \\ Oout_{C_B\backslash R} \\ Oout_{C_R\backslash B} \end{bmatrix}$$

8.7 Downsampler

This block works only with YC_BC_R input format; these filters downsample the C_B and C_R signals by a factor 2. A delay is added on the G/Y channel, which corresponds to the pipeline delay of the filters, to put the Y channel in phase with the C_B-C_R channels.

8.8 Audio input format

The TDA9983B is compatible with HDMI 1.2a (DVD support). The TDA9983B can carry audio in I²S-bus format (one stereo up to four stereo channels) or in S/PDIF format. S/PDIF or I²S-bus format can be selected via the I²C-bus. Only one audio format can be used at a time: either S/PDIF or I²S-bus. Table 15 shows the audio port allocation.

Table 15. Audio port configuration

All audio ports are LV-TTL compatible.

Audio port	I²S-bus and S/PDIF input configuration
AP0	WS (word select)
AP1	I²S-bus audio port 0
AP2	I²S-bus audio port 1
AP3	I²S-bus audio port 2
AP4	I²S-bus audio port 3
AP5	MCLK (master clock for S/PDIF)
AP6	S/PDIF input
AP7	AUX (internal test)
ACLK	SCK (I²S-bus clock)

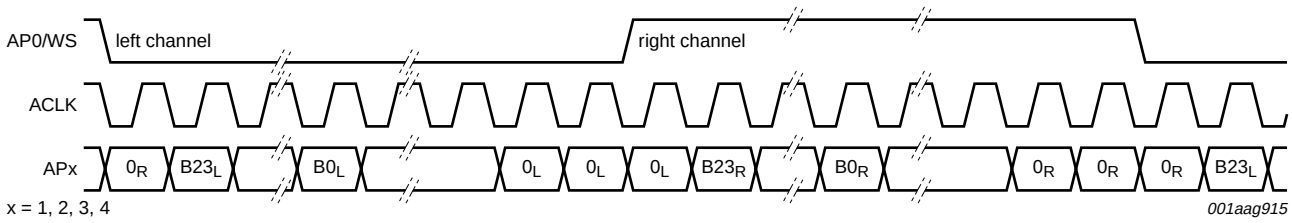
8.9 S/PDIF

The audio port AP6 is used for the S/PDIF feature. In this format the TDA9983B supports 2-channel uncompressed PCM data (IEC 60958) layout 0 or compressed bit stream up to 8 multichannels (Dolby Digital, DTS, AC-3, etc.) layout 1. The TDA9983B is able to recover the original clock from the S/PDIF signal (no need for an external clock). In addition it can also use an external clock (MCLK) to decode the S/PDIF signal.

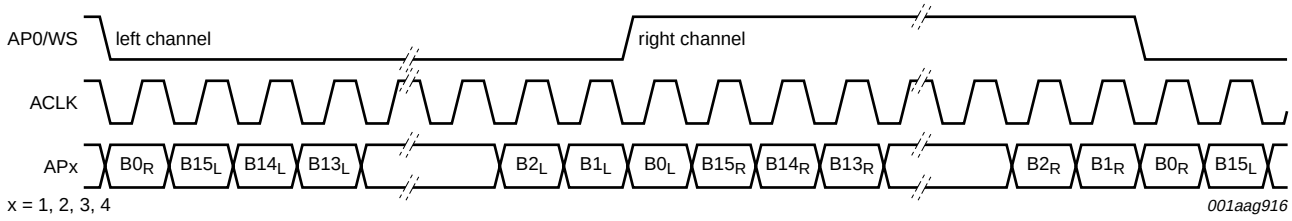
8.10 I²S-bus

The TDA9983B supports the NXP I²S-bus format. There are four I²S-bus stereo input channels (AP1 to AP4), which enable 8 uncompressed audio channels to be carried. The I²S-bus input interface receives an I²S-bus signal including serial data, word select and

serial clock. Various I²S-bus formats are supported and can be selected by setting the appropriate bits of the register. The I²S-bus input interface can receive up to 24-bit wide audio samples via the serial data input with a clock frequency of at least 32 times the input sample frequency f_s. Since the I²S-bus format is MSB aligned, audio data with an arbitrary precision can be received automatically. Audio samples with a precision better than 24 bits are truncated to 24 bits. If the input clock has a frequency of $32 \times f_s$, only 16-bit audio samples can be received. In this case, the 8 LSBs will be set to logic 0. The serial data signal carries the serial baseband audio data, sample by sample left/right interleaved. The word select signal WS indicates whether left or right channel information is transferred over the serial data line. The formats for 16-bit and 32-bit modes are shown in Figure 11.



a. 32-bit mode



b. 16-bit mode

Fig 11. NXP I²S-bus formats

8.11 Power management

The TDA9983B can be powered down via the I²C-bus register.

8.12 Interrupt controller

Pin INT is used to alert the microcontroller that a critical event concerning the HDMI has occurred (hot plug detect). This interrupt is maskable.

Hot plug or unplug detect: pin HPD is the hot plug detection pin; it is 5 V input tolerant.

8.13 Initialization

Hard reset: after power-up, the TDA9983B is activated by a hard reset via pin RST_N. However, the TDA9983B has a power-on reset.

8.14 HDMI

8.14.1 Output HDMI buffers

An external resistor must be used to set the HDMI output amplitude. It has to be connected between pin EXT_SWING and $V_{DDH(3V3)}$.

8.14.2 Pixel repetition

To transmit video formats with pixel rates below 25 Msample/s or to increase the number of audio sample packets in each frame, the TDA9983B uses pixel repetition to increase the transmitted pixel clock.

Table 16. Pixel repetition

SRL_PR[3]	SRL_PR[2]	SRL_PR[1]	SRL_PR[0]	Pixel repeated
0	0	0	0	no repetition
0	0	0	1	once
0	0	1	0	twice
0	0	1	1	3 times
0	1	0	0	4 times
0	1	0	1	5 times
0	1	1	0	6 times
0	1	1	1	7 times
1	0	0	0	8 times
1	0	0	1	9 times
1	0	1	x	undefined
1	1	x	x	undefined

8.14.3 HDMI and DVI receiver discrimination

This information is located in the E-EDID receiver part, in the ‘Vendor-Specific Data block’ within the first CEA EDID timing extension. If the 24-bit IEEE registration identifier contains the value 00 0C03h, then the receiver will support HDMI, otherwise the device will be treated as a DVI device. However, the TDA9983B does not have direct access to that information since E-EDID is read by an external microprocessor through the TDA9983B I^2C-bus gate.

8.14.4 DDC channel

The DDC-bus pins DDC_SDA and DDC_SCL are 5 V tolerant and can work at standard mode (100 kHz).

8.14.4.1 E-EDID reading

In order to get receiver capabilities, the TDA9983B must read the E-EDID of the receiver. This is made possible by temporarily connecting the I^2C-bus to the DDC lines, so that the microprocessor is able to read full EDID.

8.15 Scaler unit

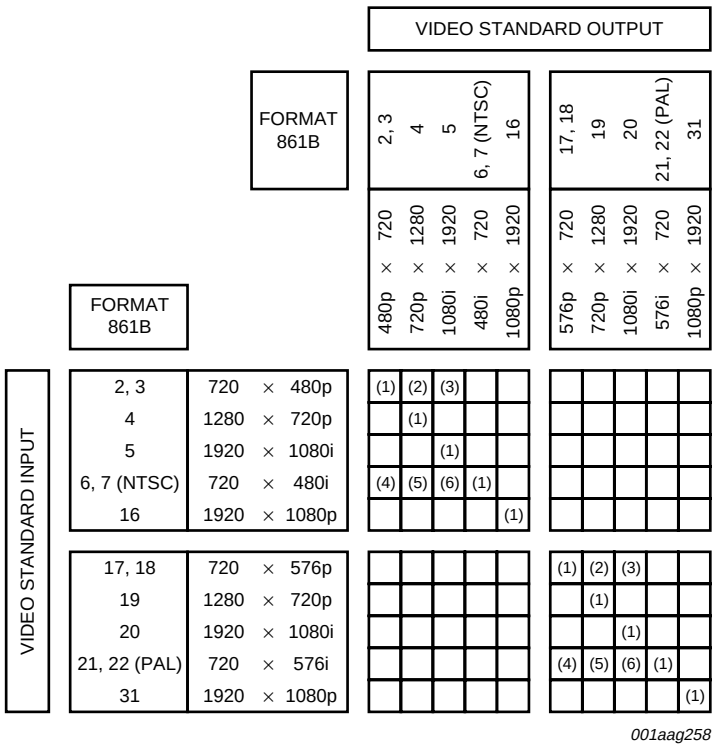
The scaler unit has the following features:

- Upscaling only: to expand input image horizontally and vertically

- Embedded deinterlacer (no need for output memory)
- Maximum output operating frequency: 74.5 MHz (HDTV supported 1080i, 720p)
- Input video standards (YC_BC_R 4 : 2 : 2 semi-planar, ITU656 and ITU656-like YC_BC_R, no RGB and no YC_BC_R 4 : 4 : 4)

8.16 Input and output video scaler

The scaler converts the standard definition video signals (480i/576i, 480p/576p) into 720p, 1080i as illustrated in Figure 12.



All upscaling modes are available only for YC_BC_R 4 : 2 : 2 input format.

(1) Pass through
(2) Upscaling
(3) Upscaling and interlacing
(4) Deinterlacing
(5) Deinterlacing and upscaling
(6) Deinterlacing, upscaling and interlacing

Fig 12. Input and output video scaler

8.17 I²C-bus interface

The I²C-bus pins I2C_SDA and I2C_SCL are 5 V tolerant and can work at fast mode (400 kHz).

9. I²C-bus register definitions

9.1 I²C-bus protocol

The registers of the TDA9983B can be accessed via the I²C-bus. The TDA9983B is used as a slave device and both the fast mode 400 kHz and the standard mode 100 kHz are supported.

Bits A0 and A1 of the I²C-bus device address are externally selected by pins A0 and A1. The I²C-bus device address is given in Table 17.

Table 17. Device address

Device address							R/$\overline{W}$
A6	A5	A4	A3	A2	A1	A0	-
1	1	1	0	0	A1	A0	1/0

The I²C-bus access format is shown in Figure 13.

For read access, the master writes the address of the TDA9983B, the subaddress to access the specific register and then the data.

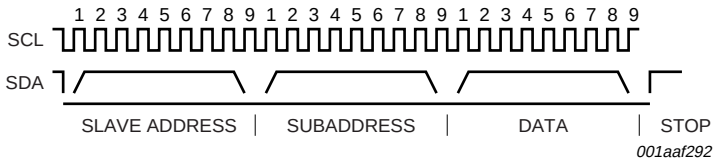


Fig 13. I²C-bus access

9.2 Memory page management

The I²C-bus memory is split into several pages and the selection between pages is made with common register CURPAGE_ADR. It is only necessary to write in this register once to change the current page. So multiple read or write operations in the same page need a write register CURPAGE_ADR once at the beginning.

Table 18. Memory pages

Page address	Memory page description	Reference
00h	General control	see Section 9.3 on page 23
01h	Scaler	see Section 9.4 on page 43
02h	PLL settings	see Section 9.5 on page 55
10h	Information frames and packets	see Section 9.6 on page 63
11h	Audio settings and content info packets	see Section 9.7 on page 81
12h	HDMI and DVI	see Section 9.8 on page 98

9.3 General control page register definitions

The current page address for the general control page is 00h.

The configuration of the registers for this page is given in Table 19.

Table 19. I²C-bus registers of memory page 00h[1]

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
VERSION	00h	R	0	1	1	0	0	0	1	0	0110 0010
MAIN_CNTRL0	01h	W	SCALER	x	x	CEHS	CECS	DEHS	DECS	SR	0000 0000
Not used	02h	-	-								0000 0000
:	:	:	:								:
Not used	0Eh	-	-								0000 0000
INT_FLAGS_0	0Fh	R/W	x	x	x	x	x	x	HPD	x	0000 0000
INT_FLAGS_1	10h	R/W	HPD_IN	x	SC_DEIL	SC_VID	SC_OUT	SC_IN	x	VS_RPT	0000 0000
Not used	11h	-	-								0000 0000
:	:	:	:								:
Not used	1Fh	-	-								0000 0000
VIP_CNTRL_0	20h	W	MIRR_A	SWAP_A[2:0]			MIRR_B	SWAP_B[2:0]			0000 0001
VIP_CNTRL_1	21h	W	MIRR_C	SWAP_C[2:0]			MIRR_D	SWAP_D[2:0]			0010 0100
VIP_CNTRL_2	22h	W	MIRR_E	SWAP_E[2:0]			MIRR_F	SWAP_F[2:0]			0101 0110
VIP_CNTRL_3	23h	W	EDGE	x	SP_SYNC[1:0]		EMB	V_TGL	H_TGL	X_TGL	0001 0110
VIP_CNTRL_4	24h	W	TST_PAT	TST_656	x	CCIR656	BLANKIT[1:0]		BLC[1:0]		0000 0001
VIP_CNTRL_5	25h	W	x	x	x	x	x	SP_CNT[1:0]		CKCASE	0000 0000
Not used	26h	-	-								0000 0000
:	:	:	:								:
Not used	7Fh	-	-								0000 0000
MAT_CONTRL	80h	W	x	x	x	x	x	MAT_BP	MAT_SC[1:0]		0000 0101
MAT_OI1_MSB	81h	W	x	x	x	x	x	OFFSET_IN1[10:8]			0000 0000
MAT_OI1_LSB	82h	W	OFFSET_IN1[7:0]								0000 0000
MAT_OI2_MSB	83h	W	x	x	x	x	x	OFFSET_IN2[10:8]			0000 0110
MAT_OI2_LSB	84h	W	OFFSET_IN2[7:0]								0000 0000
MAT_OI3_MSB	85h	W	x	x	x	x	x	OFFSET_IN3[10:8]			0000 0110
MAT_OI3_LSB	86h	W	OFFSET_IN3[7:0]								0000 0000
MAT_P11_MSB	87h	W	x	x	x	x	x	P11[10:8]			0000 0010
MAT_P11_LSB	88h	W	P11[7:0]								0000 0000
MAT_P12_MSB	89h	W	x	x	x	x	x	P12[10:8]			0000 0110
MAT_P12_LSB	8Ah	W	P12[7:0]								1001 0010
MAT_P13_MSB	8Bh	W	x	x	x	x	x	P13[10:8]			0000 0111
MAT_P13_LSB	8Ch	W	P13[7:0]								0101 0000

Table 19. I²C-bus registers of memory page 00h[1] …continued

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
MAT_P21_MSB	8Dh	W	x	x	x	x	x	P21[10:8]			0000 0010
MAT_P21_LSB	8Eh	W	P21[7:0]								0000 0000
MAT_P22_MSB	8Fh	W	x	x	x	x	x	P22[10:8]			0000 0010
MAT_P22_LSB	90h	W	P22[7:0]								1100 1110
MAT_P23_MSB	91h	W	x	x	x	x	x	P23[10:8]			0000 0000
MAT_P23_LSB	92h	W	P23[7:0]								0000 0000
MAT_P31_MSB	93h	W	x	x	x	x	x	P31[10:8]			0000 0010
MAT_P31_LSB	94h	W	P31[7:0]								0000 0000
MAT_P32_MSB	95h	W	x	x	x	x	x	P32[10:8]			0000 0000
MAT_P32_LSB	96h	W	P32[7:0]								0000 0000
MAT_P33_MSB	97h	W	x	x	x	x	x	P33[10:8]			0000 0011
MAT_P33_LSB	98h	W	P33[7:0]								1000 1100
MAT_OO1_MSB	99h	W	x	x	x	x	x	OFFSET_OUT1[10:8]			0000 0000
MAT_OO1_LSB	9Ah	W	OFFSET_OUT1[7:0]								0000 0000
MAT_OO2_MSB	9Bh	W	x	x	x	x	x	OFFSET_OUT2[10:8]			0000 0000
MAT_OO2_LSB	9Ch	W	OFFSET_OUT2[7:0]								0000 0000
MAT_OO3_MSB	9Dh	W	x	x	x	x	x	OFFSET_OUT3[10:8]			0000 0000
MAT_OO3_LSB	9Eh	W	OFFSET_OUT3[7:0]								0000 0000
Not used	9Fh	-	-	-	-	-	-	-	-	-	0000 0000
VIDFORMAT	A0h	W	x	x	x	VIDFORMAT[4:0]					0000 0000
REFPIX_MSB	A1h	W	x	x	x	PRESET_PIX[12:8]					0000 0000
REFPIX_LSB	A2h	W	PRESET_PIX[7:0]								0000 0001
REFLINE_MSB	A3h	W	x	x	x	x	x	PRESET_LINE[10:8]			0000 0000
REFLINE_LSB	A4h	W	PRESET_LINE[7:0]								0000 0001
NPIX_MSB	A5h	W	x	x	x	NPIX[12:8]					0000 0000
NPIX_LSB	A6h	W	NPIX[7:0]								0000 0000
NLINE_MSB	A7h	W	x	x	x	x	x	NLINE[10:8]			0000 0000
NLINE_LSB	A8h	W	NLINE[7:0]								0000 0000
VS_LINE_STRT_1_MSB	A9h	W	x	x	x	x	x	VS_LINE_START_1[10:8]			0000 0000
VS_LINE_STRT_1_LSB	AAh	W	VS_LINE_START_1[7:0]								0000 0000
VS_PIX_STRT_1_MSB	ABh	W	x	x	x	VS_PIX_START_1[12:8]					0000 0000
VS_PIX_STRT_1_LSB	ACh	W	VS_PIX_START_1[7:0]								0000 0000

Table 19. I²C-bus registers of memory page 00h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
VS_LINE_END_1_MSB	ADh	W	x	x	x	x	x	VS_LINE_END_1[10:8]			0000 0000
VS_LINE_END_1_LSB	AEh	W	VS_LINE_END_1[7:0]								0000 0000
VS_PIX_END_1_MSB	AFh	W	x	x	x	VS_PIX_END_1[12:8]					0000 0000
VS_PIX_END_1_LSB	B0h	W	VS_PIX_END_1[7:0]								0000 0000
VS_LINE_STRT_2_MSB	B1h	W	x	x	x	x	x	VS_LINE_START_2[10:8]			0000 0000
VS_LINE_STRT_2_LSB	B2h	W	VS_LINE_START_2[7:0]								0000 0000
VS_PIX_STRT_2_MSB	B3h	W	x	x	x	VS_PIX_START_2[12:8]					0000 0000
VS_PIX_STRT_2_LSB	B4h	W	VS_PIX_START_2[7:0]								0000 0000
VS_LINE_END_2_MSB	B5h	W	x	x	x	x	x	VS_LINE_END_2[10:8]			0000 0000
VS_LINE_END_2_LSB	B6h	W	VS_LINE_END_2[7:0]								0000 0000
VS_PIX_END_2_MSB	B7h	W	x	x	x	VS_PIX_END_2[12:8]					0000 0000
VS_PIX_END_2_LSB	B8h	W	VS_PIX_END_2[7:0]								0000 0000
HS_PIX_START_MSB	B9h	W	x	x	x	HS_PIX_START[12:8]					0000 0000
HS_PIX_START_LSB	BAh	W	HS_PIX_START[7:0]								0000 0000
HS_PIX_STOP_MSB	BBh	W	x	x	x	HS_PIX_END[12:8]					0000 0000
HS_PIX_STOP_LSB	BCh	W	HS_PIX_END[7:0]								0000 0000
VWIN_START_1_MSB	BDh	W	x	x	x	x	x	VWIN_START_1[10:8]			0000 0000
VWIN_START_1_LSB	BEh	W	VWIN_START_1[7:0]								0000 0000
VWIN_END_1_MSB	BFh	W	x	x	x	x	x	VWIN_END_1[10:8]			0000 0000
VWIN_END_1_LSB	C0h	W	VWIN_END_1[7:0]								0000 0000
VWIN_START_2_MSB	C1h	W	x	x	x	x	x	VWIN_START_2[10:8]			0000 0000
VWIN_START_2_LSB	C2h	W	VWIN_START_2[7:0]								0000 0000
VWIN_END_2_MSB	C3h	W	x	x	x	x	x	VWIN_END_2[10:8]			0000 0000
VWIN_END_2_LSB	C4h	W	VWIN_END_2[7:0]								0000 0000
DE_START_MSB	C5h	W	x	x	x	DE_START[12:8]					0000 0000
DE_START_LSB	C6h	W	DE_START[7:0]								0000 0000
DE_STOP_MSB	C7h	W	x	x	x	DE_END[12:8]					0000 0000
DE_STOP_LSB	C8h	W	DE_END[7:0]								0000 0000
COLBAR_WIDTH	C9h	W	CBW[7:0]								0000 0000
TBG_CNTRL_0	CAh	W	SYNC_ ONCE	SYNC_ MTHD	FRAME_ DIS	x	x	x	x	x	0000 0000
TBG_CNTRL_1	CBh	W	x	DWIN_DIS	VHX_EXT[2:0]			VH_TGL[2:0]			0000 0000

Table 19. I²C-bus registers of memory page 00h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
VBL_OFFSET_START	CCh	W	VBLOFF_START[7:0]								0000 0000
VBL_OFFSET_END	CDh	W	VBLOFF_END[7:0]								0000 0000
HBL_OFFSET_START	CEh	W	HBLOFF_START[7:0]								0000 0000
HBL_OFFSET_END	CFh	W	HBLOFF_END[7:0]								0000 0000
DWIN_RE_DE	D0h	W	DWIN_RE_DE[7:0]								0001 0001
DWIN_FE_DE	D1h	W	DWIN_FE_DE[7:0]								0111 1010
Not used	D2h	-	-								0000 0000
:	:	:	:								:
Not used	E3h	-	-								0000 0000
HVF_CNTRL_0	E4h	W	SM	RWB	x	x	PREFIL[1:0]		INTPOL[1:0]		0000 0000
HVF_CNTRL_1	E5h	W	x	SEMI_PLANAR	PAD[1:0]		VQR[1:0]		YUVBLK	FOR	0x00 0000
Not used	E6h	-	-								0000 0000
Not used	E7h	-	-								0000 0000
TIMER_H	E8h	W	IM_CLKSEL	WD_CLKSEL	x	x	x	x	TIM_H[1:0]		xx00 0001
TIMER_M	E9h	W	TIM_M[7:0]								1100 0010
TIMER_L	EAh	W	TIM_L[7:0]								0100 0000
Not used	EBh	-	-								0000 0000
:	:	:	:								:
Not used	EDh	-	-								0000 0000
NDIV_IM	EEh	W	x	x	x	x	NDIV_IM[3:0]				0000 0011
NDIV_PF	EFh	W	NDIF_PF[7:0]								0001 1011
RPT_CNTRL	F0h	W	x	x	x	x	REPEAT[3:0]				0000 0000
LEAD_OFF	F1h	W	x	x	x	x	LEAD_OFFSET[3:0]				0000 0010
TRAIL_OFF	F2h	W	x	x	x	x	TRAIL_OFFSET[3:0]				0000 0010
Not used	F3h	-	-								0000 0000
:	:	:	:								:
Not used	F7h	-	-								0000 0000
For test	F8h	W	x	x	x	x	x	x	x	x	0000 0000
GHOST_XADDR	F9h	W	GHOST_XADDR[6:0]							A0_ZERO	0110 0000
Not used	FAh	-	-	-	-	-	-	-	-	-	0000 0000
Not used	FBh	-	-	-	-	-	-	-	-	-	0000 0000

Table 19. I²C-bus registers of memory page 00h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
Not used	FCh	-	-	-	-	-	-	-	-	-	0000 0000
AIP_CLKSEL	FDh	W	x	x	x	SEL_AIP[1:0]		SEL_POL_CLK	SEL_FS[1:0]		0000 0000
GHOST_ADDR	FEh	W	GHOST_ADDR[6:0]							GHOST_DIS	1010 0001
CURPAGE_ADR	FFh	W	CURPAGE_ADR[7:0]								0000 0000

[1] R: reading register
W: writing register
x: bit must be set to default value for proper operation
-: not used

9.3.1 Main control register

Table 20. VERSION register (address 00h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 4	-	R	0110	TDA9983B device version
3 to 0	-	R	0010	die version

Table 21. MAIN_CNTRL0 register (address 01h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	SCALER	W		**scaler**
			0*	HDMI video formatter uses vip-output (scaler is bypassed)
			1	HDMI video formatter uses scaler-output
6 to 5	x	W	00*	undefined
4	CEHS	W		**I^2C-bus enable high speed**
			0*	I2C_SDA and I2C_SCL set to Standard or Fast mode
			1	I2C_SDA and I2C_SCL set to High-speed mode
3	CECS	W		**I^2C-bus enable current source**
			0*	I2C_SCL pull-up current source disabled
			1	I2C_SCL pull-up current source enabled
2	DEHS	W		**DDC-bus enable high speed**
			0*	DDC_SDA and DDC_SCL set to Standard or Fast mode
			1	DDC_SDA and DDC_SCL set to High-speed mode
1	DECS	W		**DDC-bus enable current source**
			0*	DDC_SCL pull-up current source disabled
			1	DDC_SCL pull-up current source enabled
0	SR	W		**soft reset**
			0*	no specific action
			1	soft reset for all modules which do not use the cclk clock domain

9.3.2 Interrupt flags/masks registers

Table 22. INT_FLAGS_0 register (address 0Fh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 2	x	R/W	0000 00*	undefined
1	HPD	R/W		**HPD:** transition on HPD input
			0*	FALSE/INT_disabled
			1	TRUE/INT_enabled
0	x	R/W	0*	undefined

Table 23. INT_FLAGS_1 register (address 10h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	HPD_IN	R/W		**HPD input:** transition on HPD input
			0*	HPD is LOW
			1	HPD is HIGH
6	x	R/W	0*	undefined
5	SC_DEIL	R/W		**scaler deinterlace:** scaler deinterlaced video buffer failure
			0*	FALSE/INT_disabled
			1	TRUE/INT_enabled
4	SC_VID	R/W		**scaler video:** scaler primary video buffer full failure
			0*	FALSE/INT_disabled
			1	TRUE/INT_enabled
3	SC_OUT	R/W		**scaler output:** scaler output failure
			0*	FALSE/INT_disabled
			1	TRUE/INT_enabled
2	SC_IN	R/W		**scaler input**: scaler input failure
			0*	FALSE/INT_disabled
			1	TRUE/INT_enabled
1	x	R/W	0*	undefined
0	VS_RPT	R/W		**rising edge on VS_RPT detected**
			0*	FALSE/INT_disabled
			1	TRUE/INT_enabled

9.3.3 Video input processing control registers

Table 24. VIP_CNTRL_0 register (address 20h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	MIRR_A	W		**mirror A**
			0*	no specific action
			1	mirror nibble; m[23:20] = s[20:23]
6 to 4	SWAP_A[2:0]	W		**swap A selector**
			000*	pin VPC[7:4] = vp[23:20]
			001	pin VPC[3:0] = vp[23:20]
			010	pin VPB[7:4] = vp[23:20]
			011	pin VPB[3:0] = vp[23:20]
			100	pin VPA[7:4] = vp[23:20]
			other	pin VPA[3:0] = vp[23:20]
3	MIRR_B	W		**mirror B**
			0*	no specific action
			1	mirror nibble; m[19:16] = s[16:19]

Table 24. VIP_CNTRL_0 register (address 20h) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
2 to 0	SWAP_B[2:0]	W		**swap B selector**
			000	pin VPC[7:4] = vp[19:16]
			001*	pin VPC[3:0] = vp[19:16]
			010	pin VPB[7:4] = vp[19:16]
			011	pin VPB[3:0] = vp[19:16]
			100	pin VPA[7:4] = vp[19:16]
			other	pin VPA[3:0] = vp[19:16]

Table 25. VIP_CNTRL_1 register (address 21h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	MIRR_C	W		**mirror C**
			0*	no specific action
			1	mirror nibble; m[15:12] = s[12:15]
6 to 4	SWAP_C[2:0]	W		**swap C selector**
			000	pin VPC[7:4] = vp[15:12]
			001	pin VPC[3:0] = vp[15:12]
			010*	pin VPB[7:4] = vp[15:12]
			011	pin VPB[3:0] = vp[15:12]
			100	pin VPA[7:4] = vp[15:12]
			other	pin VPA[3:0] = vp[15:12]
3	MIRR_D	W		**mirror D**
			0*	no specific action
			1	mirror nibble; m[11:8] = s[8:11]
2 to 0	SWAP_D[2:0]	W		**swap D selector**
			000	pin VPC[7:4] = vp[11:8]
			001	pin VPC[3:0] = vp[11:8]
			010	pin VPB[7:4] = vp[11:8]
			011	pin VPB[3:0] = vp[11:8]
			100*	pin VPA[7:4] = vp[11:8]
			other	pin VPA[3:0] = vp[11:8]

Table 26. VIP_CNTRL_2 register (address 22h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	MIRR_E	W		**mirror E**
			0*	no specific action
			1	mirror nibble; m[7:4] = s[4:7]

Table 26. VIP_CNTRL_2 register (address 22h) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
6 to 4	SWAP_E[2:0]	W		**swap E selector**
			000	pin VPC[7:4] = vp[7:4]
			001	pin VPC[3:0] = vp[7:4]
			010	pin VPB[7:4] = vp[7:4]
			011	pin VPB[3:0] = vp[7:4]
			100	pin VPA[7:4] = vp[7:4]
			101*	pin VPA[3:0] = vp[7:4]
			other	pin VPA[3:0] = vp[7:4]
3	MIRR_F	W		**mirror F**
			0*	no specific action
			1	mirror nibble; m[3:0] = s[0:3]
2 to 0	SWAP_F[2:0]	W		**swap F selector**
			000	pin VPC[7:4] = vp[3:0]
			001	pin VPC[3:0] = vp[3:0]
			010	pin VPB[7:4] = vp[3:0]
			011	pin VPB[3:0] = vp[3:0]
			100	pin VPA[7:4] = vp[3:0]
			110*	pin VPA[3:0] = vp[3:0]
			other	pin VPA[3:0] = vp[3:0]

Table 27. VIP_CNTRL_3 register (address 23h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	EDGE	W		**edge**
			0*	vp-bus synchronized on positive edge of vip_clk_m
			1	vp-bus synchronized on negative edge of vip_clk_m
6	x	W	0*	undefined
5 to 4	SP_SYNC[1:0]	W		**sp synchronization**
			00	sp_cnt synchronized by hemb
			01*	sp_cnt synchronized by rising edge de
			10	sp_cnt synchronized by rising edge of hs
			11	sp_cnt fixed at i2c_sp_cnt
3	EMB	W		**embedded**
			0*	no specific action
			1	use embedded synchronization codes
2	V_TGL	W		**v_toggle**
			0	no specific action
			1*	toggle vs/vref

Table 27. VIP_CNTRL_3 register (address 23h) bit description *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
1	H_TGL	W		**h_toggle**
			0	no specific action
			1*	toggle hs/href
0	X_TGL	W		**x_toggle**
			0*	no specific action
			1	toggle de/fref

Table 28. VIP_CNTRL_4 register (address 24h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	TST_PAT	W		**test pattern**
			0*	no specific action
			1	insert test pattern with high data activity
6	TST_656	W		**test 656**: test mode (ITU656 via audio port AP)
			0*	no specific action
			1	inject ITU656 video via audio port
5	x	W	0*	undefined
4	CCIR656	W		**CCIR 656**: ITU656 or ITU656-like at the input
			0*	no specific action
			1	activate ITU data demultiplexing (from ITU656 or ITU656-like to 4 : 2 : 2 semi-planar)
3 to 2	BLANKIT[1:0]	W		**blankit:** select source for blankit control
			00*	not de
			01	hs AND vs
			10	(not hs) AND vs
			11	hemb AND vemb
1 to 0	BLC[1:0]	W		**blanking codes**
			00	no insertion of blanking codes or test pattern
			01*	blanking codes set to RGB 4 : 4 : 4 levels
			10	blanking codes set to YUV 4 : 4 : 4 levels
			11	blanking codes set to YUV 4 : 2 : 2 levels

Table 29. VIP_CNTRL_5 register (address 25h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 3	x	W	0000 0*	undefined
2 to 1	SP_CNT[1:0]	W		**sp counter**
			00*	sp_cnt preset to ’00’
			01	sp_cnt preset to ’01’
			10	sp_cnt preset to ’10’
			11	sp_cnt preset to ’11’

Table 29. VIP_CNTRL_5 register (address 25h) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
0	CKCASE	W		**ckcase**
			0*	no specific action
			1	toggle clk1case (phase clk1 with respect to clk2)

9.3.4 Color space conversion registers

Table 30. MAT_CONTRL register (address 80h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 3	x	W	0000 0*	undefined
2	MAT_BP	W		**matrix bypassed:** bypasses or not the matrix and offsets
			0	uses color space conversion
			1*	bypasses
1 and 0	MAT_SC[1:0]	W		**matrix scale factor selection:** sets the scale factor to convert the floating matrix [C_{xy}] into an integer matrix [P_{xy}]: $\begin{bmatrix} P_{11} & P_{12} & P_{13} \\ P_{21} & P_{22} & P_{23} \\ P_{31} & P_{32} & P_{33} \end{bmatrix} = INT(S \times \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix})$ The choice depends on the biggest coefficient in absolute value $\lvert C_{xy} \rvert$
			00	when $2 \leq \lvert C_{xy} \rvert < 4$; S = 256
			01*	when $1 \leq \lvert C_{xy} \rvert < 2$; S = 512
			10	when $\lvert C_{xy} \rvert < 1$; S = 1024
			11	undefined

Table 31. Offset input registers (address 81h to 86h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
81h	MAT_OI1_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	OFFSET_IN1[10:8]	W	000*	**offset input 1:** compensates the brightness value for the G/Y channel[1]
82h	MAT_OI1_LSB	7 to 0	OFFSET_IN1[7:0]	W	00h*	
83h	MAT_OI2_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	OFFSET_IN2[10:8]	W	110*	**offset input 2:** compensates the brightness value for the R/C_R channel[1]
84h	MAT_OI2_LSB	7 to 0	OFFSET_IN2[7:0]	W	00h*	
85h	MAT_OI3_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	OFFSET_IN3[10:8]	W	110*	**offset input 3:** compensates the brightness value for the B/C_B channel[1]
86h	MAT_OI3_LSB	7 to 0	OFFSET_IN3[7:0]	W	00h*	

[1] The value is a signed 11-bit two's complement integer.

Table 32. Coefficient registers (address 87h to 98h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
87h	MAT_P11_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	P11[10:8]	W	010*	**coefficient (1, 1):** coefficient from the G/Y channel to the G/Y channel[1]
88h	MAT_P11_LSB	7 to 0	P11[7:0]	W	00h*	
89h	MAT_P12_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	P12[10:8]	W	110*	**coefficient (1, 2):** coefficient from the R/C_R channel to the G/Y channel[1]
8Ah	MAT_P12_LSB	7 to 0	P12[7:0]	W	92h*	
8Bh	MAT_P13_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	P13[10:8]	W	111*	**coefficient (1, 3):** coefficient from the B/C_B channel to the G/Y channel[1]
8Ch	MAT_P13_LSB	7 to 0	P13[7:0]	W	50h*	
8Dh	MAT_P21_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	P21[10:8]	W	010*	**coefficient (2, 1):** coefficient from the G/Y channel to the R/C_R channel[1]
8Eh	MAT_P21_LSB	7 to 0	P21[7:0]	W	00h*	
8Fh	MAT_P22_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	P22[10:8]	W	010*	**coefficient (2, 2):** coefficient from the R/C_R channel to the R/C_R channel[1]
90h	MAT_P22_LSB	7 to 0	P22[7:0]	W	CEh*	
91h	MAT_P23_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	P23[10:8]	W	000*	**coefficient (2, 3):** coefficient from the B/C_B channel to the R/C_R channel[1]
92h	MAT_P23_LSB	7 to 0	P23[7:0]	W	00h*	
93h	MAT_P31_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	P31[10:8]	W	010*	**coefficient (3, 1):** coefficient from the G/Y channel to the B/C_B channel[1]
94h	MAT_P31_LSB	7 to 0	P31[7:0]	W	00h*	
95h	MAT_P32_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	P32[10:8]	W	000*	**coefficient (3, 2):** coefficient from the R/C_R channel to the B/C_B channel[1]
96h	MAT_P32_LSB	7 to 0	P32[7:0]	W	00h*	
97h	MAT_P33_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	P33[10:8]	W	011*	**coefficient (3, 3):** coefficient from the B/C_B channel to the B/C_B channel[1]
98h	MAT_P33_LSB	7 to 0	P33[7:0]	W	8Ch*	

[1] The value is a signed 11-bit two's complement integer.

Table 33. Offset output registers (address 99h to 9Eh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
99h	MAT_OO1_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	OFFSET_OUT1[10:8]	W	000*	**offset output 1:** new clamp level for the G/Y channel[1]
9Ah	MAT_OO1_LSB	7 to 0	OFFSET_OUT1[7:0]	W	00h*	
9Bh	MAT_OO2_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	OFFSET_OUT2[10:8]	W	000*	**offset output 2:** new clamp level for the R/C_R channel[1]
9Ch	MAT_OO2_LSB	7 to 0	OFFSET_OUT2[7:0]	W	00h*	

Table 33. Offset output registers (address 99h to 9Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
9Dh	MAT_OO3_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	OFFSET_OUT3[10:8]	W	000*	**offset output 3:** new clamp level for the B/C_B channel[1]
9Eh	MAT_OO3_LSB	7 to 0	OFFSET_OUT3[7:0]	W	00h*	

[1] The value is a signed 11-bit two's complement integer.

9.3.5 Video format registers

Table 34. VIDFORMAT register (address A0h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	x	W	000*	undefined
4 to 0	VIDFORMAT[4:0]	W		**video format:** see *EIA/CEA-861B specification*
			0 0000*	640 × 480p at 60 Hz (format 1 (VGA))
			0 0001	720 × 480p at 60 Hz (format 2/3)
			0 0010	1280 × 720p at 60 Hz (format 4)
			0 0011	1920 × 1080i at 60 Hz (format 5)
			0 0100	720 × 480i at 60 Hz (format 6/7)
			0 0101	720 × 240p at 60 Hz (format 8/9)
			0 0110	1920 × 1080p at 60 Hz (format 16)
			0 0111	720 × 576p at 50 Hz (format 17/18)
			0 1000	1280 × 720p at 50 Hz (format 19)
			0 1001	1920 × 1080i at 50 Hz (format 20)
			0 1010	720 × 576i at 50 Hz (format 21/22)
			0 1011	720 × 288p at 50 Hz (format 23/24)
			others	1920 × 1080p at 50 Hz (format 31)

Table 35. REFPIX_xxx, REFLINE_xxx, NPIX_xxx and NLINE_xxx registers (address A1h to A8h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
A1h	REFPIX_MSB	7 to 5	x	W	000*	undefined
		4 to 0	PRESET_PIX[12:8]	W	0 0000*	**preset pixel:** reference pixel preset
A2h	REFPIX_LSB	7 to 0	PRESET_PIX[7:0]	W	01h*	
A3h	REFLINE_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	PRESET_LINE[10:8]	W	000*	**preset line:** reference line preset
A4h	REFLINE_LSB	7 to 0	PRESET_LINE[7:0]	W	01h*	
A5h	NPIX_MSB	7 to 5	x	W	000*	undefined
		4 to 0	NPIX[12:8]	W	0 0000*	**number pixel:** number of pixels per line
A6h	NPIX_LSB	7 to 0	NPIX[7:0]	W	00h*	
A7h	NLINE_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	NLINE[10:8]	W	000*	**number line:** number of lines per frame
A8h	NLINE_LSB	7 to 0	NLINE[7:0]	W	00h*	

Table 36. VS_LINE_STRT_xx, VS_PIX_STRT_xx, VS_LINE_END_xx, VS_PIX_END_xx registers (address A9h to B8h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
A9h	VS_LINE_STRT_1_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	VS_LINE_START_1[10:8]	W	000*	**vertical synchronization line start 1:** vertical synchronization line number for start pulse in field 1
AAh	VS_LINE_STRT_1_LSB	7 to 0	VS_LINE_START_1[7:0]	W	00h*	
ABh	VS_PIX_STRT_1_MSB	7 to 5	x	W	000*	undefined
		4 to 0	VS_PIX_START_1[12:8]	W	0 0000*	**vertical synchronization pixel start 1:** vertical synchronization pixel number for start pulse in field 1
ACh	VS_PIX_STRT_1_LSB	7 to 0	VS_PIX_START_1[7:0]	W	00h*	
ADh	VS_LINE_END_1_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	VS_LINE_END_1[10:8]	W	000*	**vertical synchronization line end 1:** vertical synchronization line number for end pulse in field 1
AEh	VS_LINE_END_1_LSB	7 to 0	VS_LINE_END_1[7:0]	W	00h*	
AFh	VS_PIX_END_1_MSB	7 to 5	x	W	000*	undefined
		4 to 0	VS_PIX_END_1[12:8]	W	0 0000*	**vertical synchronization pixel end 1:** vertical synchronization pixel number for end pulse in field 1
B0h	VS_PIX_END_1_LSB	7 to 0	VS_PIX_END_1[7:0]	W	00h*	
B1h	VS_LINE_STRT_2_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	VS_LINE_START_2[10:8]	W	000*	**vertical synchronization line start 2:** vertical synchronization line number for start pulse in field 2
B2h	VS_LINE_STRT_2_LSB	7 to 0	VS_LINE_START_2[7:0]	W	00h*	
B3h	VS_PIX_STRT_2_MSB	7 to 5	x	W	000*	undefined
		4 to 0	VS_PIX_START_2[12:8]	W	0 0000*	**vertical synchronization pixel start 2:** vertical synchronization pixel number for start pulse in field 2
B4h	VS_PIX_STRT_2_LSB	7 to 0	VS_PIX_START_2[7:0]	W	00h*	
B5h	VS_LINE_END_2_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	VS_LINE_END_2[10:8]	W	000*	**vertical synchronization line end 2:** vertical synchronization line number for end pulse in field 2
B6h	VS_LINE_END_2_LSB	7 to 0	VS_LINE_END_2[7:0]	W	00h*	
B7h	VS_PIX_END_2_MSB	7 to 5	x	W	000*	undefined
		4 to 0	VS_PIX_END_2[12:8]	W	0 0000*	**vertical synchronization pixel end 2:** vertical synchronization pixel number for end pulse in field 2
B8h	VS_PIX_END_2_LSB	7 to 0	VS_PIX_END_2[7:0]	W	00h*	

Table 37. HS_PIX_xx registers (address B9h to BCh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
B9h	HS_PIX_START_MSB	7 to 5	x	W	000*	undefined
		4 to 0	HS_PIX_START[12:8]	W	0 0000*	horizontal synchronization pixel number for start pulse in field 1
BAh	HS_PIX_START_LSB	7 to 0	HS_PIX_START[7:0]	W	00h*	
BBh	HS_PIX_STOP_MSB	7 to 5	x	W	000*	undefined
		4 to 0	HS_PIX_END[12:8]	W	0 0000*	horizontal synchronization pixel number for end pulse in field 2
BCh	HS_PIX_STOP_LSB	7 to 0	HS_PIX_END[7:0]	W	00h*	

Table 38. VWIN_START_xx and VWIN_END_xx registers (address BDh and C4h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
BDh	VWIN_START_1_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	VWIN_START_1[10:8]	W	000*	**vertical window start 1:** vertical window line number for start pulse in field 1
BEh	VWIN_START_1_LSB	7 to 0	VWIN_START_1[7:0]	W	00h*	
BFh	VWIN_END_1_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	VWIN_END_1[10:8]	W	000*	**vertical window end 1:** vertical window line number for end pulse in field 1
C0h	VWIN_END_1_LSB	7 to 0	VWIN_END_1[7:0]	W	00h*	
C1h	VWIN_START_2_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	VWIN_START_2[10:8]	W	000*	**vertical window start 2:** vertical window line number for start pulse in field 2
C2h	VWIN_START_2_LSB	7 to 0	VWIN_START_2[7:0]	W	00h*	
C3h	VWIN_END_2_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	VWIN_END_2[10:8]	W	000*	**vertical window end 2:** vertical window line number for end pulse in field 2
C4h	VWIN_END_2_LSB	7 to 0	VWIN_END_2[7:0]	W	00h*	

Table 39. DE_xxx registers (address C5h to C8h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
C5h	DE_START_MSB	7 to 5	x	W	000*	undefined
		4 to 0	DE_START[12:8]	W	0 0000*	**data enable start:** data enable pixel number for start pulse in field 1
C6h	DE_START_LSB	7 to 0	DE_START[7:0]	W	00h*	
C7h	DE_STOP_MSB	7 to 5	x	W	000*	undefined
		4 to 0	DE_END[12:8]	W	0 0000*	**data enable end:** data enable pixel number for end pulse in field 2
C8h	DE_STOP_LSB	7 to 0	DE_END[7:0]	W	00h*	

Table 40. COLBAR_WIDTH register (address C9h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	CBW[7:0]	W	00h*	**color bar width**

Table 41. TBG_CNTRL_0 register (address CAh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	SYNC_ONCE	W		**sync once**
			0*	line/pixel counters are synchronized each frame
			1	line/pixel counters are synchronized only once
6	SYNC_MTHD	W		**sync method**
			0*	synchronization is based on combination of v and h
			1	synchronization is based on combination of v and x (de)
5	FRAME_DIS	W		**frame disable:** synchronized by linecnt = 1 AND pixelcnt = 1
			0*	enable video frames
			1	disable video frames
4 to 0	x	W	0 0000*	undefined

Table 42. TBG_CNTRL_1 register (address CBh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	x	W	0*	undefined
6	DWIN_DIS	W		**data island window disable**
			0*	data island window active
			1	data island window disabled
5	VHX_EXT[2]	W		**vhx_ext 2:** bit 2
			0*	vs = vs_tbg (internal)
			1	vs = v_vip (external)
4	VHX_EXT[1]	W		**vhx_ext 1:** bit 1
			0*	hs = hs_tbg (internal)
			1	hs = h_vip (external)
3	VHX_EXT[0]	W		**vhx_ext 0:** bit 0
			0*	de = de_tbg (internal)
			1	de = x_vip (external)
2	VH_TGL[2]	W		**vh_tgl 2:** bit 2
			0*	vs/hs-polarity is determined by vidformat_table
			1	vs/hs-polarity depends on VH_TGL[1:0]
1	VH_TGL[1]	W		**vh_tgl 1:** bit 1
			0*	no specific action
			1	toggle vs (only when VH_TGL[2] = 1)
0	VH_TGL[0]	W		**vh_tgl 0:** bit 0
			0*	no specific action
			1	toggle hs (only when VH_TGL[2] = 1)

Table 43. OFFSET registers (address CCh to CFh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
CCh	VBL_OFFSET_START	7 to 0	VBLOFF_START[7:0]	W	00h*	**vertical blanking offset start:** vertical blanking offset at start active window
CDh	VBL_OFFSET_END	7 to 0	VBLOFF_END[7:0]	W	00h*	**vertical blanking offset end:** vertical blanking offset at end active window
CEh	HBL_OFFSET_START	7 to 0	HBLOFF_START[7:0]	W	00h*	**horizontal blanking offset start:** horizontal blanking offset at start active window
CFh	HBL_OFFSET_END	7 to 0	HBLOFF_END[7:0]	W	00h*	**horizontal blanking offset end:** horizontal blanking offset at end active window

Table 44. DWIN_xx_DE registers (address D0h and D1h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
D0h	DWIN_RE_DE	7 to 0	DWIN_RE_DE[7:0]	W	11h*	**data window rising edge data enable:** data island window rising edge offset with respect to data enable
D1h	DWIN_FE_DE	7 to 0	DWIN_FE_DE[7:0]	W	7Ah*	**data window falling edge data enable:** data island window falling edge offset with respect to data enable

9.3.6 HDMI video formatter control registers

Table 45. HVF_CNTRL_0 register (address E4h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	SM	W		**service mode**
			0*	no specific action
			1	service mode (color bar inserted in video path)
6	RWB	W		**red, white, blue**
			0*	4-bar color bar (Red - White - Blue - Black)
			1	8-bar color bar (White - Yellow - Magenta - Red - Cyan - Green - Blue - Black)
5 to 4	x	W	00*	undefined
3 to 2	PREFIL[1:0]	W		**prefilter**
			00*	no prefilter
			01	[1 2 1]
			10	[–1 0 9 16 9 0 –1]
			11	27 taps ITU601-compliant halfband filter

Table 45. HVF_CNTRL_0 register (address E4h) bit description *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
1 to 0	INTPOL[1:0]	W		**interpolation**
			00*	bypass (from 4 : 4 : 4 to 4 : 4 : 4)
			01	intpol_by_2 (from 4 : 2 : 2 to 4 : 4 : 4); copy sample
			10	intpol_by_2 (from 4 : 2 : 2 to 4 : 4 : 4); linear interpolation ([1 2 1] / 2 filter)
			11	undefined

Table 46. HVF_CNTRL_1 register (address E5h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	x	W	0*	undefined
6	SEMI_PLANAR	W		**semi-planar**
			0	4 : 4 : 4 at the input of the vrf-module
			1	4 : 2 : 2 at the input of the vrf-module
5 to 4	PAD[1:0]	W		**pad**
			00*	12-bit data path
			01	8-bit data path; 4 LSBs set to 0000
			10	10-bit data path; 2 LSBs set to 00
			11	10-bit data path; 2 LSBs set to 00
3 to 2	VQR[1:0]	W		**video quantization range**
			00*	full-scale
			01	RGB/YUV (max. 235 to min. 16)
			10	Y (max. 235 to min. 16); U (max. 240 to min. 16); V (max. 240 to min. 16)
			11	Y (max. 235 to min. 16); U (max. 240 to min. 16); V (max. 240 to min. 16)
1	YUVBLK	W		**YUV blank**
			0*	UV blank level = 16
			1	UV blank level = 0
0	FOR	W		**formatter**
			0*	transparent formatter (4 : 4 : 4 or 4 : 2 : 2 unprocessed)
			1	4 : 2 : 2 output format (4 : 4 : 4 to 4 : 2 : 2 conversion active)

9.3.7 Timer control registers

Table 47. Timer control registers (address E8h to EAh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
E8h	TIMER_H	7	IM_CLKSEL	W		**im timer clock select**
					0	ddc_master clocked by hdmi_clk / (NDIV_IM[3:0] + 1)
					1	ddc_master clocked by cclk / 3 (typically 10 MHz)
		6	WD_CLKSEL	W		**watchdog timer clock select**
					0	wd_timer clocked by hdmi_clk / (NDIV_PF[7:0] + 1)
					1	wd_timer clocked by cclk / 32
		5 to 2	x	W	0000*	undefined
		1 to 0	TIM_H[1:0]	W		**timer control register height**
					00	tim[17:16] = '00'
					01*	tim[17:16] = '01'
					10	tim[17:16] = '10'
					00	tim[17:16] = '11'
E9h	TIMER_M	7 to 0	TIM_M[7:0]	W		**timer control register medium**
					C2h*	tim[15:8] = TIM_M[7:0]
EAh	TIMER_L	7 to 0	TIM_L[7:0]	W		**timer control register low**
					40h*	tim[7:0] = TIM_L[7:0]

9.3.8 NDIV register

Table 48. NDIV_xxx registers (address EEh and EFh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
EEh	NDIV_IM	7 to 4	x	W	0000*	undefined
		3 to 0	NDIV_IM[3:0]	W		**N divisor DDC-bus master**
					0011*	N divisor to set clock period for DDC-bus master
EFh	NDIV_PF	7 to 0	NDIV_PF[7:0]	W		**N divisor pixel frequency**
					1Bh*	N divisor to set clock period for timers (equals pixel frequency)

9.3.9 Control registers

Table 49. Control registers (address F0h to F2h, F9h, FDh and FEh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
F0h	RPT_CNTRL	7 to 4	x	W	0000*	undefined
		3 to 0	REPEAT[3:0]	W	0000*	**repeat:** repeater control
F1h	LEAD_OFF	7 to 4	x	W	0000*	undefined
		3 to 0	LEAD_OFFSET[3:0]	W	0010*	**leading offset:** leading offset for dwin (in case rpt > 1)

Table 49. Control registers (address F0h to F2h, F9h, FDh and FEh) bit description *...continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
F2h	TRAIL_OFF	7 to 4	x	W	0000*	undefined
		3 to 0	TRAIL_OFFSET[3:0]	W	0010*	**trailing offset:** trailing offset for dwin (in case rpt > 1)
F9h	GHOST_XADDR	7 to 1	GHOST_XADDR[6:0]	W	0110 000*	**ghost extended address**
		0	A0_ZERO	W	0*	-
FDh	AIP_CLKSEL	7 to 5	x	W	000*	undefined
		4 to 3	SEL_AIP[1:0]	W		**selection audio input**
					00*	S/PDIF
					01	I^2S-bus
					1X	for internal use
		2	SEL_POL_CLK	W	0*	**select polarity clock:** for internal use
		1 to 0	SEL_FS[1:0]	W		**select fs:** CTS reference
					00*	aclk
					01	mclk
					1X	fs_64 (S/PDIF)
FEh	GHOST_ADDR	7 to 1	GHOST_ADDR[6:0]	W	1010 000*	**ghost address**
		0	GHOST_DIS	W	1*	-

9.3.10 Current page address register

Table 50. CURPAGE_ADR register (address FFh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	CURPAGE_ADR[7:0]	W	00h*	**current page address:** selects the current memory page

9.4 Scaler page register definitions

The current page address for the Scaler page is 01h.

The configuration of the registers for this page is given in Table 51.

Table 51. I²C-bus registers of memory page 01h[1]

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
SC_VIDFORMAT	00h	W	LUT_SEL[1:0]		VID_FORMAT_O[2:0]			VID_FORMAT_I[2:0]			0000 0000
SC_CNTRL	01h	W	x	x	x	x	IL_OUT_ON	PHASES_V	VS_ON	DEIL_ON	0000 0000
SC_DELTA_PHASE_V	02h	W	x	DELTA_PHASE_V[6:0]							0001 1110
SC_DELTA_PHASE_H	03h	W	x	x	x	DELTA_PHASE_H[4:0]					0001 0000
SC_START_PHASE_H	04h	W	x	x	x	x	START_PHASE_H[3:0]				0000 0000
SC_NPIX_IN_LSB	05h	W	NPIX_IN[7:0]								1101 0000
SC_NPIX_IN_MSB	06h	W	x	x	x	x	x	x	NPIX_IN[9:8]		0000 0010
SC_NPIX_OUT_LSB	07h	W	NPIX_OUT[7:0]								1101 0000
SC_NPIX_OUT_MSB	08h	W	x	x	x	x	x	NPIX_OUT[10:8]			0000 0010
SC_NLINE_IN_LSB	09h	W	NLINE_IN[7:0]								0100 0000
SC_NLINE_IN_MSB	0Ah	W	x	x	x	x	x	x	NLINE_IN[9:8]		0000 0010
SC_NLINE_OUT_LSB	0Bh	W	NLINE_OUT[7:0]								0100 0000
SC_NLINE_OUT_MSB	0Ch	W	x	x	x	x	x	x	NLINE_OUT[9:8]		0000 0010
SC_NLINE_SKIP	0Dh	W	x	x	x	x	x	NLINE_SKIP[2:0]			0000 0000
SC_SAMPLE_BUFFILL	0Eh	R	SAMPLE_BUFFILL_COMMAND[7:0]								XXXX XXXX
SC_MAX_BUFFILL_P_0	0Fh	R	MAX_BUFFILL_P[7:0]								XXXX XXXX
SC_MAX_BUFFILL_P_1	10h	R	x	x	x	x	MAX_BUFFILL_P[11:8]				XXXX XXXX
SC_MAX_BUFFILL_D_0	11h	R	MAX_BUFFILL_D[7:0]								XXXX XXXX
SC_MAX_BUFFILL_D_1	12h	R	x	x	x	x	MAX_BUFFILL_D[11:8]				XXXX XXXX
SC_SAMPLE_FIFOFILL	13h	R	SAMPLE_FIFOFILL_COMMAND[7:0]								XXXX XXXX
SC_MAX_FIFOFILL_PI	14h	R	x	x	x	MAX_FIFOFILL_PI[4:0]					XXXX XXXX
SC_MIN_FIFOFILL_PO1	15h	R	x	x	x	MIN_FIFOFILL_PO1[4:0]					XXXX XXXX
SC_MIN_FIFOFILL_PO2	16h	R	x	x	x	MIN_FIFOFILL_PO2[4:0]					XXXX XXXX
SC_MIN_FIFOFILL_PO3	17h	R	x	x	x	MIN_FIFOFILL_PO3[4:0]					XXXX XXXX
SC_MIN_FIFOFILL_PO4	18h	R	x	x	x	MIN_FIFOFILL_PO4[4:0]					XXXX XXXX
SC_MAX_FIFOFILL_DI	19h	R	x	x	x	MAX_FIFOFILL_DI[4:0]					XXXX XXXX
SC_MAX_FIFOFILL_DO	1Ah	R	x	x	x	MAX_FIFOFILL_DO[4:0]					XXXX XXXX
SC_VS_LUT_0	1Bh	W	VS_LUT0[7:0]								XXXX XXXX
SC_VS_LUT_1	1Ch	W	VS_LUT1[7:0]								XXXX XXXX
SC_VS_LUT_2	1Dh	W	VS_LUT2[7:0]								XXXX XXXX
SC_VS_LUT_3	1Eh	W	VS_LUT3[7:0]								XXXX XXXX

Table 51. I²C-bus registers of memory page 01h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
SC_VS_LUT_4	1Fh	W	VS_LUT4[7:0]								XXXX XXXX
SC_VS_LUT_5	20h	W	VS_LUT5[7:0]								XXXX XXXX
SC_VS_LUT_6	21h	W	VS_LUT6[7:0]								XXXX XXXX
SC_VS_LUT_7	22h	W	VS_LUT7[7:0]								XXXX XXXX
SC_VS_LUT_8	23h	W	VS_LUT8[7:0]								XXXX XXXX
SC_VS_LUT_9	24h	W	VS_LUT9[7:0]								XXXX XXXX
SC_VS_LUT_10	25h	W	VS_LUT10[7:0]								XXXX XXXX
SC_VS_LUT_11	26h	W	VS_LUT11[7:0]								XXXX XXXX
SC_VS_LUT_12	27h	W	VS_LUT12[7:0]								XXXX XXXX
SC_VS_LUT_13	28h	W	VS_LUT13[7:0]								XXXX XXXX
SC_VS_LUT_14	29h	W	VS_LUT14[7:0]								XXXX XXXX
SC_VS_LUT_15	2Ah	W	VS_LUT15[7:0]								XXXX XXXX
SC_VS_LUT_16	2Bh	W	VS_LUT16[7:0]								XXXX XXXX
SC_VS_LUT_17	2Ch	W	VS_LUT17[7:0]								XXXX XXXX
SC_VS_LUT_18	2Dh	W	VS_LUT18[7:0]								XXXX XXXX
SC_VS_LUT_19	2Eh	W	VS_LUT19[7:0]								XXXX XXXX
SC_VS_LUT_20	2Fh	W	VS_LUT20[7:0]								XXXX XXXX
SC_VS_LUT_21	30h	W	VS_LUT21[7:0]								XXXX XXXX
SC_VS_LUT_22	31h	W	VS_LUT22[7:0]								XXXX XXXX
SC_VS_LUT_23	32h	W	VS_LUT23[7:0]								XXXX XXXX
SC_VS_LUT_24	33h	W	VS_LUT24[7:0]								XXXX XXXX
SC_VS_LUT_25	34h	W	VS_LUT25[7:0]								XXXX XXXX
SC_VS_LUT_26	35h	W	VS_LUT26[7:0]								XXXX XXXX
SC_VS_LUT_27	36h	W	VS_LUT27[7:0]								XXXX XXXX
SC_VS_LUT_28	37h	W	VS_LUT28[7:0]								XXXX XXXX
SC_VS_LUT_29	38h	W	VS_LUT29[7:0]								XXXX XXXX
SC_VS_LUT_30	39h	W	VS_LUT30[7:0]								XXXX XXXX
SC_VS_LUT_31	3Ah	W	VS_LUT31[7:0]								XXXX XXXX
SC_VS_LUT_32	3Bh	W	VS_LUT32[7:0]								XXXX XXXX
SC_VS_LUT_33	3Ch	W	VS_LUT33[7:0]								XXXX XXXX
SC_VS_LUT_34	3Dh	W	VS_LUT34[7:0]								XXXX XXXX
SC_VS_LUT_35	3Eh	W	VS_LUT35[7:0]								XXXX XXXX

Table 51. I²C-bus registers of memory page 01h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
SC_VS_LUT_36	3Fh	W	VS_LUT36[7:0]								XXXX XXXX
SC_VS_LUT_37	40h	W	VS_LUT37[7:0]								XXXX XXXX
SC_VS_LUT_38	41h	W	VS_LUT38[7:0]								XXXX XXXX
SC_VS_LUT_39	42h	W	VS_LUT39[7:0]								XXXX XXXX
SC_VS_LUT_40	43h	W	VS_LUT40[7:0]								XXXX XXXX
SC_VS_LUT_41	44h	W	VS_LUT41[7:0]								XXXX XXXX
SC_VS_LUT_42	45h	W	VS_LUT42[7:0]								XXXX XXXX
SC_VS_LUT_43	46h	W	VS_LUT43[7:0]								XXXX XXXX
SC_VS_LUT_44	47h	W	VS_LUT44[7:0]								XXXX XXXX
Not used	48h	-	-								0000 0000
:	:	:	:								:
Not used	9Fh	-	-								0000 0000
VIDFORMAT	A0h	W	x	x	x	x	x	VIDFORMAT[2:0]			0000 0000
REFPIX_MSB	A1h	W	x	x	x	x	x	x	PRESET_PIX[9:8]		0000 0000
REFPIX_LSB	A2h	W	PRESET_PIX[7:0]								0000 0001
REFLINE_MSB	A3h	W	x	x	x	x	x	x	PRESET_LINE[9:8]		0000 0000
REFLINE_LSB	A4h	W	PRESET_LINE[7:0]								0000 0001
NPIX_MSB	A5h	W	x	x	x	x	x	x	NPIX[9:8]		0000 0000
NPIX_LSB	A6h	W	NPIX[7:0]								0000 0000
NLINE_MSB	A7h	W	x	x	x	x	x	x	NLINE[9:8]		0000 0000
NLINE_LSB	A8h	W	NLINE[7:0]								0000 0000
Not used	A9h	-	-								0000 0000
:	:	:	:								:
Not used	BCh	-	-								0000 0000
VWIN_START_1_MSB	BDh	W	x	x	x	x	x	x	VWIN_START_1[9:8]		0000 0000
VWIN_START_1_LSB	BEh	W	VWIN_START_1[7:0]								0000 0000
VWIN_END_1_MSB	BFh	W	x	x	x	x	x	x	VWIN_END_1[9:8]		0000 0000
VWIN_END_1_LSB	C0h	W	VWIN_END_1[7:0]								0000 0000
VWIN_START_2_MSB	C1h	W	x	x	x	x	x	x	VWIN_START_2[9:8]		0000 0000
VWIN_START_2_LSB	C2h	W	VWIN_START_2[7:0]								0000 0000
VWIN_END_2_MSB	C3h	W	x	x	x	x	x	x	VWIN_END_2[9:8]		0000 0000
VWIN_END_2_LSB	C4h	W	VWIN_END_2[7:0]								0000 0000

Table 51. I²C-bus registers of memory page 01h[1] …continued

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
DE_START_MSB	C5h	W	x	x	x	x	x	x	DE_START[9:8]		0000 0000
DE_START_LSB	C6h	W	DE_START[7:0]								0000 0000
DE_STOP_MSB	C7h	W	x	x	x	x	x	x	DE_END[9:8]		0000 0000
DE_STOP_LSB	C8h	W	DE_END[7:0]								0000 0000
Not used	C9h	-	-	-	-	-	-	-	-	-	0000 0000
TBG_CNTRL_0	CAh	W	SYNC_ ONCE	SYNC_ MTHD	FRAME_ DIS	x	TOP_EXT	DE_EXT	TOP_SEL	TOP_TGL	0000 0000
Not used	CBh	-	-								0000 0000
:	:	:	:								:
Not used	FEh	-	-								0000 0000
CURPAGE_ADR	FFh	W	CURPAGE_ADR[7:0]								0000 0000

[1] R: reading register
W: writing register
x: bit must be set to default value for proper operation
-: not used

9.4.1 Scaler control registers

Table 52. SC_VIDFORMAT register (address 00h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 and 6	LUT_SEL[1:0]	W		**look-up table select**
			00*	default coefficient set #1 (video)
			01	default coefficient set #2 (enhanced sharpness)
			1X	coefficient set as programmed via I^2C-bus
5 to 3	VID_FORMAT_O[2:0]	W		**video format output**
			000*	480p 60 Hz
			001	576p 50 Hz
			010	720p 50 Hz/60 Hz
			011	1080i 50 Hz/60 Hz
			1XX	customized format
2 to 0	VID_FORMAT_I[2:0]	W		**video format input**
			000*	480i 60 Hz
			001	576i 50 Hz
			010	480p 60 Hz
			011	576p 50 Hz
			1XX	customized format

Table 53. SC_CNTRL register (address 01h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 4	x	W	0000*	undefined
3	IL_OUT_ON	W		**interlaced output on**
			0*	internal line phase toggle is ignored
			1	interlaced output; output lines depend on internal line phase toggle
2	PHASES_V	W		**vertical phases**
			0*	90 vertical phases
			1	54 vertical phases
1	VS_ON	W		**vertical scaler on**
			0*	vertical scaler off
			1	vertical scaler on
0	DEIL_ON	W		**deinterlacer on**
			0*	deinterlacer off
			1	deinterlacer on

Table 54. SC_x_PHASE_x registers (address 02h to 04h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
02h	SC_DELTA_PHASE_V	7	x	W	0*	undefined
		6 to 0	DELTA_PHASE_V[6:0]	W	001 1110*	**delta phase vertical**
03h	SC_DELTA_PHASE_H	7 to 5	x	W	000*	undefined
		4 to 0	DELTA_PHASE_H[4:0]	W	1 0000*	**delta phase horizontal**
04h	SC_START_PHASE_H	7 to 4	x	W	0000*	undefined
		3 to 0	START_PHASE_H[3:0]	W	0000*	**start phase horizontal**

Table 55. SC_NPIX_xx registers (address 05h to 08h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
06h	SC_NPIX_IN_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	NPIX_IN[9:8]	W	10*	**number of input pixels**
05h	SC_NPIX_IN_LSB	7 to 0	NPIX_IN[7:0]	W	D0h*	
08h	SC_NPIX_OUT_MSB	7 to 3	x	W	0000 0*	undefined
		2 to 0	NPIX_OUT[10:8]	W	010*	**number of output pixels**
07h	SC_NPIX_OUT_LSB	7 to 0	NPIX_OUT[7:0]	W	D0h*	

Table 56. SC_NLINE_xx registers (address 09h to 0Dh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	SC_NLINE_IN_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	NLINE_IN[9:8]	W	10*	**number of input lines**
09h	SC_NLINE_IN_LSB	7 to 0	NLINE_IN[7:0]	W	40h*	
0Ch	SC_NLINE_OUT_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	NLINE_OUT[9:8]	W	10*	**number of output lines**
0Bh	SC_NLINE_OUT_LSB	7 to 0	NLINE_OUT[7:0]	W	40h*	
0Dh	SC_NLINE_SKIP	7 to 3	x	W	0000 0*	undefined
		2 to 0	NLINE_SKIP[2:0]	W	000*	**number of output lines skipped**: by vertical scaler

Table 57. SC_x_BUFFILL_xx registers (address 0Eh to 12h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
0Eh	SC_SAMPLE_BUFFILL	7 to 0	SAMPLE_BUFFILL_COMMAND[7:0]	R	-	**sample buffer filling command:** when this address is read the BUFFILL values are sampled
10h	SC_MAX_BUFFILL_P_1	7 to 4	x	R	-	undefined
		3 to 0	MAX_BUFFILL_P[11:8]	R	-	**max buffer filling primary:** filling primary video buffer
0Fh	SC_MAX_BUFFILL_P_0	7 to 0	MAX_BUFFILL_P[7:0]	R	-	

Table 57. SC_x_BUFFILL_xx registers (address 0Eh to 12h) bit description *...continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
12h	SC_MAX_BUFFILL_D_1	7 to 4	x	R	-	undefined
		3 to 0	MAX_BUFFILL_D[11:8]	R	-	**max buffer filling deinterlaced**: filling video deinterlaced buffer
11h	SC_MAX_BUFFILL_D_0	7 to 0	MAX_BUFFILL_D[7:0]	R	-	

Table 58. SC_xx_FIFOFILL_xx registers (address 13h to 1Ah) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
13h	SC_SAMPLE_FIFOFILL	7 to 0	SAMPLE_FIFOFILL_COMMAND[7:0]	R	-	**sample FIFO filling command:** when this address is read the FIFOFILL values are sampled
14h	SC_MAX_FIFOFILL_PI	7 to 5	x	R	-	undefined
		4 to 0	MAX_FIFOFILL_PI[4:0]	R	-	**max FIFO filling primary input:** filling primary video input FIFO
15h	SC_MIN_FIFOFILL_PO1	7 to 5	x	R	-	undefined
		4 to 0	MIN_FIFOFILL_PO1[4:0]	R	-	**min FIFO filling primary output 1**: filling primary video output FIFO#1
16h	SC_MIN_FIFOFILL_PO2	7 to 5	x	R	-	undefined
		4 to 0	MIN_FIFOFILL_PO2[4:0]	R	-	**min FIFO filling primary output 2**: filling primary video output FIFO#2
17h	SC_MIN_FIFOFILL_PO3	7 to 5	x	R	-	undefined
		4 to 0	MIN_FIFOFILL_PO3[4:0]	R	-	**min FIFO filling primary output 3**: filling primary video output FIFO#3
18h	SC_MIN_FIFOFILL_PO4	7 to 5	x	R	-	undefined
		4 to 0	MIN_FIFOFILL_PO4[4:0]	R	-	**min FIFO filling primary output 4**: filling primary video output FIFO#4
19h	SC_MAX_FIFOFILL_DI	7 to 5	x	R	-	undefined
		4 to 0	MAX_FIFOFILL_DI[4:0]	R	-	**max FIFO filling deinterlaced input**: filling deinterlaced video input FIFO
1Ah	SC_MAX_FIFOFILL_DO	7 to 5	x	R	-	undefined
		4 to 0	MAX_FIFOFILL_DO[4:0]	R	-	**max FIFO filling deinterlaced output**: filling deinterlaced video output FIFO

Table 59. SC_VS_LUT_xx registers (address 1Bh to 47h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
1Bh	SC_VS_LUT_0	7 to 0	VS_LUT0[7:0]	W	-	**vertical scaler LUT 0:** external LUT coefficient[0] for vertical scaler
1Ch	SC_VS_LUT_1	7 to 0	VS_LUT1[7:0]	W	-	**vertical scaler LUT 1:** external LUT coefficient[1] for vertical scaler
1Dh	SC_VS_LUT_2	7 to 0	VS_LUT2[7:0]	W	-	**vertical scaler LUT 2:** external LUT coefficient[2] for vertical scaler
1Eh	SC_VS_LUT_3	7 to 0	VS_LUT3[7:0]	W	-	**vertical scaler LUT 3:** external LUT coefficient[3] for vertical scaler
1Fh	SC_VS_LUT_4	7 to 0	VS_LUT4[7:0]	W	-	**vertical scaler LUT 4:** external LUT coefficient[4] for vertical scaler
20h	SC_VS_LUT_5	7 to 0	VS_LUT5[7:0]	W	-	**vertical scaler LUT 5:** external LUT coefficient[5] for vertical scaler
21h	SC_VS_LUT_6	7 to 0	VS_LUT6[7:0]	W	-	**vertical scaler LUT 6:** external LUT coefficient[6] for vertical scaler
22h	SC_VS_LUT_7	7 to 0	VS_LUT7[7:0]	W	-	**vertical scaler LUT 7:** external LUT coefficient[7] for vertical scaler
23h	SC_VS_LUT_8	7 to 0	VS_LUT8[7:0]	W	-	**vertical scaler LUT 8:** external LUT coefficient[8] for vertical scaler
24h	SC_VS_LUT_9	7 to 0	VS_LUT9[7:0]	W	-	**vertical scaler LUT 9:** external LUT coefficient[9] for vertical scaler
25h	SC_VS_LUT_10	7 to 0	VS_LUT10[7:0]	W	-	**vertical scaler LUT 10:** external LUT coefficient[10] for vertical scaler
26h	SC_VS_LUT_11	7 to 0	VS_LUT11[7:0]	W	-	**vertical scaler LUT 11:** external LUT coefficient[11] for vertical scaler
27h	SC_VS_LUT_12	7 to 0	VS_LUT12[7:0]	W	-	**vertical scaler LUT 12:** external LUT coefficient[12] for vertical scaler
28h	SC_VS_LUT_13	7 to 0	VS_LUT13[7:0]	W	-	**vertical scaler LUT 13:** external LUT coefficient[13] for vertical scaler
29h	SC_VS_LUT_14	7 to 0	VS_LUT14[7:0]	W	-	**vertical scaler LUT 14:** external LUT coefficient[14] for vertical scaler
2Ah	SC_VS_LUT_15	7 to 0	VS_LUT15[7:0]	W	-	**vertical scaler LUT 15:** external LUT coefficient[15] for vertical scaler
2Bh	SC_VS_LUT_16	7 to 0	VS_LUT16[7:0]	W	-	**vertical scaler LUT 16:** external LUT coefficient[16] for vertical scaler
2Ch	SC_VS_LUT_17	7 to 0	VS_LUT17[7:0]	W	-	**vertical scaler LUT 17:** external LUT coefficient[17] for vertical scaler
2Dh	SC_VS_LUT_18	7 to 0	VS_LUT18[7:0]	W	-	**vertical scaler LUT 18:** external LUT coefficient[18] for vertical scaler
2Eh	SC_VS_LUT_19	7 to 0	VS_LUT19[7:0]	W	-	**vertical scaler LUT 19:** external LUT coefficient[19] for vertical scaler
2Fh	SC_VS_LUT_20	7 to 0	VS_LUT20[7:0]	W	-	**vertical scaler LUT 20:** external LUT coefficient[20] for vertical scaler
30h	SC_VS_LUT_21	7 to 0	VS_LUT21[7:0]	W	-	**vertical scaler LUT 21:** external LUT coefficient[21] for vertical scaler
31h	SC_VS_LUT_22	7 to 0	VS_LUT22[7:0]	W	-	**vertical scaler LUT 22:** external LUT coefficient[22] for vertical scaler

Table 59. SC_VS_LUT_xx registers (address 1Bh to 47h) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
32h	SC_VS_LUT_23	7 to 0	VS_LUT23[7:0]	W	-	**vertical scaler LUT 23:** external LUT coefficient[23] for vertical scaler
33h	SC_VS_LUT_24	7 to 0	VS_LUT24[7:0]	W	-	**vertical scaler LUT 24:** external LUT coefficient[24] for vertical scaler
34h	SC_VS_LUT_25	7 to 0	VS_LUT25[7:0]	W	-	**vertical scaler LUT 25:** external LUT coefficient[25] for vertical scaler
35h	SC_VS_LUT_26	7 to 0	VS_LUT26[7:0]	W	-	**vertical scaler LUT 26:** external LUT coefficient[26] for vertical scaler
36h	SC_VS_LUT_27	7 to 0	VS_LUT27[7:0]	W	-	**vertical scaler LUT 27:** external LUT coefficient[27] for vertical scaler
37h	SC_VS_LUT_28	7 to 0	VS_LUT28[7:0]	W	-	**vertical scaler LUT 28:** external LUT coefficient[28] for vertical scaler
38h	SC_VS_LUT_29	7 to 0	VS_LUT29[7:0]	W	-	**vertical scaler LUT 29:** external LUT coefficient[29] for vertical scaler
39h	SC_VS_LUT_30	7 to 0	VS_LUT30[7:0]	W	-	**vertical scaler LUT 30:** external LUT coefficient[30] for vertical scaler
3Ah	SC_VS_LUT_31	7 to 0	VS_LUT31[7:0]	W	-	**vertical scaler LUT 31:** external LUT coefficient[31] for vertical scaler
3Bh	SC_VS_LUT_32	7 to 0	VS_LUT32[7:0]	W	-	**vertical scaler LUT 32:** external LUT coefficient[32] for vertical scaler
3Ch	SC_VS_LUT_33	7 to 0	VS_LUT33[7:0]	W	-	**vertical scaler LUT 33:** external LUT coefficient[33] for vertical scaler
3Dh	SC_VS_LUT_34	7 to 0	VS_LUT34[7:0]	W	-	**vertical scaler LUT 34:** external LUT coefficient[34] for vertical scaler
3Eh	SC_VS_LUT_35	7 to 0	VS_LUT35[7:0]	W	-	**vertical scaler LUT 35:** external LUT coefficient[35] for vertical scaler
3Fh	SC_VS_LUT_36	7 to 0	VS_LUT36[7:0]	W	-	**vertical scaler LUT 36:** external LUT coefficient[36] for vertical scaler
40h	SC_VS_LUT_37	7 to 0	VS_LUT37[7:0]	W	-	**vertical scaler LUT 37:** external LUT coefficient[37] for vertical scaler
41h	SC_VS_LUT_38	7 to 0	VS_LUT38[7:0]	W	-	**vertical scaler LUT 38:** external LUT coefficient[38] for vertical scaler
42h	SC_VS_LUT_39	7 to 0	VS_LUT39[7:0]	W	-	**vertical scaler LUT 39:** external LUT coefficient[39] for vertical scaler
43h	SC_VS_LUT_40	7 to 0	VS_LUT40[7:0]	W	-	**vertical scaler LUT 40:** external LUT coefficient[40] for vertical scaler
44h	SC_VS_LUT_41	7 to 0	VS_LUT41[7:0]	W	-	**vertical scaler LUT 41:** external LUT coefficient[41] for vertical scaler
45h	SC_VS_LUT_42	7 to 0	VS_LUT42[7:0]	W	-	**vertical scaler LUT 42:** external LUT coefficient[42] for vertical scaler
46h	SC_VS_LUT_43	7 to 0	VS_LUT43[7:0]	W	-	**vertical scaler LUT 43:** external LUT coefficient[43] for vertical scaler
47h	SC_VS_LUT_44	7 to 0	VS_LUT44[7:0]	W	-	**vertical scaler LUT 44:** external LUT coefficient[44] for vertical scaler

9.4.2 Scaling input time base generator control registers

Table 60. VIDFORMAT register (address A0h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 3	x	W	0000 0*	undefined
2 to 0	VIDFORMAT[2:0]	W		**video format:** time base generator for scaler input formats
			000*	480i 60 Hz
			001	576i 50 Hz
			010	480p 60 Hz
			011	576p 50 Hz
			1XX	reserved for future use

Table 61. REFPIX_xx, REFLINE_xx, NPIX_xx and NLINE_xx registers (address A1h to A8h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
A1h	REFPIX_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	PRESET_PIX[9:8]	W	00*	**preset pixel:** reference pixel preset
A2h	REFPIX_LSB	7 to 0	PRESET_PIX[7:0]	W	01h*	
A3h	REFLINE_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	PRESET_LINE[9:8]	W	00*	**preset line:** reference line preset
A4h	REFLINE_LSB	7 to 0	PRESET_LINE[7:0]	W	01h*	
A5h	NPIX_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	NPIX[9:8]	W	00*	**number pixel:** number of pixels per line
A6h	NPIX_LSB	7 to 0	NPIX[7:0]	W	00h*	
A7h	NLINE_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	NLINE[9:8]	W	00*	**number line:** number of lines per frame
A8h	NLINE_LSB	7 to 0	NLINE[7:0]	W	00h*	

Table 62. VWIN_START_x_xx and VWIN_END_x_xx registers (address BDh to C4h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
BDh	VWIN_START_1_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	VWIN_START_1[9:8]	W	00*	**vertical window start 1:** vertical window line number for start pulse in field 1
BEh	VWIN_START_1_LSB	7 to 0	VWIN_START_1[7:0]	W	00h*	
BFh	VWIN_END_1_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	VWIN_END_1[9:8]	W	00*	**vertical window end 1**: vertical window line number for end pulse in field 1
C0h	VWIN_END_1_LSB	7 to 0	VWIN_END_1[7:0]	W	00h*	
C1h	VWIN_START_2_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	VWIN_START_2[9:8]	W	00*	**vertical window start 2**: vertical window line number for start pulse in field 2
C2h	VWIN_START_2_LSB	7 to 0	VWIN_START_2[7:0]	W	00h*	

Table 62. VWIN_START_x_xx and VWIN_END_x_xx registers (address BDh to C4h) bit description *...continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
C3h	VWIN_END_2_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	VWIN_END_2[9:8]	W	00*	**vertical window end 2**: vertical window line number for end pulse in field 2
C4h	VWIN_END_2_LSB	7 to 0	VWIN_END_2[7:0]	W	00h*	

Table 63. DE_START_x and DE_STOP_x registers (address C5h to C8h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
C5h	DE_START_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	DE_START[9:8]	W	00*	**data enable start**: data enable pixel number for start pulse in field 1
C6h	DE_START_LSB	7 to 0	DE_START[7:0]	W	00h*	
C7h	DE_STOP_MSB	7 to 2	x	W	0000 00*	undefined
		1 to 0	DE_END[9:8]	W	00*	**data enable end**: data enable pixel number for end pulse in field 2
C8h	DE_STOP_LSB	7 to 0	DE_END[7:0]	W	00h*	

Table 64. TBG_CNTRL_0 register (address CAh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	SYNC_ONCE	W		**sync once**
			0*	line/pixel counters are synchronized each frame
			1	line/pixel counters are synchronized only once
6	SYNC_MTHD	W		**sync method**
			0*	synchronization is based on combination of v and h
			1	synchronization is based on combination of v and x (de)
5	FRAME_DIS	W		**frame disable**: synchronized by linecnt = 1 AND pixelcnt = 1
			0*	enable video frames
			1	disable video frames
4	x	W	0*	undefined
3	TOP_EXT	W		**top external**
			0*	top = top_tbg_sci
			1	top = x_vip (external; fref)
2	DE_EXT	W		**data enable external**
			0*	de = de_tbg_sci (internal)
			1	de = x_vip (external; de)

Table 64. TBG_CNTRL_0 register (address CAh) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
1	TOP_SEL	W		**top select**
			0*	top_tbg_sci = top_tbg_sci (internal; programmed via I^2C-bus)
			1	top_tbg_sci = top_tbg_vrf
0	TOP_TGL	W		**top toggle**
			0*	no specific action
			1	toggle top_tbg_sci

9.4.3 Current page address register

Table 65. CURPAGE_ADR register (address FFh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	CURPAGE_ADR[7:0]	W	00h*	**current page address:** selects the current memory page

9.5 PLL settings page register definitions

The current page address for the PLL settings page is 02h.

The configuration of the registers for this page is given in Table 66.

Table 66. I²C-bus registers of memory page 02h[1]

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
PLL_SERIAL_1	00h	R/W	x	SRL_MAN_IP	SRL_REG_IP[2:0]			SRL_IZ[1:0]		SRL_FDN	0000 0000
PLL_SERIAL_2	01h	R/W	SRL_PR[3:0]				x	x	SRL_NOSC[1:0]		0000 0000
PLL_SERIAL_3	02h	R/W	x	x	x	SRL_PXIN_SEL	x	x	SRL_DE	SRL_CCIR	0000 0000
SERIALIZER	03h	R/W	SRL_PHASE3[3:0]				SRL_PHASE2[3:0]				0000 0000
BUFFER_OUT	04h	R/W	x	x	x	x	SRL_FORCE[1:0]		SRL_CLK[1:0]		0000 0000
PLL_SCG1	05h	R/W	x	x	x	x	x	x	x	SCG_FDN	0000 0001
PLL_SCG2	06h	R/W	BYPASS_SCG	x	x	SELPLLCLKIN	x	x	SCG_NOSC[1:0]		1001 0000
PLL_SCGN1	07h	R/W	SCG_NDIV[7:0]								1111 1010
PLL_SCGN2	08h	R/W	x	x	x	x	x	SCG_NDIV[10:8]			0000 0000
PLL_SCGR1	09h	R/W	SCG_RDIV[7:0]								0101 1011
PLL_SCGR2	0Ah	R/W	x	x	x	x	x	x	x	SCG_RDIV[8]	0000 0000
PLL_DE	0Bh	R/W	BYPASS_PLLDE	x	PLLDE_NOSC[1:0]		x	PLLDE_IZ[1:0]		PLLDE_FDN	1000 0001
CCIR_DIV	0Ch	R/W	x	x	x	x	x	x	x	REFDIV2	0000 0001
VAI_PLL	0Dh	R	x	PLLDE_HVP	PLLSCG_HVP	PLLSRL_HVP	x	PLLDE_LOCK	PLLSCG_LOCK	PLLSRL_LOCK	0000 0000
AUDIO_DIV	0Eh	R/W	x	x	x	x	x	AUDIO_DIV[2:0]			0000 0011
TEST1	0Fh	R/W	x	x	x	TSTSERPHOE	x	x	TST_NOSC	TST_HVP	0000 0000
TEST2	10h	R/W	x	x	x	x	x	x	PWD1V8	DIVTESTOE	0000 0000
SEL_CLK	11h	R/W	x	x	x	x	ENA_SC_CLK	SEL_VRF_CLK[1:0]		SEL_CLK1	0000 0000
Not used	12h	-	-								0000 0000
:	:	:	:								:
Not used	FEh	-	-								0000 0000
CURPAGE_ADR	FFh	W	CURPAGE_ADR[7:0]								0000 0000

[1] R: reading register
W: writing register
x: bit must be set to default value for proper operation
-: not used

9.5.1 PLL serial registers

Table 67. PLL_SERIAL_1 register (address 00h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	x	R/W	0*	undefined
6	SRL_MAN_IP	R/W		**serializer manual current pole**
			0*	automatic setting of output current pole charge pump (ip_auto)
			1	manual setting of output current pole charge pump (ip_manual)
5 to 3	SRL_REG_IP[2:0]	R/W		**serializer current pole:** PLL pole charge pump output current (ip_manual)
			000*	400 nA
			001	200 nA
			010	133 nA
			011	100 nA
			100	80 nA
			101	66 nA
			110	57 nA
			111	50 nA
2 to 1	SRL_IZ[1:0]	R/W		**serializer zero current**: PLL zero charge pump output current
			00*	Iz / 5
			01	Iz / 10
			10	Iz / 15
			11	Iz / 20
0	SRL_FDN	R/W		**serializer fdn**
			0*	normal (PLL loop active)
			1	standby (PLL loop open)

Table 68. PLL_SERIAL_2 register (address 01h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 4	SRL_PR[3:0]	R/W		**serializer pixel repetition:** pixel repetition factor (ip_auto)
			0000*	pr = 1 (ip_auto = 400 nA)
			0001	pr = 2 (ip_auto = 200 nA)
			0010	pr = 3 (ip_auto = 133 nA)
			0011	pr = 4 (ip_auto = 100 nA)
			0100	pr = 5 (ip_auto = 80 nA)
			0101	pr = 6 (ip_auto = 66 nA)
			0110	pr = 7 (ip_auto = 57 nA)
			0111	pr = 8 (ip_auto = 50 nA)
			1000	pr = 9 (ip_auto = 50 nA)
			1001	pr = 10 (ip_auto = 50 nA)
			other	undefined
3 to 2	x	R/W	00*	undefined
1 to 0	SRL_NOSC[1:0]	R/W		**serializer N oscillator**: predivider division factor
			00*	div_by_1; PLL output frequency range = (800 to 1500) Msample/s (Iz = 1.0+)
			01	div_by_2; PLL output frequency range = (400 to 800) Msample/s (Iz = 1.5+)
			10	div_by_4; PLL output frequency range = (200 to 400) Msample/s (Iz = 2.0+)
			11	div_by_4; PLL output frequency range = (200 to 400) Msample/s (Iz = 2.0+)

Table 69. PLL_SERIAL_3 register (address 02h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	x	R/W	000*	undefined
4	SRL_PXIN_SEL	R/W		**serializer pixel input select**
			0*	PXINclko = SCAclko
			1	PXINclko = SCAclko / 2
3 to 2	x	R/W	00*	undefined
1	SRL_DE	R/W		**serializer double edge**: double edge divider in feedback loop
			0*	no division
			1	divide by 2
0	SRL_CCIR	R/W		**serializer CCIR**
			0*	pllsrl_in = pllsrl_refin
			1	pllsrl_in = pllsrl_refin / 2

Table 70. SERIALIZER register (address 03h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 4	SRL_PHASE3[3:0]	R/W	0000*	**serializer phase 3**: phase selection of third storage level of the serializer input
3 to 0	SRL_PHASE2[3:0]	R/W	0000*	**serializer phase 2**: phase selection of second storage level of the serializer input

Table 71. BUFFER_OUT register (address 04h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 4	x	R/W	0000*	undefined
3 to 2	SRL_FORCE[1:0]	R/W		**serializer force**
			00*	TMDS outputs active (normal operation)
			01	TMDS outputs active (normal operation)
			10	TMDS outputs forced '0'
			11	TMDS outputs forced '1'
1 to 0	SRL_CLK[1:0]	R/W		**serializer clock**
			00*	TMDS TXC = TMDSclk (normal operation)
			01	TMDS TXC = SERclk / 2
			10	TMDS TXC = undefined
			11	TMDS TXC = SERclk

Table 72. PLL_SCG1 register (address 05h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 1	x	R/W	0000 000*	undefined
0	SCG_FDN	R/W		**scg fnd**
			0	normal (PLL loop active)
			1*	standby (PLL loop open)

Table 73. PLL_SCG2 register (address 06h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	BYPASS_SCG	R/W		**bypass scg**
			0	SCAclko = scg_nosc predivider output
			1*	SCAclko = pllscg_inref
6 to 5	x	R/W	00*	undefined
4	SELPLLCLKIN	R/W		**select PLL clock input**
			0	pllscg_in = pllsca_inref
			1*	pllscg_in = pllclkin
3 to 2	x	R/W	00*	undefined

Table 73. PLL_SCG2 register (address 06h) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
1 to 0	SCG_NOSC[1:0]	R/W		**scg N oscillator**
			00*	div_by_1; PLL output frequency range = (80 to 150) Msample/s
			01	div_by_2; PLL output frequency range = (40 to 80) Msample/s
			10	div_by_4; PLL output frequency range = (20 to 40) Msample/s
			11	div_by_8; PLL output frequency range = (10 to 20) Msample/s

Table 74. PLL_SCGNx registers (address 07h to 08h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
08h	PLL_SCGN2	7 to 3	x	R/W	0000 0*	undefined
		2 to 0	SCG_NDIV[10:8]	R/W	000*	**scg N divider**: PLL feedback oscillator divider
07h	PLL_SCGN1	7 to 0	SCG_NDIV[7:0]	R/W	FAh*	

Table 75. PLL_SCGRx registers (address 09h to 0Ah) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	PLL_SCGR2	7 to 1	x	R/W	0000 000*	undefined
		0	SCG_RDIV[8]	R/W	0*	**scg R divider**: divider value of the PLL reference input clock
09h	PLL_SCGR1	7 to 0	SCG_RDIV[7:0]	R/W	5Bh*	

Table 76. PLL_DE register (address 0Bh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	BYPASS_PLLDE	R/W		**bypass PLL double edge**
			0	pllde0 = de_nosc predivider output
			1*	pllde0 = pllde_inref
6	x	R/W	0*	undefined
5 to 4	PLLDE_NOSC[1:0]	R/W		**PLL double edge N oscillator**
			00*	div_by_1; PLL output frequency range = (80 to 150) Msample/s
			01	div_by_2; PLL output frequency range = (40 to 80) Msample/s
			10	div_by_4; PLL output frequency range = (20 to 40) Msample/s
			11	div_by_8; PLL output frequency range = (10 to 20) Msample/s
3	x	R/W	0*	undefined

Table 76. PLL_DE register (address 0Bh) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
2 to 1	PLLDE_IZ[1:0]	R/W		**PLL double edge zero current**
			00*	Iz / 5
			01	Iz / 10
			10	Iz / 15
			11	Iz / 20
0	PLLDE_FDN	R/W		**PLL double edge fdn**
			0	normal (PLL loop active)
			1*	standby (PLL loop open)

Table 77. CCIR_DIV register (address 0Ch) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 1	x	R/W	0000 000*	undefined
0	REFDIV2	R/W		**reference divider 2**
			0	pllde_inref = pllclkin
			1*	pllde_inref = pllclkin / 2

Table 78. VAI_PLL register (address 0Dh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	x	R	0*	undefined
6	PLLDE_HVP	R		**PLL DE high voltage protection**
			0*	PLLDE high voltage protection cell output is '0'
			1	PLLDE high voltage protection cell output is '1'
5	PLLSCG_HVP	R		**PLL SCG high voltage protection**
			0*	PLLSCG high voltage protection cell output is '0'
			1	PLLSCG high voltage protection cell output is '1'
4	PLLSRL_HVP	R		**PLL SRL high voltage protection**
			0*	PLLSRL high voltage protection cell output is '0'
			1	PLLSRL high voltage protection cell output is '1'
3	x	R	0*	undefined
2	PLLDE_LOCK	R		**PLL DE locked**
			0*	PLLDE not locked
			1	PLLDE in lock
1	PLLSCG_LOCK	R		**PLL SCG locked**
			0*	PLLSCG not locked
			1	PLLSCG in lock
0	PLLSRL_LOCK	R		**PLL SRL locked**
			0*	PLLSRL not locked
			1	PLLSRL in lock

Table 79. AUDIO_DIV register (address 0Eh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 3	x	R/W	0000 0*	undefined
2 to 0	AUDIO_DIV[2:0]	R/W		**audio divider:** not guaranteed; under reservation (ip_manual)
			000	Audio_Clk_Out = SERclk / 1
			001	Audio_Clk_Out = SERclk / 2
			010	Audio_Clk_Out = SERclk / 4
			011*	Audio_Clk_Out = SERclk / 8
			100	Audio_Clk_Out = SERclk / 16
			101	Audio_Clk_Out = SERclk / 32
			11X	do not use

Table 80. TESTx registers (address 0Fh and 10h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
0Fh	TEST1	7 to 5	x	R/W	000*	undefined
		4	TSTSERPHOE	R/W		**test serializer phoe**
					0*	srl_tst_ph2_o = '0'; srl_tst_ph3_o = '0'
					1	srl_tst_ph2_o = 'active'; srl_tst_ph3_o = 'active'
		3 to 2	x	R/W	00*	undefined
		1	TST_NOSC	R/W		**test N oscillator:** test mode nosc predividers
					0*	normal mode; input nosc predivider = PLL oscillator output
					1	test mode; input nosc predivider = PLL reference input
		0	TST_HVP	R/W		**test high voltage protection:** test high voltage protection cells
					0*	normal PLL mode
					1	test mode; HVP input forced to $V_{DDA(PLL\_3V3)}$
10h	TEST2	7 to 2	x	R/W	0000 00*	undefined
		1	PWD1V8	R/W		**power-down 1.8 V**
					0*	normal operation
					1	sleep mode PLLs
		0	DIVTESTOE	R/W		**divider tests output enable:** enable activity of scaler PLL dividers test outputs
					0*	test outputs = '0'
					1	test outputs = active

Table 81. SEL_CLK register (address 11h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 4	x	R/W	0000*	undefined
3	ENA_SC_CLK	R/W		**enable scaler clocks**
			0*	disable scaler clocks (sc_clk_m, clk1_m)
			1	enable scaler clocks (sc_clk_m, clk1_m)
2 to 1	SEL_VRF_CLK[1:0]	R/W		**select video reformatter clock**
			00*	vrf_clk_m = not tmdsclkpo; sc_clk_m = tmdsclkpo
			01	vrf_clk_m = scaclko_pllscgon; sc_clk_m = not scaclko_pllscgon
			10	vrf_clk_m = scaclko_tmdsclkn; sc_clk_m = not scaclko_tmdsclkn
			11	vrf_clk_m = scaclko_tmdsclkn; sc_clk_m = not scaclko_tmdsclkn
0	SEL_CLK1	R/W		**select clock 1**
			0*	clk1_m = not (plldeo)
			1	clk1_m = plldeo_div2

9.5.2 Current page address register

Table 82. CURPAGE_ADR register (address FFh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	CURPAGE_ADR[7:0]	W	00h*	**current page address:** selects the current memory page

9.6 Information frames and packets page register definitions

The current page address for the Information frames and packets page is 10h.

The configuration of the registers for this page is given in Table 83.

Table 83. I²C-bus registers of memory page 10h[1]

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
Not used	00h	-	-								0000 0000
:	:	:	:								:
Not used	1Fh	-	-								0000 0000
VSP_IF_TYPE	20h	R/W	VSP_IF_TYPE[7:0]								1000 0001
VSP_IF_VERSION	21h	R/W	VSP_IF_VERSION[7:0]								0000 0000
VSP_IF_LENGTH	22h	R/W	x	x	x	VSP_IF_LENGTH[4:0]					0000 0000
VSP_IF_CHECKSUM	23h	R/W	VSP_IF_CHECKSUM[7:0]								0000 0000
VSP_IF_IEEE_LSB	24h	R/W	VSP_IF_IEEE[7:0]								0000 0000
VSP_IF_IEEE_ISB	25h	R/W	VSP_IF_IEEE[15:8]								0000 0000
VSP_IF_IEEE_MSB	26h	R/W	VSP_IF_IEEE[23:16]								0000 0000
VSP_IF_BYTE4	27h	R/W	VSP_IF_PB4[7:0]								0000 0000
VSP_IF_BYTE5	28h	R/W	VSP_IF_PB5[7:0]								0000 0000
VSP_IF_BYTE6	29h	R/W	VSP_IF_PB6[7:0]								0000 0000
VSP_IF_BYTE7	2Ah	R/W	VSP_IF_PB7[7:0]								0000 0000
VSP_IF_BYTE8	2Bh	R/W	VSP_IF_PB8[7:0]								0000 0000
VSP_IF_BYTE9	2Ch	R/W	VSP_IF_PB9[7:0]								0000 0000
VSP_IF_BYTE10	2Dh	R/W	VSP_IF_PB10[7:0]								0000 0000
VSP_IF_BYTE11	2Eh	R/W	VSP_IF_PB11[7:0]								0000 0000
VSP_IF_BYTE12	2Fh	R/W	VSP_IF_PB12[7:0]								0000 0000
VSP_IF_BYTE13	30h	R/W	VSP_IF_PB13[7:0]								0000 0000
VSP_IF_BYTE14	31h	R/W	VSP_IF_PB14[7:0]								0000 0000
VSP_IF_BYTE15	32h	R/W	VSP_IF_PB15[7:0]								0000 0000
VSP_IF_BYTE16	33h	R/W	VSP_IF_PB16[7:0]								0000 0000
VSP_IF_BYTE17	34h	R/W	VSP_IF_PB17[7:0]								0000 0000
VSP_IF_BYTE18	35h	R/W	VSP_IF_PB18[7:0]								0000 0000
VSP_IF_BYTE19	36h	R/W	VSP_IF_PB19[7:0]								0000 0000
VSP_IF_BYTE20	37h	R/W	VSP_IF_PB20[7:0]								0000 0000
VSP_IF_BYTE21	38h	R/W	VSP_IF_PB21[7:0]								0000 0000
VSP_IF_BYTE22	39h	R/W	VSP_IF_PB22[7:0]								0000 0000
VSP_IF_BYTE23	3Ah	R/W	VSP_IF_PB23[7:0]								0000 0000
VSP_IF_BYTE24	3Bh	R/W	VSP_IF_PB24[7:0]								0000 0000
VSP_IF_BYTE25	3Ch	R/W	VSP_IF_PB25[7:0]								0000 0000

Table 83. I²C-bus registers of memory page 10h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
VSP_IF_BYTE26	3Dh	R/W	VSP_IF_PB26[7:0]								0000 0000
VSP_IF_BYTE27	3Eh	R/W	VSP_IF_PB27[7:0]								0000 0000
Not used	3Fh	-	-								0000 0000
AVI_IF_TYPE	40h	R/W	AVI_IF_TYPE[7:0]								1000 0010
AVI_IF_VERSION	41h	R/W	AVI_IF_VERSION[7:0]								0000 0000
AVI_IF_LENGTH	42h	R/W	x	x	x	AVI_IF_LENGTH[4:0]					0000 0000
AVI_IF_CHECKSUM	43h	R/W	AVI_IF_CHECKSUM[7:0]								0000 0000
AVI_IF_BYTE1	44h	R/W	reserved	AVI_IF_Y[1:0]		AVI_IF_A	AVI_IF_B[1:0]		AVI_IF_S[1:0]		0000 0000
AVI_IF_BYTE2	45h	R/W	AVI_IF_C[1:0]		AVI_IF_M[1:0]		AVI_IF_R[3:0]				0000 0000
AVI_IF_BYTE3	46h	R/W	reserved						AVI_IF_SC[1:0]		0000 0000
AVI_IF_BYTE4	47h	R/W	reserved	AVI_IF_VIC[6:0]							0000 0000
AVI_IF_BYTE5	48h	R/W	reserved				AVI_IF_PR[3:0]				0000 0000
AVI_IF_BYTE6	49h	R/W	LINE_E_TP_BAR[7:0]								0000 0000
AVI_IF_BYTE7	4Ah	R/W	LINE_E_TP_BAR[15:8]								0000 0000
AVI_IF_BYTE8	4Bh	R/W	LINE_S_BT_BAR[7:0]								0000 0000
AVI_IF_BYTE9	4Ch	R/W	LINE_S_BT_BAR[15:8]								0000 0000
AVI_IF_BYTE10	4Dh	R/W	PIX_E_LF_BAR[7:0]								0000 0000
AVI_IF_BYTE11	4Eh	R/W	PIX_E_LF_BAR[15:8]								0000 0000
AVI_IF_BYTE12	4Fh	R/W	PIX_S_RG_BAR[7:0]								0000 0000
AVI_IF_BYTE13	50h	R/W	PIX_S_RG_BAR[15:8]								0000 0000
AVI_IF_BYTE14	51h	R/W	AVI_IF_RB14[7:0]								0000 0000
AVI_IF_BYTE15	52h	R/W	AVI_IF_RB15[7:0]								0000 0000
AVI_IF_BYTE16	53h	R/W	AVI_IF_RB16[7:0]								0000 0000
AVI_IF_BYTE17	54h	R/W	AVI_IF_RB17[7:0]								0000 0000
AVI_IF_BYTE18	55h	R/W	AVI_IF_RB18[7:0]								0000 0000
AVI_IF_BYTE19	56h	R/W	AVI_IF_RB19[7:0]								0000 0000
AVI_IF_BYTE20	57h	R/W	AVI_IF_RB20[7:0]								0000 0000
AVI_IF_BYTE21	58h	R/W	AVI_IF_RB21[7:0]								0000 0000
AVI_IF_BYTE22	59h	R/W	AVI_IF_RB22[7:0]								0000 0000
AVI_IF_BYTE23	5Ah	R/W	AVI_IF_RB23[7:0]								0000 0000
AVI_IF_BYTE24	5Bh	R/W	AVI_IF_RB24[7:0]								0000 0000
AVI_IF_BYTE25	5Ch	R/W	AVI_IF_RB25[7:0]								0000 0000

Table 83. I²C-bus registers of memory page 10h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
AVI_IF_BYTE26	5Dh	R/W	AVI_IF_RB26[7:0]								0000 0000
AVI_IF_BYTE27	5Eh	R/W	AVI_IF_RB27[7:0]								0000 0000
Not used	5Fh	-	-								0000 0000
SPD_IF_TYPE	60h	R/W	SPD_IF_TYPE[7:0]								1000 0011
SPD_IF_VERSION	61h	R/W	SPD_IF_VERSION[7:0]								0000 0000
SPD_IF_LENGTH	62h	R/W	x	x	x	SPD_IF_LENGTH[4:0]					0000 0000
SPD_IF_CHECKSUM	63h	R/W	SPD_IF_CHECKSUM[7:0]								0000 0000
SPD_IF_BYTE1	64h	R/W	x	SPD_IF_VN1[6:0]							0000 0000
SPD_IF_BYTE2	65h	R/W	x	SPD_IF_VN2[6:0]							0000 0000
SPD_IF_BYTE3	66h	R/W	x	SPD_IF_VN3[6:0]							0000 0000
SPD_IF_BYTE4	67h	R/W	x	SPD_IF_VN4[6:0]							0000 0000
SPD_IF_BYTE5	68h	R/W	x	SPD_IF_VN5[6:0]							0000 0000
SPD_IF_BYTE6	69h	R/W	x	SPD_IF_VN6[6:0]							0000 0000
SPD_IF_BYTE7	6Ah	R/W	x	SPD_IF_VN7[6:0]							0000 0000
SPD_IF_BYTE8	6Bh	R/W	x	SPD_IF_VN8[6:0]							0000 0000
SPD_IF_BYTE9	6Ch	R/W	x	SPD_IF_PD1[6:0]							0000 0000
SPD_IF_BYTE10	6Dh	R/W	x	SPD_IF_PD2[6:0]							0000 0000
SPD_IF_BYTE11	6Eh	R/W	x	SPD_IF_PD3[6:0]							0000 0000
SPD_IF_BYTE12	6Fh	R/W	x	SPD_IF_PD4[6:0]							0000 0000
SPD_IF_BYTE13	70h	R/W	x	SPD_IF_PD5[6:0]							0000 0000
SPD_IF_BYTE14	71h	R/W	x	SPD_IF_PD6[6:0]							0000 0000
SPD_IF_BYTE15	72h	R/W	x	SPD_IF_PD7[6:0]							0000 0000
SPD_IF_BYTE16	73h	R/W	x	SPD_IF_PD8[6:0]							0000 0000
SPD_IF_BYTE17	74h	R/W	x	SPD_IF_PD9[6:0]							0000 0000
SPD_IF_BYTE18	75h	R/W	x	SPD_IF_PD10[6:0]							0000 0000
SPD_IF_BYTE19	76h	R/W	x	SPD_IF_PD11[6:0]							0000 0000
SPD_IF_BYTE20	77h	R/W	x	SPD_IF_PD12[6:0]							0000 0000
SPD_IF_BYTE21	78h	R/W	x	SPD_IF_PD13[6:0]							0000 0000
SPD_IF_BYTE22	79h	R/W	x	SPD_IF_PD14[6:0]							0000 0000
SPD_IF_BYTE23	7Ah	R/W	x	SPD_IF_PD15[6:0]							0000 0000
SPD_IF_BYTE24	7Bh	R/W	x	SPD_IF_PD16[6:0]							0000 0000
SPD_IF_BYTE25	7Ch	R/W	SPD_IF_SDI[7:0]								0000 0000

Table 83. I²C-bus registers of memory page 10h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
SPD_IF_BYTE26	7Dh	R/W	SPD_IF_BYTE26[7:0]								0000 0000
SPD_IF_BYTE27	7Eh	R/W	SPD_IF_BYTE27[7:0]								0000 0000
Not used	7Fh	-	-								0000 0000
AUD_IF_TYPE	80h	R/W	AUD_IF_TYPE[7:0]								1000 0100
AUD_IF_VERSION	81h	R/W	AUD_IF_VERSION[7:0]								0000 0000
AUD_IF_LENGTH	82h	R/W	x	x	x	AUD_IF_LENGTH[4:0]					0000 0000
AUD_IF_CHECKSUM	83h	R/W	AUD_IF_CHECKSUM[7:0]								0000 0000
AUD_IF_BYTE1	84h	R/W	AUD_IF_CT[3:0]				reserved	AUD_IF_CC[2:0]			0000 0000
AUD_IF_BYTE2	85h	R/W	reserved			AUD_IF_SF[2:0]			AUD_IF_SS[1:0]		0000 0000
AUD_IF_BYTE3	86h	R/W	AUD_IF_BYTE3[7:0]								0000 0000
AUD_IF_BYTE4	87h	R/W	AUD_IF_CA[7:0]								0000 0000
AUD_IF_BYTE5	88h	R/W	AUD_IF_DM_INH	AUD_IF_LSV[3:0]				reserved			0000 0000
AUD_IF_BYTE6	89h	R/W	AUD_IF_BYTE6[7:0]								0000 0000
AUD_IF_BYTE7	8Ah	R/W	AUD_IF_BYTE7[7:0]								0000 0000
AUD_IF_BYTE8	8Bh	R/W	AUD_IF_BYTE8[7:0]								0000 0000
AUD_IF_BYTE9	8Ch	R/W	AUD_IF_BYTE9[7:0]								0000 0000
AUD_IF_BYTE10	8Dh	R/W	AUD_IF_BYTE10[7:0]								0000 0000
AUD_IF_BYTE11	8Eh	R/W	AUD_IF_BYTE11[7:0]								0000 0000
AUD_IF_BYTE12	8Fh	R/W	AUD_IF_BYTE12[7:0]								0000 0000
AUD_IF_BYTE13	90h	R/W	AUD_IF_BYTE13[7:0]								0000 0000
AUD_IF_BYTE14	91h	R/W	AUD_IF_BYTE14[7:0]								0000 0000
AUD_IF_BYTE15	92h	R/W	AUD_IF_BYTE15[7:0]								0000 0000
AUD_IF_BYTE16	93h	R/W	AUD_IF_BYTE16[7:0]								0000 0000
AUD_IF_BYTE17	94h	R/W	AUD_IF_BYTE17[7:0]								0000 0000
AUD_IF_BYTE18	95h	R/W	AUD_IF_BYTE18[7:0]								0000 0000
AUD_IF_BYTE19	96h	R/W	AUD_IF_BYTE19[7:0]								0000 0000
AUD_IF_BYTE20	97h	R/W	AUD_IF_BYTE20[7:0]								0000 0000
AUD_IF_BYTE21	98h	R/W	AUD_IF_BYTE21[7:0]								0000 0000
AUD_IF_BYTE22	99h	R/W	AUD_IF_BYTE22[7:0]								0000 0000
AUD_IF_BYTE23	9Ah	R/W	AUD_IF_BYTE23[7:0]								0000 0000
AUD_IF_BYTE24	9Bh	R/W	AUD_IF_BYTE24[7:0]								0000 0000

Table 83. I²C-bus registers of memory page 10h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
AUD_IF_BYTE25	9Ch	R/W	AUD_IF_BYTE25[7:0]								0000 0000
AUD_IF_BYTE26	9Dh	R/W	AUD_IF_BYTE26[7:0]								0000 0000
AUD_IF_BYTE27	9Eh	R/W	AUD_IF_BYTE27[7:0]								0000 0000
Not used	9Fh	-	-								0000 0000
MPS_IF_TYPE	A0h	R/W	MPS_IF_TYPE[7:0]								1000 0101
MPS_IF_VERSION	A1h	R/W	MPS_IF_VERSION[7:0]								0000 0000
MPS_IF_LENGTH	A2h	R/W	x	x	x	MPS_IF_LENGTH[4:0]					0000 0000
MPS_IF_CHECKSUM	A3h	R/W	MPS_IF_CHECKSUM[7:0]								0000 0000
MPS_IF_BYTE1	A4h	R/W	MPS_IF_MB0[7:0]								0000 0000
MPS_IF_BYTE2	A5h	R/W	MPS_IF_MB1[7:0]								0000 0000
MPS_IF_BYTE3	A6h	R/W	MPS_IF_MB2[7:0]								0000 0000
MPS_IF_BYTE4	A7h	R/W	MPS_IF_MB3[7:0]								0000 0000
MPS_IF_BYTE5	A8h	R/W	reserved			MPS_IF_FR0	reserved		MPS_IF_MF[1:0]		0000 0000
MPS_IF_BYTE6	A9h	R/W	MPS_IF_BYTE6[7:0]								0000 0000
MPS_IF_BYTE7	AAh	R/W	MPS_IF_BYTE7[7:0]								0000 0000
MPS_IF_BYTE8	ABh	R/W	MPS_IF_BYTE8[7:0]								0000 0000
MPS_IF_BYTE9	ACh	R/W	MPS_IF_BYTE9[7:0]								0000 0000
MPS_IF_BYTE10	ADh	R/W	MPS_IF_BYTE10[7:0]								0000 0000
MPS_IF_BYTE11	AEh	R/W	MPS_IF_BYTE11[7:0]								0000 0000
MPS_IF_BYTE12	AFh	R/W	MPS_IF_BYTE12[7:0]								0000 0000
MPS_IF_BYTE13	B0h	R/W	MPS_IF_BYTE13[7:0]								0000 0000
MPS_IF_BYTE14	B1h	R/W	MPS_IF_BYTE14[7:0]								0000 0000
MPS_IF_BYTE15	B2h	R/W	MPS_IF_BYTE15[7:0]								0000 0000
MPS_IF_BYTE16	B3h	R/W	MPS_IF_BYTE16[7:0]								0000 0000
MPS_IF_BYTE17	B4h	R/W	MPS_IF_BYTE17[7:0]								0000 0000
MPS_IF_BYTE18	B5h	R/W	MPS_IF_BYTE18[7:0]								0000 0000
MPS_IF_BYTE19	B6h	R/W	MPS_IF_BYTE19[7:0]								0000 0000
MPS_IF_BYTE20	B7h	R/W	MPS_IF_BYTE20[7:0]								0000 0000
MPS_IF_BYTE21	B8h	R/W	MPS_IF_BYTE21[7:0]								0000 0000
MPS_IF_BYTE22	B9h	R/W	MPS_IF_BYTE22[7:0]								0000 0000
MPS_IF_BYTE23	BAh	R/W	MPS_IF_BYTE23[7:0]								0000 0000

Table 83. I²C-bus registers of memory page 10h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
MPS_IF_BYTE24	BBh	R/W	MPS_IF_BYTE24[7:0]								0000 0000
MPS_IF_BYTE25	BCh	R/W	MPS_IF_BYTE25[7:0]								0000 0000
MPS_IF_BYTE26	BDh	R/W	MPS_IF_BYTE26[7:0]								0000 0000
MPS_IF_BYTE27	BEh	R/W	MPS_IF_BYTE27[7:0]								0000 0000
Not used	BFh	-	-								0000 0000
:	:	:	:								:
Not used	FEh	-	-								0000 0000
CURPAGE_ADR	FFh	W	CURPAGE_ADR[7:0]								0000 0000

[1] R: reading register
W: writing register
x: bit must be set to default value for proper operation
-: not used

9.6.1 Vendor-specific InfoFrame registers

Below is an example of use. Please refer to *EIA/CEA-861B specification* and *HDMI 1.2a specification* for the correct definition of data bytes.

Table 84. VSP_IF_xx registers (address 20h to 3Eh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
20h	VSP_IF_TYPE	7 to 0	VSP_IF_TYPE[7:0]	R/W	81h*	**vendor-specific InfoFrame packet type:** gives the packet type of the vendor-specific InfoFrame packet (80h + InfoFrame type code as per *EIA/CEA-861B*)
21h	VSP_IF_VERSION	7 to 0	VSP_IF_ VERSION[7:0]	R/W	00h*	**vendor-specific InfoFrame version:** gives the version number of the vendor-specific InfoFrame
22h	VSP_IF_LENGTH	7 to 5	x	R/W	000*	reserved (shall be 000)
		4 to 0	VSP_IF_ LENGTH[4:0]	R/W	0 0000*	**vendor-specific InfoFrame length:** gives the number of data bytes for the vendor-specific InfoFrame; this length does not include the checksum
23h	VSP_IF_ CHECKSUM	7 to 0	VSP_IF_ CHECKSUM[7:0]	R/W	00h*	**vendor-specific InfoFrame checksum:** shall be calculated such that a byte-wide sum of all three bytes of the packet header and all valid bytes of the vendor-specific InfoFrame packet contents (determined by InfoFrame length) plus the checksum itself equals 0
24h	VSP_IF_IEEE_LSB	7 to 0	VSP_IF_IEEE[7:0]	R/W	00h*	**vendor-specific InfoFrame IEEE:** 24-bit IEEE registration identifier
25h	VSP_IF_IEEE_ISB	7 to 0	VSP_IF_IEEE[15:8]	R/W	00h*	
26h	VSP_IF_IEEE_MSB	7 to 0	VSP_IF_IEEE[23:16]	R/W	00h*	
						vendor-specific InfoFrame payload byte x: x = 4 to 27
27h	VSP_IF_BYTE4	7 to 0	VSP_IF_PB4[7:0]	R/W	00h*	byte 4
28h	VSP_IF_BYTE5	7 to 0	VSP_IF_PB5[7:0]	R/W	00h*	byte 5
29h	VSP_IF_BYTE6	7 to 0	VSP_IF_PB6[7:0]	R/W	00h*	byte 6
2Ah	VSP_IF_BYTE7	7 to 0	VSP_IF_PB7[7:0]	R/W	00h*	byte 7
2Bh	VSP_IF_BYTE8	7 to 0	VSP_IF_PB8[7:0]	R/W	00h*	byte 8
2Ch	VSP_IF_BYTE9	7 to 0	VSP_IF_PB9[7:0]	R/W	00h*	byte 9
2Dh	VSP_IF_BYTE10	7 to 0	VSP_IF_PB10[7:0]	R/W	00h*	byte 10
2Eh	VSP_IF_BYTE11	7 to 0	VSP_IF_PB11[7:0]	R/W	00h*	byte 11
2Fh	VSP_IF_BYTE12	7 to 0	VSP_IF_PB12[7:0]	R/W	00h*	byte 12
30h	VSP_IF_BYTE13	7 to 0	VSP_IF_PB13[7:0]	R/W	00h*	byte 13
31h	VSP_IF_BYTE14	7 to 0	VSP_IF_PB14[7:0]	R/W	00h*	byte 14
32h	VSP_IF_BYTE15	7 to 0	VSP_IF_PB15[7:0]	R/W	00h*	byte 15
33h	VSP_IF_BYTE16	7 to 0	VSP_IF_PB16[7:0]	R/W	00h*	byte 16
34h	VSP_IF_BYTE17	7 to 0	VSP_IF_PB17[7:0]	R/W	00h*	byte 17
35h	VSP_IF_BYTE18	7 to 0	VSP_IF_PB18[7:0]	R/W	00h*	byte 18
36h	VSP_IF_BYTE19	7 to 0	VSP_IF_PB19[7:0]	R/W	00h*	byte 19

Table 84. VSP_IF_xx registers (address 20h to 3Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
37h	VSP_IF_BYTE20	7 to 0	VSP_IF_PB20[7:0]	R/W	00h*	byte 20
38h	VSP_IF_BYTE21	7 to 0	VSP_IF_PB21[7:0]	R/W	00h*	byte 21
39h	VSP_IF_BYTE22	7 to 0	VSP_IF_PB22[7:0]	R/W	00h*	byte 22
3Ah	VSP_IF_BYTE23	7 to 0	VSP_IF_PB23[7:0]	R/W	00h*	byte 23
3Bh	VSP_IF_BYTE24	7 to 0	VSP_IF_PB24[7:0]	R/W	00h*	byte 24
3Ch	VSP_IF_BYTE25	7 to 0	VSP_IF_PB25[7:0]	R/W	00h*	byte 25
3Dh	VSP_IF_BYTE26	7 to 0	VSP_IF_PB26[7:0]	R/W	00h*	byte 26
3Eh	VSP_IF_BYTE27	7 to 0	VSP_IF_PB27[7:0]	R/W	00h*	byte 27

9.6.2 Auxiliary video information InfoFrame registers

Below is an example of use. Please refer to *EIA/CEA-861B specification* and *HDMI 1.2a specification* for the correct definition of data bytes.

Table 85. AVI_IF_xx registers (address 40h to 5Eh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
40h	AVI_IF_TYPE	7 to 0	AVI_IF_TYPE[7:0]	R/W	82h*	**auxiliary video information InfoFrame packet type:** gives the packet type of the auxiliary video information InfoFrame packet (80h + InfoFrame type code as per *EIA/CEA-861B*)
41h	AVI_IF_VERSION	7 to 0	AVI_IF_VERSION[7:0]	R/W	00h*	**auxiliary video information InfoFrame version:** gives the version number of the auxiliary video information InfoFrame
42h	AVI_IF_LENGTH	7 to 5	x	R/W	000*	reserved (shall be 000)
		4 to 0	AVI_IF_LENGTH[4:0]	R/W	0 0000*	**auxiliary video information InfoFrame length:** gives the number of data bytes for the auxiliary video information InfoFrame; this length does not include the checksum
43h	AVI_IF_ CHECKSUM	7 to 0	AVI_IF_ CHECKSUM[7:0]	R/W	00h*	**auxiliary video information InfoFrame checksum:** shall be calculated such that a byte-wide sum of all three bytes of the packet header and all valid bytes of the auxiliary video information InfoFrame packet contents (determined by InfoFrame length) plus the checksum itself equals 0

Table 85. AVI_IF_xx registers (address 40h to 5Eh) bit description *...continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
44h	AVI_IF_BYTE1	7	reserved	R/W	0*	reserved (shall be zero)
		6 to 5	AVI_IF_Y[1:0]	R/W		**auxiliary video information InfoFrame Y**: RGB or YC_BC_R indicator
					00*	RGB
					01	YC_BC_R 4 : 2 : 2
					10	YC_BC_R 4 : 4 : 4
					11	future
		4	AVI_IF_A	R/W		**auxiliary video information InfoFrame A**: active format information present
					0*	no data
					1	active format information valid
		3 to 2	AVI_IF_B[1:0]	R/W		**auxiliary video information InfoFrame bar:** bar information
					00*	bar data not valid
					01	vertical bar info valid
					10	horizontal bar info valid
					11	vertical and horizontal bar info valid
		1 to 0	AVI_IF_S[1:0]	R/W		**auxiliary video information InfoFrame scan:** scan information
					00*	no data
					01	overscanned (television)
					10	underscanned (computer)
					11	future
45h	AVI_IF_BYTE2	7 to 6	AVI_IF_C[1:0]	R/W		**auxiliary video information InfoFrame colorimetry**: colorimetry
					00*	no data
					01	ITU601
					10	ITU709
					11	future
		5 to 4	AVI_IF_M[1:0]	R/W		**auxiliary video information InfoFrame M**: picture aspect ratio
					00*	no data
					01	4 : 3
					10	16 : 9
					11	future
		3 to 0	AVI_IF_R[3:0]	R/W		**auxiliary video information InfoFrame ratio**: active format aspect ratio
					1000	same as picture aspect ratio
					1001	4 : 3 (center)
					1010	16 : 9 (center)
					1011	14 : 9 (center)
					other	per DVB AFD active_format field

Table 85. AVI_IF_xx registers (address 40h to 5Eh) bit description *...continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
46h	AVI_IF_BYTE3	7 to 2	reserved	R/W	0000 00*	reserved (shall be zero)
		1 to 0	AVI_IF_SC[1:0]	R/W		**auxiliary video information InfoFrame scaling**: non-uniform picture scaling
					00*	no known non-uniform scaling
					01	picture has been scaled horizontally
					10	picture has been scaled vertically
					11	picture has been scaled horizontally and vertically
47h	AVI_IF_BYTE4	7	reserved	R/W	0*	reserved (shall be zero)
		6 to 0	AVI_IF_VIC[6:0]	R/W	000 0000*	**auxiliary video information InfoFrame video identification code**: video identification code
48h	AVI_IF_BYTE5	7 to 4	reserved	R/W	0000*	reserved (shall be zero)
		3 to 0	AVI_IF_PR[3:0]	R/W	0000*	**auxiliary video information InfoFrame pixel repetition**: pixel repetition
49h	AVI_IF_BYTE6	7 to 0	LINE_E_TP_BAR[7:0]	R/W	00h*	**line number of end of top bar**
4Ah	AVI_IF_BYTE7	7 to 0	LINE_E_TP_BAR[15:8]	R/W	00h*	
4Bh	AVI_IF_BYTE8	7 to 0	LINE_S_BT_BAR[7:0]	R/W	00h*	**line number of start of bottom bar**
4Ch	AVI_IF_BYTE9	7 to 0	LINE_S_BT_BAR[15:8]	R/W	00h*	
4Dh	AVI_IF_BYTE10	7 to 0	PIX_E_LF_BAR[7:0]	R/W	00h*	**pixel number of end of left bar**
4Eh	AVI_IF_BYTE11	7 to 0	PIX_E_LF_BAR[15:8]	R/W	00h*	
4Fh	AVI_IF_BYTE12	7 to 0	PIX_S_RG_BAR[7:0]	R/W	00h*	**pixel number of start of right bar**
50h	AVI_IF_BYTE13	7 to 0	PIX_S_RG_BAR[15:8]	R/W	00h*	
						auxiliary video information InfoFrame reserved byte x: x = 14 to 27
51h	AVI_IF_BYTE14	7 to 0	AVI_IF_RB14[7:0]	R/W	00h*	byte 14; reserved (shall be zero)
52h	AVI_IF_BYTE15	7 to 0	AVI_IF_RB15[7:0]	R/W	00h*	byte 15; reserved (shall be zero)
53h	AVI_IF_BYTE16	7 to 0	AVI_IF_RB16[7:0]	R/W	00h*	byte 16; reserved (shall be zero)
54h	AVI_IF_BYTE17	7 to 0	AVI_IF_RB17[7:0]	R/W	00h*	byte 17; reserved (shall be zero)
55h	AVI_IF_BYTE18	7 to 0	AVI_IF_RB18[7:0]	R/W	00h*	byte 18; reserved (shall be zero)
56h	AVI_IF_BYTE19	7 to 0	AVI_IF_RB19[7:0]	R/W	00h*	byte 19; reserved (shall be zero)
57h	AVI_IF_BYTE20	7 to 0	AVI_IF_RB20[7:0]	R/W	00h*	byte 20; reserved (shall be zero)
58h	AVI_IF_BYTE21	7 to 0	AVI_IF_RB21[7:0]	R/W	00h*	byte 21; reserved (shall be zero)
59h	AVI_IF_BYTE22	7 to 0	AVI_IF_RB22[7:0]	R/W	00h*	byte 22; reserved (shall be zero)
5Ah	AVI_IF_BYTE23	7 to 0	AVI_IF_RB23[7:0]	R/W	00h*	byte 23; reserved (shall be zero)
5Bh	AVI_IF_BYTE24	7 to 0	AVI_IF_RB24[7:0]	R/W	00h*	byte 24; reserved (shall be zero)
5Ch	AVI_IF_BYTE25	7 to 0	AVI_IF_RB25[7:0]	R/W	00h*	byte 25; reserved (shall be zero)
5Dh	AVI_IF_BYTE26	7 to 0	AVI_IF_RB26[7:0]	R/W	00h*	byte 26; reserved (shall be zero)
5Eh	AVI_IF_BYTE27	7 to 0	AVI_IF_RB27[7:0]	R/W	00h*	byte 27; reserved (shall be zero)

9.6.3 Source product description InfoFrame registers

Below is an example of use. Please refer to *EIA/CEA-861B specification* and *HDMI 1.2a specification* for the correct definition of data bytes.

Table 86. SPD_IF_xx registers (address 60h to 7Eh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
60h	SPD_IF_TYPE	7 to 0	SPD_IF_TYPE[7:0]	R/W	83h*	**source product description InfoFrame packet type:** gives the packet type of the source product description InfoFrame packet (80h + InfoFrame type code as per *EIA/CEA-861B*)
61h	SPD_IF_VERSION	7 to 0	SPD_IF_ VERSION[7:0]	R/W	00h*	**source product description InfoFrame version**: gives the version number of the source product description InfoFrame
62h	SPD_IF_LENGTH	7 to 5	x	R/W	000*	reserved (shall be 000)
		4 to 0	SPD_IF_LENGTH[4:0]	R/W	0 0000*	**source product description InfoFrame length**: gives the number of data bytes for the source product description InfoFrame; this length does not include the checksum
63h	SPD_IF_CHECKSUM	7 to 0	SPD_IF_ CHECKSUM[7:0]	R/W	00h*	**source product description InfoFrame checksum**: shall be calculated such that a byte-wide sum of all three bytes of the packet header and all valid bytes of the source product description InfoFrame packet contents (determined by InfoFrame length) plus the checksum itself equals 0
						source product description InfoFrame vendor name: 7-bit ASCII code
64h	SPD_IF_BYTE1	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_VN1[6:0]	R/W	000 0000*	character 1
65h	SPD_IF_BYTE2	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_VN2[6:0]	R/W	000 0000*	character 2
66h	SPD_IF_BYTE3	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_VN3[6:0]	R/W	000 0000*	character 3
67h	SPD_IF_BYTE4	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_VN4[6:0]	R/W	000 0000*	character 4
68h	SPD_IF_BYTE5	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_VN5[6:0]	R/W	000 0000*	character 5
69h	SPD_IF_BYTE6	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_VN6[6:0]	R/W	000 0000*	character 6
6Ah	SPD_IF_BYTE7	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_VN7[6:0]	R/W	000 0000*	character 7

Table 86. SPD_IF_xx registers (address 60h to 7Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
6Bh	SPD_IF_BYTE8	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_VN8[6:0]	R/W	000 0000*	character 8
						source product description InfoFrame product description: 7-bit ASCII code
6Ch	SPD_IF_BYTE9	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD1[6:0]	R/W	000 0000*	character 1
6Dh	SPD_IF_BYTE10	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD2[6:0]	R/W	000 0000*	character 2
6Eh	SPD_IF_BYTE11	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD3[6:0]	R/W	000 0000*	character 3
6Fh	SPD_IF_BYTE12	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD4[6:0]	R/W	000 0000*	character 4
70h	SPD_IF_BYTE13	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD5[6:0]	R/W	000 0000*	character 5
71h	SPD_IF_BYTE14	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD6[6:0]	R/W	000 0000*	character 6
72h	SPD_IF_BYTE15	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD7[6:0]	R/W	000 0000*	character 7
73h	SPD_IF_BYTE16	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD8[6:0]	R/W	000 0000*	character 8
74h	SPD_IF_BYTE17	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD9[6:0]	R/W	000 0000*	character 9
75h	SPD_IF_BYTE18	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD10[6:0]	R/W	000 0000*	character 10
76h	SPD_IF_BYTE19	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD11[6:0]	R/W	000 0000*	character 11
77h	SPD_IF_BYTE20	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD12[6:0]	R/W	000 0000*	character 12
78h	SPD_IF_BYTE21	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD13[6:0]	R/W	000 0000*	character 13
79h	SPD_IF_BYTE22	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD14[6:0]	R/W	000 0000*	character 14
7Ah	SPD_IF_BYTE23	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD15[6:0]	R/W	000 0000*	character 15
7Bh	SPD_IF_BYTE24	7	x	R/W	0*	reserved (shall be zero)
		6 to 0	SPD_IF_PD16[6:0]	R/W	000 0000*	character 16

Table 86. SPD_IF_xx registers (address 60h to 7Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
7Ch	SPD_IF_BYTE25	7 to 0	SPD_IF_SDI[7:0]	R/W		**source product description InfoFrame source device information:** source device information
					00h*	unknown
					01h	digital STB
					02h	DVD
					03h	D-VHS
					04h	HDD video
					05h	DVC
					06h	DSC
					07h	video CD
					08h	game
					09h	PC general
						source product description InfoFrame data byte
7Dh	SPD_IF_BYTE26	7 to 0	SPD_IF_BYTE26[7:0]	R/W	00h*	data byte 26
7Eh	SPD_IF_BYTE27	7 to 0	SPD_IF_BYTE27[7:0]	R/W	00h*	data byte 27

9.6.4 Audio InfoFrame registers

Below is an example of use. Please refer to *EIA/CEA-861B specification* and *HDMI 1.2a specification* for the correct definition of data bytes.

Table 87. AUD_IF_xx registers (address 80h to 9Eh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
80h	AUD_IF_TYPE	7 to 0	AUD_IF_TYPE[7:0]	R/W	84h*	**audio InfoFrame packet type:** gives the packet type of the audio InfoFrame packet (80h + InfoFrame type code as per *EIA/CEA-861B*)
81h	AUD_IF_VERSION	7 to 0	AUD_IF_ VERSION[7:0]	R/W	00h*	**audio InfoFrame version**: gives the version number of the audio InfoFrame
82h	AUD_IF_LENGTH	7 to 5	x	R/W	000*	reserved (shall be zero)
		4 to 0	AUD_IF_LENGTH[4:0]	R/W	0 0000*	**audio InfoFrame length**: gives the number of data bytes for the audio InfoFrame; this length does not include the checksum
83h	AUD_IF_CHECKSUM	7 to 0	AUD_IF_ CHECKSUM[7:0]	R/W	00h*	**audio InfoFrame checksum**: shall be calculated such that a byte-wide sum of all three bytes of the packet header and all valid bytes of the audio InfoFrame packet contents (determined by InfoFrame length) plus the checksum itself equals 0

Table 87. AUD_IF_xx registers (address 80h to 9Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
84h	AUD_IF_BYTE1	7 to 4	AUD_IF_CT[3:0]	R/W		**audio InfoFrame coding type:** audio coding type
					0000*	refer to stream header
					0001	IEC 60958 PCM
					0010	AC-3
					0011	MPEG1
					0100	MP3
					0101	MPEG2
					0110	AAC
					0111	DTS
					1000	ATRAC
					other	undefined
		3	reserved	R/W	0*	reserved bit
		2 to 0	AUD_IF_CC[2:0]	R/W		**audio InfoFrame channel count:** audio channel count
					000*	refer to stream header
					001	2 channels
					010	3 channels
					011	4 channels
					100	5 channels
					101	6 channels
					110	7 channels
					111	8 channels
85h	AUD_IF_BYTE2	7 to 5	reserved	R/W	000*	reserved (shall be zero)
		4 to 2	AUD_IF_SF[2:0]	R/W		**audio InfoFrame sampling frequency:** sampling frequency
					000*	refer to stream header
					001	32 kHz
					010	44.1 kHz (CD)
					011	48 kHz
					100	88.2 kHz
					101	96 kHz
					110	176.4 kHz
					111	192 kHz
		1 to 0	AUD_IF_SS[1:0]	R/W		**audio InfoFrame sample size:** sample size
					00*	refer to stream header
					01	16 bits
					10	20 bits
					11	24 bits

Table 87. AUD_IF_xx registers (address 80h to 9Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
86h	AUD_IF_BYTE3	7 to 0	AUD_IF_BYTE3[7:0]	R/W	00h*	**audio InfoFrame data byte 3:** value × 8 kHz = maximum bit rate of audio stream (compressed audio format)
87h	AUD_IF_BYTE4	7 to 0	AUD_IF_CA[7:0]	R/W	00h*	**audio InfoFrame channel allocation:** channel allocation (LPCM)
88h	AUD_IF_BYTE5	7	AUD_IF_DM_INH	R/W		**audio InfoFrame down-mix inhibit flag:** down-mix inhibit flag
					0*	permitted or no information about any assertion of this
					1	prohibited
		6 to 3	AUD_IF_LSV[3:0]	R/W		**audio InfoFrame level shift value:** level shift value
					0000*	0 dB
					0001	1 dB
					0010	2 dB
					0011	3 dB
					1000	4 dB
					:	:
					1111	15 dB
		2 to 0	reserved	R/W	000*	reserved (shall be 000h)
						audio InfoFrame data byte x: x = 6 to 27
89h	AUD_IF_BYTE6	7 to 0	AUD_IF_BYTE6[7:0]	R/W	00h*	byte 6: reserved (shall be zero)
8Ah	AUD_IF_BYTE7	6 to 0	AUD_IF_BYTE7[7:0]	R/W	00h*	byte 7: reserved (shall be zero)
8Bh	AUD_IF_BYTE8	6 to 0	AUD_IF_BYTE8[7:0]	R/W	00h*	byte 8: reserved (shall be zero)
8Ch	AUD_IF_BYTE9	6 to 0	AUD_IF_BYTE9[7:0]	R/W	00h*	byte 9: reserved (shall be zero)
8Dh	AUD_IF_BYTE10	7 to 0	AUD_IF_BYTE10[7:0]	R/W	00h*	byte 10: reserved (shall be zero)
8Eh	AUD_IF_BYTE11	7 to 0	AUD_IF_BYTE11[7:0]	R/W	00h*	byte 11: reserved (shall be zero)
8Fh	AUD_IF_BYTE12	7 to 0	AUD_IF_BYTE12[7:0]	R/W	00h*	byte 12: reserved (shall be zero)
90h	AUD_IF_BYTE13	7 to 0	AUD_IF_BYTE13[7:0]	R/W	00h*	byte 13: reserved (shall be zero)
91h	AUD_IF_BYTE14	7 to 0	AUD_IF_BYTE14[7:0]	R/W	00h*	byte 14: reserved (shall be zero)
92h	AUD_IF_BYTE15	7 to 0	AUD_IF_BYTE15[7:0]	R/W	00h*	byte 15: reserved (shall be zero)
93h	AUD_IF_BYTE16	7 to 0	AUD_IF_BYTE16[7:0]	R/W	00h*	byte 16: reserved (shall be zero)
94h	AUD_IF_BYTE17	7 to 0	AUD_IF_BYTE17[7:0]	R/W	00h*	byte 17: reserved (shall be zero)
95h	AUD_IF_BYTE18	7 to 0	AUD_IF_BYTE18[7:0]	R/W	00h*	byte 18: reserved (shall be zero)
96h	AUD_IF_BYTE19	7 to 0	AUD_IF_BYTE19[7:0]	R/W	00h*	byte 19: reserved (shall be zero)
97h	AUD_IF_BYTE20	7 to 0	AUD_IF_BYTE20[7:0]	R/W	00h*	byte 20: reserved (shall be zero)
98h	AUD_IF_BYTE21	7 to 0	AUD_IF_BYTE21[7:0]	R/W	00h*	byte 21: reserved (shall be zero)
99h	AUD_IF_BYTE22	7 to 0	AUD_IF_BYTE22[7:0]	R/W	00h*	byte 22: reserved (shall be zero)
9Ah	AUD_IF_BYTE23	7 to 0	AUD_IF_BYTE23[7:0]	R/W	00h*	byte 23: reserved (shall be zero)

Table 87. AUD_IF_xx registers (address 80h to 9Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
9Bh	AUD_IF_BYTE24	7 to 0	AUD_IF_BYTE24[7:0]	R/W	00h*	byte 24: reserved (shall be zero)
9Ch	AUD_IF_BYTE25	7 to 0	AUD_IF_BYTE25[7:0]	R/W	00h*	byte 25: reserved (shall be zero)
9Dh	AUD_IF_BYTE26	7 to 0	AUD_IF_BYTE26[7:0]	R/W	00h*	byte 26: reserved (shall be zero)
9Eh	AUD_IF_BYTE27	7 to 0	AUD_IF_BYTE27[7:0]	R/W	00h*	byte 27: reserved (shall be zero)

9.6.5 MPEG source InfoFrame registers

Below is an example of use. Please refer to *EIA/CEA-861B specification* and *HDMI 1.2a specification* for the correct definition of data bytes.

Table 88. MPS_IF_xx registers (address A0h to BEh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
A0h	MPS_IF_TYPE	7 to 0	MPS_IF_TYPE[7:0]	R/W	85h*	**MPEG source InfoFrame packet type:** gives the packet type of the MPEG source InfoFrame packet (80h + InfoFrame type code as per *EIA/CEA-861B*)
A1h	MPS_IF_VERSION	7 to 0	MPS_IF_VERSION[7:0]	R/W	00h*	**MPEG source InfoFrame version**: gives the version number of the MPEG source InfoFrame
A2h	MPS_IF_LENGTH	7 to 5	x	R/W	000*	reserved (shall be zero)
		4 to 0	MPS_IF_LENGTH[4:0]	R/W	0 0000*	**MPEG source InfoFrame length**: gives the number of data bytes for the MPEG source InfoFrame; this length does not include the checksum
A3h	MPS_IF_ CHECKSUM	7 to 0	MPS_IF_ CHECKSUM[7:0]	R/W	00h*	**MPEG source InfoFrame checksum**: shall be calculated such that a byte-wide sum of all three bytes of the packet header and all valid bytes of the MPEG source InfoFrame packet contents (determined by InfoFrame length) plus the checksum itself equals 0
						MPEG source InfoFrame MPEG bit rate (Hz)
A4h	MPS_IF_BYTE1	7 to 0	MPS_IF_MB0[7:0]	R/W	00h*	MB#0 (lower byte)
A5h	MPS_IF_BYTE2	7 to 0	MPS_IF_MB1[7:0]	R/W	00h*	MB#1 (medium byte)
A6h	MPS_IF_BYTE3	7 to 0	MPS_IF_MB2[7:0]	R/W	00h*	MB#2 (medium byte)
A7h	MPS_IF_BYTE4	7 to 0	MPS_IF_MB3[7:0]	R/W	00h*	MB#3 (upper byte)

Table 88. MPS_IF_xx registers (address A0h to BEh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
A8h	MPS_IF_BYTE5	7 to 5	reserved	R/W	000*	reserved
		4	MPS_IF_FR0	R/W		**MPEG source InfoFrame field repeat 0**: for 3 : 2 pull-down
					0*	new field (picture)
					1	repeated field
		3 to 2	reserved	R/W	00*	reserved
		1 to 0	MPS_IF_MF[1:0]	R/W		**MPEG source InfoFrame MPEG frame**: MPEG frame
					00*	unknown (no data)
					01	I picture
					10	B picture
					11	P picture
						MPEG source InfoFrame byte x: x = 6 to 27
A9h	MPS_IF_BYTE6	7 to 0	MPS_IF_BYTE6[7:0]	R/W	00h*	byte 6: reserved (shall be zero)
AAh	MPS_IF_BYTE7	6 to 0	MPS_IF_BYTE7[7:0]	R/W	000 0000*	byte 7: reserved (shall be zero)
ABh	MPS_IF_BYTE8	6 to 0	MPS_IF_BYTE8[7:0]	R/W	000 0000*	byte 8: reserved (shall be zero)
ACh	MPS_IF_BYTE9	6 to 0	MPS_IF_BYTE9[7:0]	R/W	000 0000*	byte 9: reserved (shall be zero)
ADh	MPS_IF_BYTE10	7 to 0	MPS_IF_BYTE10[7:0]	R/W	00h*	byte 10: reserved (shall be zero)
AEh	MPS_IF_BYTE11	7 to 0	MPS_IF_BYTE11[7:0]	R/W	00h*	byte 11: reserved
AFh	MPS_IF_BYTE12	7 to 0	MPS_IF_BYTE12[7:0]	R/W	00h*	byte 12: reserved
B0h	MPS_IF_BYTE13	7 to 0	MPS_IF_BYTE13[7:0]	R/W	00h*	byte 13: reserved
B1h	MPS_IF_BYTE14	7 to 0	MPS_IF_BYTE14[7:0]	R/W	00h*	byte 14: reserved
B2h	MPS_IF_BYTE15	7 to 0	MPS_IF_BYTE15[7:0]	R/W	00h*	byte 15: reserved
B3h	MPS_IF_BYTE16	7 to 0	MPS_IF_BYTE16[7:0]	R/W	00h*	byte 16: reserved
B4h	MPS_IF_BYTE17	7 to 0	MPS_IF_BYTE17[7:0]	R/W	00h*	byte 17: reserved
B5h	MPS_IF_BYTE18	7 to 0	MPS_IF_BYTE18[7:0]	R/W	00h*	byte 18: reserved
B6h	MPS_IF_BYTE19	7 to 0	MPS_IF_BYTE19[7:0]	R/W	00h*	byte 19: reserved
B7h	MPS_IF_BYTE20	7 to 0	MPS_IF_BYTE20[7:0]	R/W	00h*	byte 20: reserved
B8h	MPS_IF_BYTE21	7 to 0	MPS_IF_BYTE21[7:0]	R/W	00h*	byte 21: reserved
B9h	MPS_IF_BYTE22	7 to 0	MPS_IF_BYTE22[7:0]	R/W	00h*	byte 22: reserved
BAh	MPS_IF_BYTE23	7 to 0	MPS_IF_BYTE23[7:0]	R/W	00h*	byte 23: reserved
BBh	MPS_IF_BYTE24	7 to 0	MPS_IF_BYTE24[7:0]	R/W	00h*	byte 24: reserved
BCh	MPS_IF_BYTE25	7 to 0	MPS_IF_BYTE25[7:0]	R/W	00h*	byte 25: reserved
BDh	MPS_IF_BYTE26	7 to 0	MPS_IF_BYTE26[7:0]	R/W	00h*	byte 26: reserved
BEh	MPS_IF_BYTE27	7 to 0	MPS_IF_BYTE27[7:0]	R/W	00h*	byte 27: reserved

9.6.6 Current page address register

Table 89. CURPAGE_ADR register (address FFh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	CURPAGE_ADR[7:0]	W	00h*	**current page address:** selects the current memory page

9.7 Audio settings and content info packets page register definitions

The current page address for the audio settings and content info packets page is 11h.

The configuration of the registers for this page is given in Table 90.

Table 90. I²C-bus registers of memory page 11h[1]

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
AIP_CNTRL_0	00h	R/W	x	RST_CTS	ACR_MAN	x	x	LAYOUT	SWAP	RST_FIFO	0000 0000
CA_I2S	01h	R/W	x	x	x	CA_I2S[4:0]					0000 0000
For test	02h	R/W	x	x	x	x	x	x	x	x	0000 0000
For test	03h	R/W	x	x	x	x	x	x	x	x	0000 0000
LATENCY_RD	04h	R/W	LATENCY_RD[7:0]								0000 0100
ACR_CTS_0	05h	R/W	CTS[7:0]								0111 1000
ACR_CTS_1	06h	R/W	CTS[15:8]								0110 1001
ACR_CTS_2	07h	R/W	x	x	x	x	CTS[19:16]				0000 0000
ACR_N_0	08h	R/W	N[7:0]								0000 0000
ACR_N_1	09h	R/W	N[15:8]								0110 0000
ACR_N_2	0Ah	R/W	x	x	x	x	N[19:16]				0000 0000
GC_AVMUTE	0Bh	R/W	x	x	x	x	x	x	SET_MUTE	CLR_MUTE	0000 0000
CTS_N	0Ch	R/W	x	x	M_SEL[1:0]		x	K_SEL[2:0]			0000 0000
ENC_CNTRL	0Dh	R/W	x	x	x	x	CTL_CODE[1:0]		DC_CTL[1:0]		0000 0100
DIP_FLAGS	0Eh	R/W	FORCE_NULL	NULL	-	ACP	ISRC2	ISRC1	GC	ACR	0000 0000
DIP_IF_FLAGS	0Fh	R/W	x	x	IF5	IF4	IF3	IF2	IF1	x	0000 0000
Not used	10h	-	-								0000 0000
:	:	:	:								:
Not used	13h	-	-								0000 0000
CH_STAT_B_0	14h	R/W	CH_STAT_BYTE_0[7:0]								0000 0000
CH_STAT_B_1	15h	R/W	CH_STAT_BYTE_1[7:0]								0000 0000
CH_STAT_B_3	16h	R/W	CH_STAT_BYTE_3[7:0]								0000 0000
CH_STAT_B_4	17h	R/W	CH_STAT_BYTE_4[7:0]								0000 0000
CH_STAT_B_2_AP0_L	18h	R/W	CH_STAT_BYTE_2_AP0_L[7:0]								0000 0000
CH_STAT_B_2_AP0_R	19h	R/W	CH_STAT_BYTE_2_AP0_R[7:0]								0000 0000
CH_STAT_B_2_AP1_L	1Ah	R/W	CH_STAT_BYTE_2_AP1_L[7:0]								0000 0000
CH_STAT_B_2_AP1_R	1Bh	R/W	CH_STAT_BYTE_2_AP1_R[7:0]								0000 0000
CH_STAT_B_2_AP2_L	1Ch	R/W	CH_STAT_BYTE_2_AP2_L[7:0]								0000 0000
CH_STAT_B_2_AP2_R	1Dh	R/W	CH_STAT_BYTE_2_AP2_R[7:0]								0000 0000
CH_STAT_B_2_AP3_L	1Eh	R/W	CH_STAT_BYTE_2_AP3_L[7:0]								0000 0000

Table 90. I²C-bus registers of memory page 11h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
CH_STAT_B_2_AP3_R	1Fh	R/W	CH_STAT_BYTE_2_AP3_R[7:0]								0000 0000
ISRC1_PACKET_TYPE	20h	R/W	ISRC1_PACKET_TYPE[7:0]								0000 0101
ISRC1_CTRL	21h	R/W	ISRC_CONT	ISRC_VALID	ISRC1_RSVD[5:3]			ISRC_STATUS[2:0]			0000 0000
ISRC1_RSVD	22h	R/W	ISRC1_RSVD[7:0]								0000 0000
UPC_EAN_ISRC_0	23h	R/W	UPC_EAN_ISRC_0[7:0]								0000 0000
UPC_EAN_ISRC_1	24h	R/W	UPC_EAN_ISRC_1[7:0]								0000 0000
UPC_EAN_ISRC_2	25h	R/W	UPC_EAN_ISRC_2[7:0]								0000 0000
UPC_EAN_ISRC_3	26h	R/W	UPC_EAN_ISRC_3[7:0]								0000 0000
UPC_EAN_ISRC_4	27h	R/W	UPC_EAN_ISRC_4[7:0]								0000 0000
UPC_EAN_ISRC_5	28h	R/W	UPC_EAN_ISRC_5[7:0]								0000 0000
UPC_EAN_ISRC_6	29h	R/W	UPC_EAN_ISRC_6[7:0]								0000 0000
UPC_EAN_ISRC_7	2Ah	R/W	UPC_EAN_ISRC_7[7:0]								0000 0000
UPC_EAN_ISRC_8	2Bh	R/W	UPC_EAN_ISRC_8[7:0]								0000 0000
UPC_EAN_ISRC_9	2Ch	R/W	UPC_EAN_ISRC_9[7:0]								0000 0000
UPC_EAN_ISRC_10	2Dh	R/W	UPC_EAN_ISRC_10[7:0]								0000 0000
UPC_EAN_ISRC_11	2Eh	R/W	UPC_EAN_ISRC_11[7:0]								0000 0000
UPC_EAN_ISRC_12	2Fh	R/W	UPC_EAN_ISRC_12[7:0]								0000 0000
UPC_EAN_ISRC_13	30h	R/W	UPC_EAN_ISRC_13[7:0]								0000 0000
UPC_EAN_ISRC_14	31h	R/W	UPC_EAN_ISRC_14[7:0]								0000 0000
UPC_EAN_ISRC_15	32h	R/W	UPC_EAN_ISRC_15[7:0]								0000 0000
ISRC1_PB16	33h	R/W	ISRC1_PB_BYTE_16[7:0]								0000 0000
ISRC1_PB17	34h	R/W	ISRC1_PB_BYTE_17[7:0]								0000 0000
ISRC1_PB18	35h	R/W	ISRC1_PB_BYTE_18[7:0]								0000 0000
ISRC1_PB19	36h	R/W	ISRC1_PB_BYTE_19[7:0]								0000 0000
ISRC1_PB20	37h	R/W	ISRC1_PB_BYTE_20[7:0]								0000 0000
ISRC1_PB21	38h	R/W	ISRC1_PB_BYTE_21[7:0]								0000 0000
ISRC1_PB22	39h	R/W	ISRC1_PB_BYTE_22[7:0]								0000 0000
ISRC1_PB23	3Ah	R/W	ISRC1_PB_BYTE_23[7:0]								0000 0000
ISRC1_PB24	3Bh	R/W	ISRC1_PB_BYTE_24[7:0]								0000 0000
ISRC1_PB25	3Ch	R/W	ISRC1_PB_BYTE_25[7:0]								0000 0000
ISRC1_PB26	3Dh	R/W	ISRC1_PB_BYTE_26[7:0]								0000 0000

Table 90. I²C-bus registers of memory page 11h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
ISRC1_PB27	3Eh	R/W	ISRC1_PB_BYTE_27[7:0]								0000 0000
Not used	3Fh	-	-								0000 0000
ISRC2_PACKET_TYPE	40h	R/W	ISRC2_PACKET_TYPE[7:0]								0000 0110
ISRC2_RSVD1	41h	R/W	ISRC2_RSVD1[7:0]								0000 0000
ISRC2_RSVD2	42h	R/W	ISRC2_RSVD2[7:0]								0000 0000
UPC_EAN_ISRC_16	43h	R/W	UPC_EAN_ISRC_16[7:0]								0000 0000
UPC_EAN_ISRC_17	44h	R/W	UPC_EAN_ISRC_17[7:0]								0000 0000
UPC_EAN_ISRC_18	45h	R/W	UPC_EAN_ISRC_18[7:0]								0000 0000
UPC_EAN_ISRC_19	46h	R/W	UPC_EAN_ISRC_19[7:0]								0000 0000
UPC_EAN_ISRC_20	47h	R/W	UPC_EAN_ISRC_20[7:0]								0000 0000
UPC_EAN_ISRC_21	48h	R/W	UPC_EAN_ISRC_21[7:0]								0000 0000
UPC_EAN_ISRC_22	49h	R/W	UPC_EAN_ISRC_22[7:0]								0000 0000
UPC_EAN_ISRC_23	4Ah	R/W	UPC_EAN_ISRC_23[7:0]								0000 0000
UPC_EAN_ISRC_24	4Bh	R/W	UPC_EAN_ISRC_24[7:0]								0000 0000
UPC_EAN_ISRC_25	4Ch	R/W	UPC_EAN_ISRC_25[7:0]								0000 0000
UPC_EAN_ISRC_26	4Dh	R/W	UPC_EAN_ISRC_26[7:0]								0000 0000
UPC_EAN_ISRC_27	4Eh	R/W	UPC_EAN_ISRC_27[7:0]								0000 0000
UPC_EAN_ISRC_28	4Fh	R/W	UPC_EAN_ISRC_28[7:0]								0000 0000
UPC_EAN_ISRC_29	50h	R/W	UPC_EAN_ISRC_29[7:0]								0000 0000
UPC_EAN_ISRC_30	51h	R/W	UPC_EAN_ISRC_30[7:0]								0000 0000
UPC_EAN_ISRC_31	52h	R/W	UPC_EAN_ISRC_31[7:0]								0000 0000
ISRC2_PB16	53h	R/W	ISRC2_PB_BYTE_16[7:0]								0000 0000
ISRC2_PB17	54h	R/W	ISRC2_PB_BYTE_17[7:0]								0000 0000
ISRC2_PB18	55h	R/W	ISRC2_PB_BYTE_18[7:0]								0000 0000
ISRC2_PB19	56h	R/W	ISRC2_PB_BYTE_19[7:0]								0000 0000
ISRC2_PB20	57h	R/W	ISRC2_PB_BYTE_20[7:0]								0000 0000
ISRC2_PB21	58h	R/W	ISRC2_PB_BYTE_21[7:0]								0000 0000
ISRC2_PB22	59h	R/W	ISRC2_PB_BYTE_22[7:0]								0000 0000
ISRC2_PB23	5Ah	R/W	ISRC2_PB_BYTE_23[7:0]								0000 0000
ISRC2_PB24	5Bh	R/W	ISRC2_PB_BYTE_24[7:0]								0000 0000
ISRC2_PB25	5Ch	R/W	ISRC2_PB_BYTE_25[7:0]								0000 0000
ISRC2_PB26	5Dh	R/W	ISRC2_PB_BYTE_26[7:0]								0000 0000

Table 90. I²C-bus registers of memory page 11h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
ISRC2_PB27	5Eh	R/W	ISRC2_PB_BYTE_27[7:0]								0000 0000
Not used	5Fh	-	-								0000 0000
ACP_PACKET_TYPE	60h	R/W	ACP_PACKET_TYPE[7:0]								0000 0100
ACP_TYPE	61h	R/W	ACP_TYPE[7:0]								0000 0000
ACP_RSVD	62h	R/W	ACP_RSVD[7:0]								0000 0000
ACP_PB0	63h	R/W	ACP_PB_BYTE_0[7:0]								0000 0000
ACP_PB1	64h	R/W	ACP_PB_BYTE_1[7:0]								0000 0000
ACP_PB2	65h	R/W	ACP_PB_BYTE_2[7:0]								0000 0000
ACP_PB3	66h	R/W	ACP_PB_BYTE_3[7:0]								0000 0000
ACP_PB4	67h	R/W	ACP_PB_BYTE_4[7:0]								0000 0000
ACP_PB5	68h	R/W	ACP_PB_BYTE_5[7:0]								0000 0000
ACP_PB6	69h	R/W	ACP_PB_BYTE_6[7:0]								0000 0000
ACP_PB7	6Ah	R/W	ACP_PB_BYTE_7[7:0]								0000 0000
ACP_PB8	6Bh	R/W	ACP_PB_BYTE_8[7:0]								0000 0000
ACP_PB9	6Ch	R/W	ACP_PB_BYTE_9[7:0]								0000 0000
ACP_PB10	6Dh	R/W	ACP_PB_BYTE_10[7:0]								0000 0000
ACP_PB11	6Eh	R/W	ACP_PB_BYTE_11[7:0]								0000 0000
ACP_PB12	6Fh	R/W	ACP_PB_BYTE_12[7:0]								0000 0000
ACP_PB13	70h	R/W	ACP_PB_BYTE_13[7:0]								0000 0000
ACP_PB14	71h	R/W	ACP_PB_BYTE_14[7:0]								0000 0000
ACP_PB15	72h	R/W	ACP_PB_BYTE_15[7:0]								0000 0000
ACP_PB16	73h	R/W	ACP_PB_BYTE_16[7:0]								0000 0000
ACP_PB17	74h	R/W	ACP_PB_BYTE_17[7:0]								0000 0000
ACP_PB18	75h	R/W	ACP_PB_BYTE_18[7:0]								0000 0000
ACP_PB19	76h	R/W	ACP_PB_BYTE_19[7:0]								0000 0000
ACP_PB20	77h	R/W	ACP_PB_BYTE_20[7:0]								0000 0000
ACP_PB21	78h	R/W	ACP_PB_BYTE_21[7:0]								0000 0000
ACP_PB22	79h	R/W	ACP_PB_BYTE_22[7:0]								0000 0000
ACP_PB23	7Ah	R/W	ACP_PB_BYTE_23[7:0]								0000 0000
ACP_PB24	7Bh	R/W	ACP_PB_BYTE_24[7:0]								0000 0000
ACP_PB25	7Ch	R/W	ACP_PB_BYTE_25[7:0]								0000 0000
ACP_PB26	7Dh	R/W	ACP_PB_BYTE_26[7:0]								0000 0000

Table 90. I²C-bus registers of memory page 11h[1] *…continued*

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
ACP_PB27	7Eh	R/W	ACP_PB_BYTE_27[7:0]								0000 0000
Not used	7Fh	-	-								0000 0000
:	:	:	:								:
Not used	FEh	-	-								0000 0000
CURPAGE_ADR	FFh	W	CURPAGE_ADR[7:0]								0000 0000

[1] R: reading register
W: writing register
x: bit must be set to default value for proper operation
-: not used

9.7.1 Audio input processor control registers

Table 91. AIP_CNTRL_0 register (address 00h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	x	R/W	0*	undefined
6	RST_CTS	R/W		**reset CTS**
			0*	no specific action
			1	reset CTS generation (soft reset)
5	ACR_MAN	R/W		**audio clock regeneration manual**
			0*	automatic audio clock regeneration time stamp generation
			1	manual audio clock regeneration time stamp generation
4 to 3	x	R/W	00*	undefined
2	LAYOUT	R/W		**layout**
			0*	set layout 0
			1	set layout 1
1	SWAP	R/W	0*	**swap:** for internal use
0	RST_FIFO	R/W		**reset FIFO**
			0*	no specific action
			1	reset audio FIFO

Table 92. CA_I2S register (address 01h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	x	R/W	000*	undefined
4 to 0	CA_I2S[4:0]	R/W	0 0000*	**channel allocation I^2S-bus port:** layout 1

Table 93. LATENCY_RD register (address 04h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	LATENCY_RD[7:0]	R/W	04h*	**latency read:** latency value in audio FIFO

Table 94. ACR_CTS_x registers (address 05h to 07h) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
07h	ACR_CTS_2	7 to 4	x	R/W	0000*	undefined
		3 to 0	CTS[19:16]	R/W	0000*	**CTS:** audio clock recovery CTS value for manual CTS settings
06h	ACR_CTS_1	7 to 0	CTS[15:8]	R/W	69h*	
05h	ACR_CTS_0	7 to 0	CTS[7:0]	R/W	78h*	

Table 95. ACR_N_x registers (address 08h to 0Ah) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	ACR_N_2	7 to 4	x	R/W	0000*	undefined
		3 to 0	N[19:16]	R/W	0000*	**N:** audio clock recovery N value for manual N-settings
09h	ACR_N_1	7 to 0	N[15:8]	R/W	60h*	
08h	ACR_N_0	7 to 0	N[7:0]	R/W	00h*	

Table 96. GC_AVMUTE register (address 0Bh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 2	x	R/W	0000 00*	undefined
1	SET_MUTE	R/W		**set mute:** GCP.SB0 (bit 0)
			0*	no specific action
			1	set AVMUTE flag
0	CLR_MUTE	R/W		**clear mute:** GCP.SB0 (bit 4)
			0*	no specific action
			1	clear AVMUTE flag

Table 97. CTS_N register (address 0Ch) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 6	x	R/W	00*	undefined
5 to 4	M_SEL[1:0]	R/W		**M select:** postdivider mts (measured time stamp)
			00*	CTS = mts
			01	CTS = mts / 2
			10	CTS = mts / 4
			11	CTS = mts / 8
3	x	R/W	0*	undefined
2 to 0	K_SEL[2:0]	R/W		**K select:** predivider (scales n)
			000*	k = 1
			001	k = 2
			010	k = 3
			011	k = 4
			1XX	k = 8

Table 98. ENC_CNTRL register (address 0Dh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 4	x	R/W	0000*	undefined

Table 98. ENC_CNTRL register (address 0Dh) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
3 to 2	CTL_CODE[1:0]	R/W		**control code:** force CTL[1:0]
			00	CTL[1:0] = 00 (DVI mode)
			01*	CTL[1:0] = 01 (advised to use in case of HDMI mode)
			10	CTL[1:0] = 10 (only for debugging purposes)
			11	CTL[1:0] = 11 (only for debugging purposes)
1 to 0	DC_CTL[1:0]	R/W		**disparity counter control**
			00*	video guard band initializes disparity_cnt
			01	video_data_enable enables disparity_cnt
			10	free-running disparity_cnt
			11	undefined

Table 99. DIP_FLAGS register (address 0Eh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	FORCE_NULL	R/W		**force null**
			0*	no specific action
			1	insert null-packets continuously
6	NULL	R/W		**null**
			0*	no specific action
			1	insert one null-packet (this bit is reset by internal control)
5	-	R/W		**-:** data packet header/contents as specified by registers 80h to 9Eh
			0*	no specific action
			1	insert InfoFrame in first free slot after the keepout window
4	ACP	R/W		**audio content protection:** data packet header/contents as specified by registers 60h to 7Eh (see Table 105)
			0*	no specific action
			1	insert 'acp' in first free slot after the keepout window
3	ISRC2	R/W		**international standard recording code 2:** data packet header/contents as specified by registers 40h to 5Eh (see Table 104)
			0*	no specific action
			1	insert 'isrc2' in first free slot after the keepout window

Table 99. DIP_FLAGS register (address 0Eh) bit description *...continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
2	ISRC1	R/W		**international standard recording code 1:** data packet header/contents as specified by registers 20h to 3Eh (see Table 103)
			0*	no specific action
			1	insert 'isrc1' in first free slot after the keepout window
1	GC	R/W		**general control**
			0*	no specific action
			1	insert general control packet (just after v-pulse)
0	ACR	R/W		**audio clock regeneration**
			0*	no specific action
			1	insert audio clock regeneration packets

Table 100. DIP_IF_FLAGS register (address 0Fh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 6	x	R/W	00*	undefined
5	IF5	R/W		**if5:** data packet header/contents as specified by registers A0h to BEh (page 10h)
			0*	no specific action
			1	insert 'if5' in first free slot after the keepout window
4	IF4	R/W		**if4:** data packet header/contents as specified by registers 80h to 9Eh (page 10h)
			0*	no specific action
			1	insert 'if4' in first free slot after the keepout window
3	IF3	R/W		**if3:** data packet header/contents as specified by registers 60h to 7Eh (page 10h)
			0*	no specific action
			1	insert 'if3' in first free slot after the keepout window
2	IF2	R/W		**if2:** data packet header/contents as specified by registers 40h to 5Eh (page 10h)
			0*	no specific action
			1	insert 'if2' in first free slot after the keepout window
1	IF1	R/W		**if1:** data packet header/contents as specified by registers 20h to 3Eh (page 10h)
			0*	no specific action
			1	insert 'if1' in first free slot after the keepout window
0	x	R/W	0*	undefined

Table 101. CH_STAT_B_x channel status bytes 0, 1, 3 and 4 registers (address 14h to 17h) bit description
*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
						channel status byte x: x = 0 to 4
14h	CH_STAT_B_0	7 to 0	CH_STAT_BYTE_0[7:0]	R/W	00h*	byte 0
15h	CH_STAT_B_1	7 to 0	CH_STAT_BYTE_1[7:0]	R/W	00h*	byte 1
16h	CH_STAT_B_3	7 to 0	CH_STAT_BYTE_3[7:0]	R/W	00h*	byte 3
17h	CH_STAT_B_4	7 to 0	CH_STAT_BYTE_4[7:0]	R/W	00h*	byte 4

Table 102. CH_STAT_B_2_APx_n channel status byte 2 registers (address 18h to 1Fh) bit description
*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
						channel status byte 2 of audio port x: x = 0 to 3
18h	CH_STAT_B_2_AP0_L	7 to 0	CH_STAT_BYTE_2_AP0_L[7:0]	R/W	00h*	audio port 0 left
19h	CH_STAT_B_2_AP0_R	7 to 0	CH_STAT_BYTE_2_AP0_R[7:0]	R/W	00h*	audio port 0 right
1Ah	CH_STAT_B_2_AP1_L	7 to 0	CH_STAT_BYTE_2_AP1_L[7:0]	R/W	00h*	audio port 1 left
1Bh	CH_STAT_B_2_AP1_R	7 to 0	CH_STAT_BYTE_2_AP1_R[7:0]	R/W	00h*	audio port 1 right
1Ch	CH_STAT_B_2_AP2_L	7 to 0	CH_STAT_BYTE_2_AP2_L[7:0]	R/W	00h*	audio port 2 left
1Dh	CH_STAT_B_2_AP2_R	7 to 0	CH_STAT_BYTE_2_AP2_R[7:0]	R/W	00h*	audio port 2 right
1Eh	CH_STAT_B_2_AP3_L	7 to 0	CH_STAT_BYTE_2_AP3_L[7:0]	R/W	00h*	audio port 3 left
1Fh	CH_STAT_B_2_AP3_R	7 to 0	CH_STAT_BYTE_2_AP3_R[7:0]	R/W	00h*	audio port 3 right

9.7.2 ISRC packets registers

Below is an example of use. Please refer to *HDMI 1.2a specification* for the correct definition of data bytes.

See *HDMI 1.2a specification, section 8.8* for rules regarding the use of the ISRC packets.

Table 103. ISRC1 packet registers (address 20h to 3Eh) bit description
*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
20h	ISRC1_PACKET_TYPE	7 to 0	ISRC1_PACKET_TYPE[7:0]	R/W	05h*	**ISRC1 packet type:** packet type of the ISRC1 packet
21h	ISRC1_CTRL	7	ISRC_CONT	R/W	0*	**ISRC continued**: ISRC continued in next packet
		6	ISRC_VALID	R/W	0*	**ISRC valid**: ISRC status and data are valid
		5 to 3	ISRC1_RSVD[5:3]	R/W	000*	**ISRC1 reserved:** reserved (shall be zero)
		2 to 0	ISRC_STATUS[2:0]	R/W	000*	**ISRC status**
					001	starting position
					010	intermediate position
					100	ending position

Table 103. ISRC1 packet registers (address 20h to 3Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
22h	ISRC1_RSVD	7 to 0	ISRC1_RSVD[7:0]	R/W	00h*	**ISRC1 reserved:** reserved (shall be zero)
						ISRC1 data byte x: x = 0 to 15
23h	UPC_EAN_ISRC_0	7 to 0	UPC_EAN_ISRC_0[7:0]	R/W	00h*	UPC/EAN or ISRC byte 0
24h	UPC_EAN_ISRC_1	7 to 0	UPC_EAN_ISRC_1[7:0]	R/W	00h*	UPC/EAN or ISRC byte 1
25h	UPC_EAN_ISRC_2	7 to 0	UPC_EAN_ISRC_2[7:0]	R/W	00h*	UPC/EAN or ISRC byte 2
26h	UPC_EAN_ISRC_3	7 to 0	UPC_EAN_ISRC_3[7:0]	R/W	00h*	UPC/EAN or ISRC byte 3
27h	UPC_EAN_ISRC_4	7 to 0	UPC_EAN_ISRC_4[7:0]	R/W	00h*	UPC/EAN or ISRC byte 4
28h	UPC_EAN_ISRC_5	7 to 0	UPC_EAN_ISRC_5[7:0]	R/W	00h*	UPC/EAN or ISRC byte 5
29h	UPC_EAN_ISRC_6	7 to 0	UPC_EAN_ISRC_6[7:0]	R/W	00h*	UPC/EAN or ISRC byte 6
2Ah	UPC_EAN_ISRC_7	7 to 0	UPC_EAN_ISRC_7[7:0]	R/W	00h*	UPC/EAN or ISRC byte 7
2Bh	UPC_EAN_ISRC_8	7 to 0	UPC_EAN_ISRC_8[7:0]	R/W	00h*	UPC/EAN or ISRC byte 8
2Ch	UPC_EAN_ISRC_9	7 to 0	UPC_EAN_ISRC_9[7:0]	R/W	00h*	UPC/EAN or ISRC byte 9
2Dh	UPC_EAN_ISRC_10	7 to 0	UPC_EAN_ISRC_10[7:0]	R/W	00h*	UPC/EAN or ISRC byte 10
2Eh	UPC_EAN_ISRC_11	7 to 0	UPC_EAN_ISRC_11[7:0]	R/W	00h*	UPC/EAN or ISRC byte 11
2Fh	UPC_EAN_ISRC_12	7 to 0	UPC_EAN_ISRC_12[7:0]	R/W	00h*	UPC/EAN or ISRC byte 12
30h	UPC_EAN_ISRC_13	7 to 0	UPC_EAN_ISRC_13[7:0]	R/W	00h*	UPC/EAN or ISRC byte 13
31h	UPC_EAN_ISRC_14	7 to 0	UPC_EAN_ISRC_14[7:0]	R/W	00h*	UPC/EAN or ISRC byte 14
32h	UPC_EAN_ISRC_15	7 to 0	UPC_EAN_ISRC_15[7:0]	R/W	00h*	UPC/EAN or ISRC byte 15
						ISRC1 data byte x: x = 16 to 27
33h	ISRC1_PB16	7 to 0	ISRC1_PB_BYTE_16[7:0]	R/W	00h*	reserved byte 16 (shall be set to a value of 0)
34h	ISRC1_PB17	7 to 0	ISRC1_PB_BYTE_17[7:0]	R/W	00h*	reserved byte 17 (shall be set to a value of 0)
35h	ISRC1_PB18	7 to 0	ISRC1_PB_BYTE_18[7:0]	R/W	00h*	reserved byte 18 (shall be set to a value of 0)
36h	ISRC1_PB19	7 to 0	ISRC1_PB_BYTE_19[7:0]	R/W	00h*	reserved byte 19 (shall be set to a value of 0)
37h	ISRC1_PB20	7 to 0	ISRC1_PB_BYTE_20[7:0]	R/W	00h*	reserved byte 20 (shall be set to a value of 0)
38h	ISRC1_PB21	7 to 0	ISRC1_PB_BYTE_21[7:0]	R/W	00h*	reserved byte 21 (shall be set to a value of 0)
39h	ISRC1_PB22	7 to 0	ISRC1_PB_BYTE_22[7:0]	R/W	00h*	reserved byte 22 (shall be set to a value of 0)
3Ah	ISRC1_PB23	7 to 0	ISRC1_PB_BYTE_23[7:0]	R/W	00h*	reserved byte 23 (shall be set to a value of 0)
3Bh	ISRC1_PB24	7 to 0	ISRC1_PB_BYTE_24[7:0]	R/W	00h*	reserved byte 24 (shall be set to a value of 0)
3Ch	ISRC1_PB25	7 to 0	ISRC1_PB_BYTE_25[7:0]	R/W	00h*	reserved byte 25 (shall be set to a value of 0)
3Dh	ISRC1_PB26	7 to 0	ISRC1_PB_BYTE_26[7:0]	R/W	00h*	reserved byte 26 (shall be set to a value of 0)
3Eh	ISRC1_PB27	7 to 0	ISRC1_PB_BYTE_27[7:0]	R/W	00h*	reserved byte 27 (shall be set to a value of 0)

Table 104. ISRC2 packet registers (address 40h to 5Eh) bit description

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
40h	ISRC2_PACKET_TYPE	7 to 0	ISRC2_PACKET_TYPE[7:0]	R/W	06h*	**ISRC2 packet type:** packet type of the ISRC2 packet
41h	ISRC2_RSVD1	7 to 0	ISRC2_RSVD1[7:0]	R/W	00h*	**ISRC2 reserved 1:** reserved (shall be zero)
42h	ISRC2_RSVD2	7 to 0	ISRC2_RSVD2[7:0]	R/W	00h*	**ISRC2 reserved 2:** reserved (shall be zero)
						ISRC2 data byte x: x = 0 to 15
43h	UPC_EAN_ISRC_16	7 to 0	UPC_EAN_ISRC_16[7:0]	R/W	00h*	UPC/EAN or ISRC byte 16
44h	UPC_EAN_ISRC_17	7 to 0	UPC_EAN_ISRC_17[7:0]	R/W	00h*	UPC/EAN or ISRC byte 17
45h	UPC_EAN_ISRC_18	7 to 0	UPC_EAN_ISRC_18[7:0]	R/W	00h*	UPC/EAN or ISRC byte 18
46h	UPC_EAN_ISRC_19	7 to 0	UPC_EAN_ISRC_19[7:0]	R/W	00h*	UPC/EAN or ISRC byte 19
47h	UPC_EAN_ISRC_20	7 to 0	UPC_EAN_ISRC_20[7:0]	R/W	00h*	UPC/EAN or ISRC byte 20
48h	UPC_EAN_ISRC_21	7 to 0	UPC_EAN_ISRC_21[7:0]	R/W	00h*	UPC/EAN or ISRC byte 21
49h	UPC_EAN_ISRC_22	7 to 0	UPC_EAN_ISRC_22[7:0]	R/W	00h*	UPC/EAN or ISRC byte 22
4Ah	UPC_EAN_ISRC_23	7 to 0	UPC_EAN_ISRC_23[7:0]	R/W	00h*	UPC/EAN or ISRC byte 23
4Bh	UPC_EAN_ISRC_24	7 to 0	UPC_EAN_ISRC_24[7:0]	R/W	00h*	UPC/EAN or ISRC byte 24
4Ch	UPC_EAN_ISRC_25	7 to 0	UPC_EAN_ISRC_25[7:0]	R/W	00h*	UPC/EAN or ISRC byte 25
4Dh	UPC_EAN_ISRC_26	7 to 0	UPC_EAN_ISRC_26[7:0]	R/W	00h*	UPC/EAN or ISRC byte 26
4Eh	UPC_EAN_ISRC_27	7 to 0	UPC_EAN_ISRC_27[7:0]	R/W	00h*	UPC/EAN or ISRC byte 27
4Fh	UPC_EAN_ISRC_28	7 to 0	UPC_EAN_ISRC_28[7:0]	R/W	00h*	UPC/EAN or ISRC byte 28
50h	UPC_EAN_ISRC_29	7 to 0	UPC_EAN_ISRC_29[7:0]	R/W	00h*	UPC/EAN or ISRC byte 29
51h	UPC_EAN_ISRC_30	7 to 0	UPC_EAN_ISRC_30[7:0]	R/W	00h*	UPC/EAN or ISRC byte 30
52h	UPC_EAN_ISRC_31	7 to 0	UPC_EAN_ISRC_31[7:0]	R/W	00h*	UPC/EAN or ISRC byte 31
						ISRC2 data byte x: x = 16 to 27
53h	ISRC2_PB16	7 to 0	ISRC2_PB_BYTE_16[7:0]	R/W	00h*	reserved byte 16 (shall be set to a value of 0)
54h	ISRC2_PB17	7 to 0	ISRC2_PB_BYTE_17[7:0]	R/W	00h*	reserved byte 17 (shall be set to a value of 0)
55h	ISRC2_PB18	7 to 0	ISRC2_PB_BYTE_18[7:0]	R/W	00h*	reserved byte 18 (shall be set to a value of 0)
56h	ISRC2_PB19	7 to 0	ISRC2_PB_BYTE_19[7:0]	R/W	00h*	reserved byte 19 (shall be set to a value of 0)
57h	ISRC2_PB20	7 to 0	ISRC2_PB_BYTE_20[7:0]	R/W	00h*	reserved byte 20 (shall be set to a value of 0)
58h	ISRC2_PB21	7 to 0	ISRC2_PB_BYTE_21[7:0]	R/W	00h*	reserved byte 21 (shall be set to a value of 0)
59h	ISRC2_PB22	7 to 0	ISRC2_PB_BYTE_22[7:0]	R/W	00h*	reserved byte 22 (shall be set to a value of 0)
5Ah	ISRC2_PB23	7 to 0	ISRC2_PB_BYTE_23[7:0]	R/W	00h*	reserved byte 23 (shall be set to a value of 0)
5Bh	ISRC2_PB24	7 to 0	ISRC2_PB_BYTE_24[7:0]	R/W	00h*	reserved byte 24 (shall be set to a value of 0)

Table 104. ISRC2 packet registers (address 40h to 5Eh) bit description *…continued*
*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
5Ch	ISRC2_PB25	7 to 0	ISRC2_PB_BYTE_25[7:0]	R/W	00h*	reserved byte 25 (shall be set to a value of 0)
5Dh	ISRC2_PB26	7 to 0	ISRC2_PB_BYTE_26[7:0]	R/W	00h*	reserved byte 26 (shall be set to a value of 0)
5Eh	ISRC2_PB27	7 to 0	ISRC2_PB_BYTE_27[7:0]	R/W	00h*	reserved byte 27 (shall be set to a value of 0)

9.7.3 Audio content protection packet registers

Below is an example of use. Please refer to *HDMI 1.2a specification* for the correct definition of data bytes.

See *HDMI 1.2a specification, section 9.3* for rules regarding the use of ACP packets.

Table 105. ACP packet registers (address 60h to 7Eh) bit description
*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
60h	ACP_ PACKET_ TYPE	7 to 0	ACP_PACKET_ TYPE[7:0]	R/W	04h*	**audio content protection packet type**: packet type of the audio content protection packet
61h	ACP_TYPE	7 to 0	ACP_TYPE[7:0]	R/W	00h*	**audio content protection type:** content protection type
62h	ACP_RSVD	7 to 0	ACP_RSVD[7:0]	R/W	00h*	**audio content protection reserved:** reserved (shall be zero)
63h	ACP_PB0	7 to 0	ACP_PB_BYTE_0[7:0]	R/W	00h*	**audio content protection data byte 0**
						ACP_TYPE = 2: DVD-audio DVD-Audio_Type_Dependent_ Generation [8 bits] identifies the generation of the DVD-Audio-specific ACP_Type_ Dependent fields. Shall be set to logic 1.
						ACP_TYPE = 3: super audio CD CCI_1_b0[7:0]

Table 105. ACP packet registers (address 60h to 7Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
						audio content protection data byte 1
64h	ACP_PB1	7 to 6	ACP_PB_BYTE_1[7:6]	R/W	00*	ACP_TYPE = 2: DVD audio Copy_Permission[1:0] = audio_copy_permission parameter
						ACP_TYPE = 3: super audio CD CCI_1_b1[7:6]
		5 to 3	ACP_PB_BYTE_1[5:3]	R/W	000*	ACP_TYPE = 2: DVD audio Copy_Number[2:0] = audio_copy_number parameter
						ACP_TYPE = 3: super audio CD CCI_1_b1[5:3]
		2 to 1	ACP_PB_BYTE_1[2:1]	R/W	00*	ACP_TYPE = 2: DVD audio Quality[1:0] = audio_quality parameter
						ACP_TYPE = 3: super audio CD CCI_1_b1[2:1]
		0	ACP_PB_BYTE_1[0]	R/W	0*	ACP_TYPE = 2: DVD audio Transaction = audio_transaction parameter
						ACP_TYPE = 3: super audio CD CCI_1_b1[0]
65h	ACP_PB2	7 to 0	ACP_PB_BYTE_2[7:0]	R/W	00h*	**audio content protection data byte 2**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b2[7:0]
66h	ACP_PB3	7 to 0	ACP_PB_BYTE_3[7:0]	R/W	00h*	**audio content protection data byte 3**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b3[7:0]
67h	ACP_PB4	7 to 0	ACP_PB_BYTE_4[7:0]	R/W	00h*	**audio content protection data byte 4**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b4[7:0]
68h	ACP_PB5	7 to 0	ACP_PB_BYTE_5[7:0]	R/W	00h*	**audio content protection data byte 5**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b5[7:0]

Table 105. ACP packet registers (address 60h to 7Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
69h	ACP_PB6	7 to 0	ACP_PB_BYTE_6[7:0]	R/W	00h*	**audio content protection data byte 6**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b6[7:0]
6Ah	ACP_PB7	7 to 0	ACP_PB_BYTE_7[7:0]	R/W	00h*	**audio content protection data byte 7**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b7[7:0]
6Bh	ACP_PB8	7 to 0	ACP_PB_BYTE_8[7:0]	R/W	00h*	**audio content protection data byte 8**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b8[7:0]
6Ch	ACP_PB9	7 to 0	ACP_PB_BYTE_9[7:0]	R/W	00h*	**audio content protection data byte 9**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b9[7:0]
6Dh	ACP_PB10	7 to 0	ACP_PB_BYTE_10[7:0]	R/W	00h*	**audio content protection data byte 10**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b10[7:0]
6Eh	ACP_PB11	7 to 0	ACP_PB_BYTE_11[7:0]	R/W	00h*	**audio content protection data byte 11**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b11[7:0]
6Fh	ACP_PB12	7 to 0	ACP_PB_BYTE_12[7:0]	R/W	00h*	**audio content protection data byte 12**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b12[7:0]
70h	ACP_PB13	7 to 0	ACP_PB_BYTE_13[7:0]	R/W	00h*	**audio content protection data byte 13**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b13[7:0]

Table 105. ACP packet registers (address 60h to 7Eh) bit description *…continued*

*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
71h	ACP_PB14	7 to 0	ACP_PB_BYTE_14[7:0]	R/W	00h*	**audio content protection data byte 14**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b14[7:0]
72h	ACP_PB15	7 to 0	ACP_PB_BYTE_15[7:0]	R/W	00h*	**audio content protection data byte 15**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b15[7:0]
73h	ACP_PB16	7 to 0	ACP_PB_BYTE_16[7:0]	R/W	00h*	**audio content protection data byte 16**
						ACP_TYPE = 2: DVD audio reserved (0)
						ACP_TYPE = 3: super audio CD CCI_1_b16[7:0]
74h	ACP_PB17	7 to 0	ACP_PB_BYTE_17[7:0]	R/W	00h*	**audio content protection data byte 17**
						ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)
75h	ACP_PB18	7 to 0	ACP_PB_BYTE_18[7:0]	R/W	00h*	**audio content protection data byte 18**
						ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)
76h	ACP_PB19	7 to 0	ACP_PB_BYTE_19[7:0]	R/W	00h*	**audio content protection data byte 19**
						ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)
77h	ACP_PB20	7 to 0	ACP_PB_BYTE_20[7:0]	R/W	00h*	**audio content protection data byte 20**
						ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)
78h	ACP_PB21	7 to 0	ACP_PB_BYTE_21[7:0]	R/W	00h*	**audio content protection data byte 21**
						ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)
79h	ACP_PB22	7 to 0	ACP_PB_BYTE_22[7:0]	R/W	00h*	**audio content protection data byte 22**
						ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)

Table 105. ACP packet registers (address 60h to 7Eh) bit description *…continued*
*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
7Ah	ACP_PB23	7 to 0	ACP_PB_BYTE_23[7:0]	R/W	00h*	**audio content protection data byte 23** ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)
7Bh	ACP_PB24	7 to 0	ACP_PB_BYTE_24[7:0]	R/W	00h*	**audio content protection data byte 24** ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)
7Ch	ACP_PB25	7 to 0	ACP_PB_BYTE_25[7:0]	R/W	00h*	**audio content protection data byte 25** ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)
7Dh	ACP_PB26	7 to 0	ACP_PB_BYTE_26[7:0]	R/W	00h*	**audio content protection data byte 26** ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)
7Eh	ACP_PB27	7 to 0	ACP_PB_BYTE_27[7:0]	R/W	00h*	**audio content protection data byte 27** ACP_TYPE = 2: DVD audio or ACP_TYPE = 3: super audio CD reserved (0)

9.7.4 Current page address register

Table 106. CURPAGE_ADR register (address FFh) bit description
*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	CURPAGE_ADR[7:0]	W	00h*	**current page address:** selects the current memory page

9.8 HDMI and DVI page register definitions

The current page address for the HDMI and DVI page is 12h.

The configuration of the registers for this page is given in Table 107.

Table 107. I²C-bus registers of memory page 12h[1]

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
Not used	00h	-	-								0000 0000
:	:	:	:								:
Not used	B7h	-	-								0000 0000
HDCP_TX33	B8h	R/W	x	x	x	x	x	x	HDMI	x	0000 0000
Not used	B9h	-	-								0000 0000
:	:	:	:								:
Not used	FEh	-	-								0000 0000
CURPAGE_ADR	FFh	W	CURPAGE_ADR[7:0]								0000 0000

[1] R: reading register
W: writing register
x: bit must be set to default value for proper operation
-: not used

9.8.1 HDMI control registers

Table 108. HDCP_TX33 register (address B8h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 6	x	R/W	0000 00*	undefined
1	HDMI	R/W		**HDMI**
			0*	DVI mode
			1	HDMI mode
0	x	R/W	0*	undefined

9.8.2 Current page address register

Table 109. CURPAGE_ADR register (address FFh) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	CURPAGE_ADR[7:0]	W	00h*	**current page address:** selects the current memory page

10. Limiting values

Table 110. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		–0.5	+4.6	V
$V_{DD(1V8)}$	supply voltage (1.8 V)		–0.5	+2.5	V
ΔV_{DD}	supply voltage difference		–0.5	+0.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		-	125	°C
V_{esd}	electrostatic discharge voltage	HBM	–1500	+1500	V

11. Thermal characteristics

Table 111. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC 4L board	26.5	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		10.2	K/W

12. Static characteristics

Table 112. Supplies

$V_{DDA(FRO\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(PLL\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(3V3)}$ = 3.0 V to 3.6 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; V_{PP} = 0 V; T_{amb} = 0 °C to 70 °C.
Typical values are measured at $V_{DDA(FRO\_3V3)}$ = $V_{DDA(PLL\_3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V; $V_{DDC(1V8)}$ = 1.8 V; V_{PP} = 0 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TDA9983BHW/8 and TDA9983BHW/15							
$V_{DDA(FRO\_3V3)}$	free running oscillator 3.3 V analog supply voltage			3.0	3.3	3.6	V
$V_{DDA(PLL\_3V3)}$	PLL 3.3 V analog supply voltage			3.0	3.3	3.6	V
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)		[1]	3.0	3.3	3.6	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		[1]	1.65	1.8	1.95	V
TDA9983BHW/8; up to 81 MHz							
$I_{DDA(FRO\_3V3)}$	free running oscillator 3.3 V analog supply current			-	0	1	mA
$I_{DDA(PLL\_3V3)}$	PLL 3.3 V analog supply current		[2]	-	4.5	6	mA
$I_{DDD(3V3)}$	digital supply current (3.3 V)			-	-	5	mA
$I_{DDH(3V3)}$	HDMI supply current (3.3 V)			-	14	16.5	mA
$I_{DDC(1V8)}$	core supply current (1.8 V)		[2]	-	154.5	200	mA
$f_{clk(max)}$	maximum clock frequency		[3]	81	-	-	MHz
P_{cons}	power consumption		[3]	-	322	-	mW
		worst case	[2]	-	338	503	mW
P_{tot}	total power dissipation		[3]	-	458	-	mW
		worst case	[2]	-	472	651	mW
P_{pd}	power dissipation in power-down mode			-	13.5	38.4	mW
TDA9983BHW/15; up to 150 MHz							
$I_{DDA(FRO\_3V3)}$	free running oscillator 3.3 V analog supply current			-	0	1	mA
$I_{DDA(PLL\_3V3)}$	PLL 3.3 V analog supply current		[4]	-	4	5	mA
$I_{DDD(3V3)}$	digital supply current (3.3 V)			-	-	5	mA
$I_{DDH(3V3)}$	HDMI supply current (3.3 V)			-	14	16.5	mA
$I_{DDC(1V8)}$	core supply current (1.8 V)		[4]	-	167	210	mA
$f_{clk(max)}$	maximum clock frequency		[4]	150	-	-	MHz
P_{cons}	power consumption		[4]	-	361	583	mW
P_{tot}	total power dissipation		[4]	-	495	732	mW
P_{pd}	power dissipation in power-down mode			-	13.5	38.4	mW

[1] The $V_{DDD(3V3)}$ and $V_{DDC(1V8)}$ power supplies must always follow the sequence shown in Figure 14 to ensure proper power-up conditions.

[2] Worst case video format:
  a) Input 480p (YC_BC_R 4 : 2 : 2 semi-planar)
  b) Output 720p (YC_BC_R 4 : 2 : 2)

[3] Video format:
  a) Input 480p (ITU656 embedded sync, rising edge)
  b) Output 1080i (YC_BC_R 4 : 2 : 2)

[4] Video format:
  a) Input 1080p (RGB 4 : 4 : 4 external sync, rising edge)

b) Output 1080p (RGB 4 : 4 : 4)

Table 113. LV-TTL digital inputs and outputs

$V_{DDA(FRO\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(PLL\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(3V3)}$ = 3.0 V to 3.6 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; V_{PP} = 0 V; T_{amb} = 0 °C to 70 °C.
Typical values are measured at $V_{DDA(FRO\_3V3)}$ = $V_{DDA(PLL\_3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V; $V_{DDC(1V8)}$ = 1.8 V; V_{PP} = 0 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Not 5 V tolerant inputs: pins HSYNC, VSYNC, AP[7:0], ACLK, TM, A0, A1, VPA[7:0], VPB[7:0], VPC[7:0], VCLK, DE and RST_N						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
I_{IL}	LOW-level input current		–1	-	+1	µA
I_{IH}	HIGH-level input current		–1	-	+1	µA
C_i	input capacitance		-	4.5	-	pF
5 V tolerant input: pin HPD						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
C_i	input capacitance		-	4.5	-	pF
Output: pin INT						
V_{OL}	LOW-level output voltage	C_L = 10 pF; I_{OL} = 2 mA	-	-	0.4	V

Table 114. TMDS outputs

$V_{DDA(FRO\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(PLL\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(3V3)}$ = 3.0 V to 3.6 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; V_{PP} = 0 V; T_{amb} = 0 °C to 70 °C.
Typical values are measured at $V_{DDA(FRO\_3V3)}$ = $V_{DDA(PLL\_3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V; $V_{DDC(1V8)}$ = 1.8 V; V_{PP} = 0 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS output pins: TX0–, TX0+, TX1–, TX1+, TX2–, TX2+, TXC– and TXC+						
$V_{o(p-p)}$	peak-to-peak output voltage	single output; R_{ext} = 610 Ω (1 % tolerance) with test load and operating condition as in *HDMI 1.2a specification*	400	525	600	mV
V_{OH}	HIGH-level output voltage		3.125	3.3	3.475	V
V_{OL}	LOW-level output voltage		2.535	2.8	3.065	V

13. Dynamic characteristics

Table 115. Timing characteristics

$V_{DDA(FRO\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(PLL\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(3V3)}$ = 3.0 V to 3.6 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; V_{PP} = 0 V; T_{amb} = 0 °C to 70 °C.
Typical values are measured at $V_{DDA(FRO\_3V3)}$ = $V_{DDA(PLL\_3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V; $V_{DDC(1V8)}$ = 1.8 V; V_{PP} = 0 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies: pins $V_{DDC(1V8)}$, $V_{DDD(3V3)}$; see Figure 14						
t_d	delay time		1	-	-	ms
Clock inputs: pins VCLK, VPA[7:0], VPB[7:0], VPC[7:0]; see Figure 15, 16, 17, 18 and 19						
$f_{clk(max)}$	maximum clock frequency	TDA9983BHW/8	81	-	-	MHz
		TDA9983BHW/15	150	-	-	MHz
$t_{su(D)}$	data input set-up time		−1.3	-	-	ns
$t_{h(D)}$	data input hold time		3.6	-	-	ns
δ_{clk}	clock duty cycle		40	-	60	%
DDC I²C-bus; 5 V tolerant; master bus: pins DDC_SDA and DDC_SCL						
f_{SCL}	SCL clock frequency	standard mode	-	-	100	kHz
I²C-bus; 5 V tolerant; master bus: pins I2C_SDA and I2C_SCL						
f_{SCL}	SCL clock frequency	standard mode	-	-	100	kHz
		fast mode	-	-	400	kHz
TMDS output pins: TXC− and TXC+						
$f_{clk(max)}$	maximum clock frequency	TDA9983BHW/8	81	-	-	MHz
		TDA9983BHW/15	150	-	-	MHz
TMDS output pins: TX0−, TX0+, TX1−, TX1+, TX2− and TX2+						
$f_{clk(max)}$	maximum clock frequency	TDA9983BHW/8	810	-	-	MHz
		TDA9983BHW/15	1.5	-	-	GHz

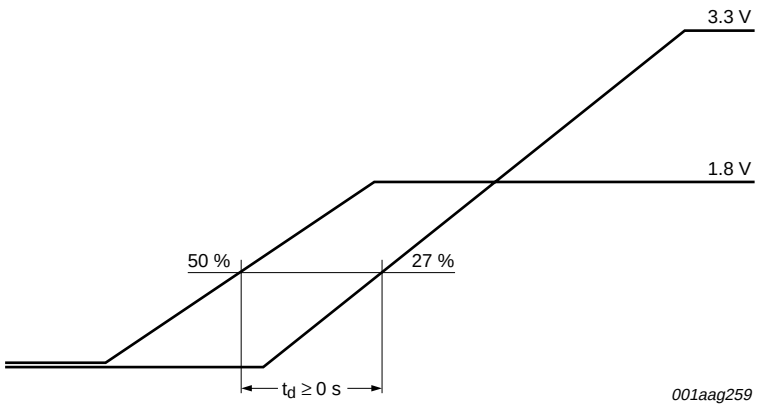


Fig 14. Power supply sequencing

13.1 Input format

In Table 116 the port VPA has been mapped to C_B (YUV space)/B (RGB space), VPB has been mapped to Y (YUV space)/G (RGB space) and VPC has been mapped to C_R (YUV space)/R (RGB space).

Table 116. Input format

Input pins	Signal	RGB	YUV						
		4 : 4 : 4[1]	4 : 4 : 4[2]	4 : 2 : 2 (semi-planar)[3]		4 : 2 : 2: (ITU656-like)[4]			
Video port A									
VPA[0]	C_B[0]/B[0]	B[0]	C_B[0]	Y_0[0]	Y_1[0]	C_B[0]	Y_0[0]	C_R[0]	Y_1[0]
VPA[1]	C_B[1]/B[1]	B[1]	C_B[1]	Y_0[1]	Y_1[1]	C_B[1]	Y_0[1]	C_R[1]	Y_1[1]
VPA[2]	C_B[2]/B[2]	B[2]	C_B[2]	Y_0[2]	Y_1[2]	C_B[2]	Y_0[2]	C_R[2]	Y_1[2]
VPA[3]	C_B[3]/B[3]	B[3]	C_B[3]	Y_0[3]	Y_1[3]	C_B[3]	Y_0[3]	C_R[3]	Y_1[3]
VPA[4]	C_B[4]/B[4]	B[4]	C_B[4]	C_B[0]	C_R[0]	L	L	L	L
VPA[5]	C_B[5]/B[5]	B[5]	C_B[5]	C_B[1]	C_R[1]	L	L	L	L
VPA[6]	C_B[6]/B[6]	B[6]	C_B[6]	C_B[2]	C_R[2]	L	L	L	L
VPA[7]	C_B[7]/B[7]	B[7]	C_B[7]	C_B[3]	C_R[3]	L	L	L	L
Video port B									
VPB[0]	Y[0]/G[0]	G[0]	Y[0]	Y_0[4]	Y_1[4]	C_B[4]	Y_0[4]	C_R[4]	Y_1[4]
VPB[1]	Y[1]/G[1]	G[1]	Y[1]	Y_0[5]	Y_1[5]	C_B[5]	Y_0[5]	C_R[5]	Y_1[5]
VPB[2]	Y[2]/G[2]	G[2]	Y[2]	Y_0[6]	Y_1[6]	C_B[6]	Y_0[6]	C_R[6]	Y_1[6]
VPB[3]	Y[3]/G[3]	G[3]	Y[3]	Y_0[7]	Y_1[7]	C_B[7]	Y_0[7]	C_R[7]	Y_1[7]
VPB[4]	Y[4]/G[4]	G[4]	Y[4]	Y_0[8]	Y_1[8]	C_B[8]	Y_0[8]	C_R[8]	Y_1[8]
VPB[5]	Y[5]/G[5]	G[5]	Y[5]	Y_0[9]	Y_1[9]	C_B[9]	Y_0[9]	C_R[9]	Y_1[9]
VPB[6]	Y[6]/G[6]	G[6]	Y[6]	Y_0[10]	Y_1[10]	C_B[10]	Y_0[10]	C_R[10]	Y_1[10]
VPB[7]	Y[7]/G[7]	G[7]	Y[7]	Y_0[11]	Y_1[11]	C_B[11]	Y_0[11]	C_R[11]	Y_1[11]
Video port C									
VPC[0]	C_R[0]/R[0]	R[0]	C_R[0]	C_B[4]	C_R[4]	L	L	L	L
VPC[1]	C_R[1]/R[1]	R[1]	C_R[1]	C_B[5]	C_R[5]	L	L	L	L
VPC[2]	C_R[2]/R[2]	R[2]	C_R[2]	C_B[6]	C_R[6]	L	L	L	L
VPC[3]	C_R[3]/R[3]	R[3]	C_R[3]	C_B[7]	C_R[7]	L	L	L	L
VPC[4]	C_R[4]/R[4]	R[4]	C_R[4]	C_B[8]	C_R[8]	L	L	L	L
VPC[5]	C_R[5]/R[5]	R[5]	C_R[5]	C_B[9]	C_R[9]	L	L	L	L
VPC[6]	C_R[6]/R[6]	R[6]	C_R[6]	C_B[10]	C_R[10]	L	L	L	L
VPC[7]	C_R[7]/R[7]	R[7]	C_R[7]	C_B[11]	C_R[11]	L	L	L	L

[1] Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

[2] Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

[3] Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

[4] Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

13.2 Example of supported video

The TDA9983B supports all EIA/CEA-861B, ATSC video input formats.

Table 117. Timing parameters for EIA/CEA-861B

Format nr.	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition	Scaler
59.94 Hz systems								
1 (VGA)	640 × 480p	59.9401	800	525	31.4685	25.174825	1	-
2, 3	720 × 480p	59.9401	858	525	31.4685	27	1	X
4	1280 × 720p	59.9401	1650	750	44.955	74.175824	1	-
5	1920 × 1080i	59.9401	2200	1125	33.7163	74.175824	1	-
6, 7 (NTSC)	720 × 480i	59.9401	858	525	15.7343	13.5	2	X
8, 9	720 × 240p	59.9401	858	262	15.7043	13.474286	2	-
8, 9	720 × 240p	59.9401	858	263	15.7642	13.525714	2	-
10, 11	720 × 480i	59.9401	858	525	15.7343	13.5	4, 5, 7[1], 8[1], 10[1]	-
12, 13	720 × 240p	59.9401	858	262	15.7043	13.474286	4, 5, 7[1], 8[1], 10[1]	-
12, 13	720 × 240p	59.9401	858	263	15.7642	13.525714	4, 5, 7[1], 8[1], 10[1]	-
14, 15	1440 × 480p	59.9401	1716	525	31.4685	54	2	-
16[1]	1920 × 1080p	59.9401	2200	1125	67.4326	148.35165[1]	1	-
60 Hz systems								
1 (VGA)	640 × 480p	60	800	525	31.5	25.2	1	-
2, 3	720 × 480p	60	858	525	31.5	27.27	1	X
4	1280 × 720p	60	1650	750	45	74.25	1	-
5	1920 × 1080i	60	2200	1125	33.75	74.25	1	-
6, 7 (NTSC)	720 × 480i	60	858	525	15.75	13.5135	2	X
8, 9	720 × 240p	60	858	262	15.72	13.48776	2	-
8, 9	720 × 240p	60	858	263	15.78	13.53924	2	-
10, 11	720 × 480i	60	858	525	15.75	13.5135	4, 5, 7[1], 8[1], 10[1]	-
12, 13	720 × 240p	60	858	262	15.72	13.48776	4, 5, 7[1], 8[1], 10[1]	-
12, 13	720 × 240p	60	858	263	15.78	13.53924	4, 5, 7[1], 8[1], 10[1]	-
14, 15	1440 × 480p	60	1716	525	31.5	54.054	2	-
16[1]	1920 × 1080p	60	2200	1125	67.5	148.5[1]	1	-
50 Hz systems								
17, 18	720 × 576p	50	864	625	31.25	27	1	X
19	1280 × 720p	50	1980	750	37.5	74.25	1	-
20	1920 × 1080i	50	2640	1125	28.125	74.25	1	-
21, 22 (PAL)	720 × 576i	50	864	625	15.625	13.5	1	X
23, 24	720 × 288p	50	864	312	15.6	13.4784	2	-
23, 24	720 × 288p	50	864	313	15.65	13.5216	2	-

Table 117. Timing parameters for EIA/CEA-861B *…continued*

Format nr.	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition	Scaler
23, 24	720 × 288p	50	864	314	15.7	13.5648	2	-
25, 26	720 × 576i	50	864	625	15.625	13.5	4, 5, 7[1], 8[1], 10[1]	-
27, 28	720 × 288p	50	864	312	15.6	13.4784	4, 5, 7[1], 8[1], 10[1]	-
27, 28	720 × 288p	50	864	313	15.65	13.5216	4, 5, 7[1], 8[1], 10[1]	-
27, 28	720 × 288p	50	864	314	15.7	13.5648	2	-
29, 30	1440 × 576p	50	1728	625	31.25	54	1	-
31[1]	1920 × 1080p	50	2640	1125	56.25	148.5[1]	1	-
Various systems								
32	1920 × 1080p	23.976	2750	1125	26.973	74.175824	1	-
32	1920 × 1080p	24	2750	1125	27	74.25	1	-
33	1920 × 1080p	25	2640	1125	28.125	74.25	1	-
34	1920 × 1080p	29.97	2200	1125	33.716	74.175824	1	-
34	1920 × 1080p	30	2200	1125	33.75	74.25	1	-

[1] Only for TDA9983BHW/15.

Table 118. Timing parameters for PC standards below 150 MHz

Standard	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition	Scaler
VGA	640 × 350p	85.08	832	445	37.8606	31.5000192	-	-
	640 × 400p	85.08	832	445	37.8606	31.5000192	-	-
	720 × 400p	85.039	936	446	37.927394	35.50004078	-	-
	640 × 480p	59.94005994	800	525	31.46853147	25.17482517	-	-
	640 × 480p	72.809	832	520	37.86068	31.50008576	-	-
	640 × 480p	75	840	500	37.5	31.5	-	-
	640 × 480p	85.008	832	509	43.269072	35.9998679	-	-
SVGA	800 × 600p	56.250	1024	625	35.15625	36	-	-
	800 × 600p	60.317	1056	628	37.879076	40.00030426	-	-
	800 × 600p	72.188	1040	666	48.077208	50.00029632	-	-
	800 × 600p	75.000	1056	625	46.875	49.5	-	-
	800 × 600p	85.061	1048	631	53.673491	56.24981857	-	-

Table 118. Timing parameters for PC standards below 150 MHz *…continued*

Standard	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition	Scaler
XGA	1024 × 786p	60.004	1344	806	48.363224	65.00017306	-	-
	1024 × 786p	70.069	1328	806	56.475614	74.99961539	-	-
	1024 × 786p	75.029	1312	800	60.0232	78.7504384	-	-
	1024 × 786p[1]	84.997	1376	808	68.677576	94.50034458	-	-
	1024 × 786i	86.957	1264	817	35.5219345	44.89972521	-	-
	1152 × 864p[1]	75.000	1600	900	67.5	108	-	-
	1152 × 864p[1]	84.999	1576	907	77.094093	121.5002906	-	-
	1280 × 960p[1]	60	1800	1000	60	108	-	-
	1280 × 960p[1]	85.002	1728	1011	85.937022	148.499174	-	-
SXGA[1]	1280 × 1024p[1]	60.020	1688	1066	63.98132	108.0004682	-	-
	1280 × 1024p[1]	75.025	1688	1066	79.97665	135.0005852	-	-

[1] Only for TDA9983BHW/15.

13.3 Timing diagrams

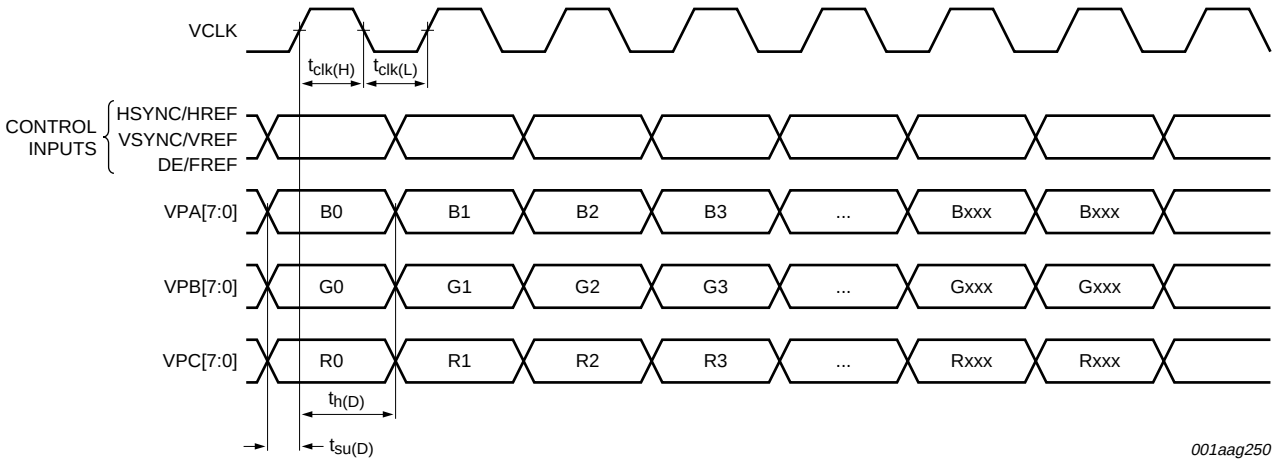


Fig 15. Timing in RGB 4 : 4 : 4 (rising edge) input

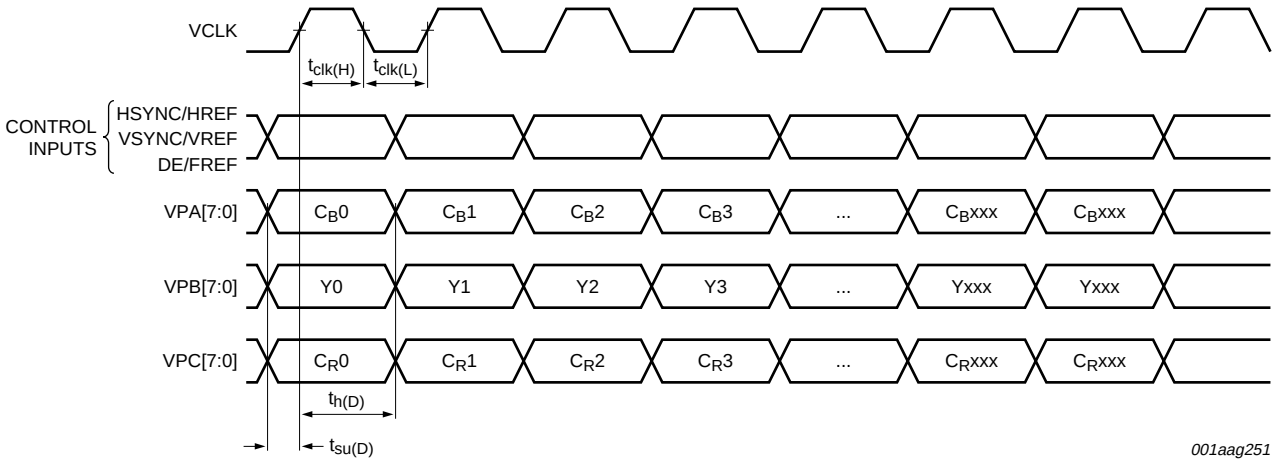


Fig 16. Timing in YC_BC_R 4 : 4 : 4 (rising edge) input

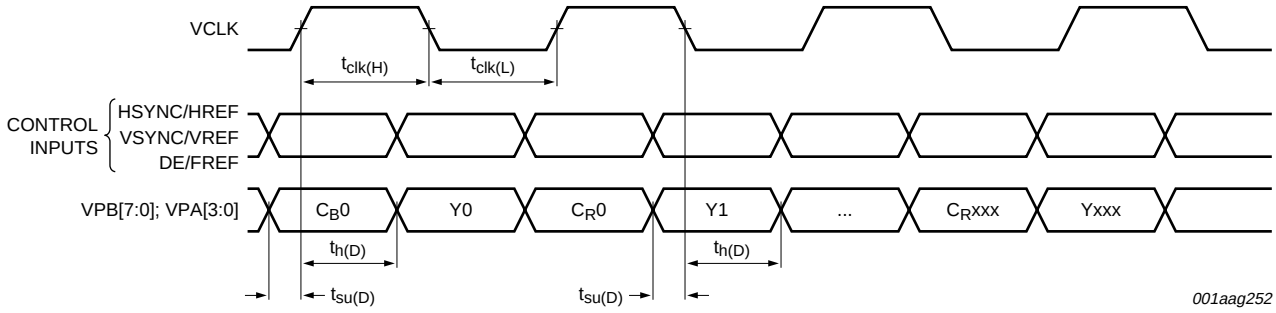


Fig 17. Timing YC_BC_R 4 : 2 : 2 ITU656-like double edge (rising and falling) input

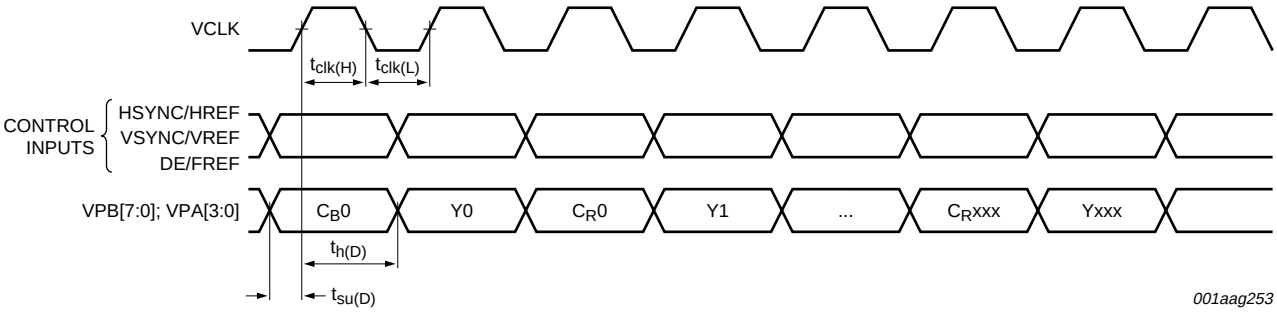


Fig 18. Timing YC_BC_R 4 : 2 : 2 ITU656-like single edge external (rising edge) input

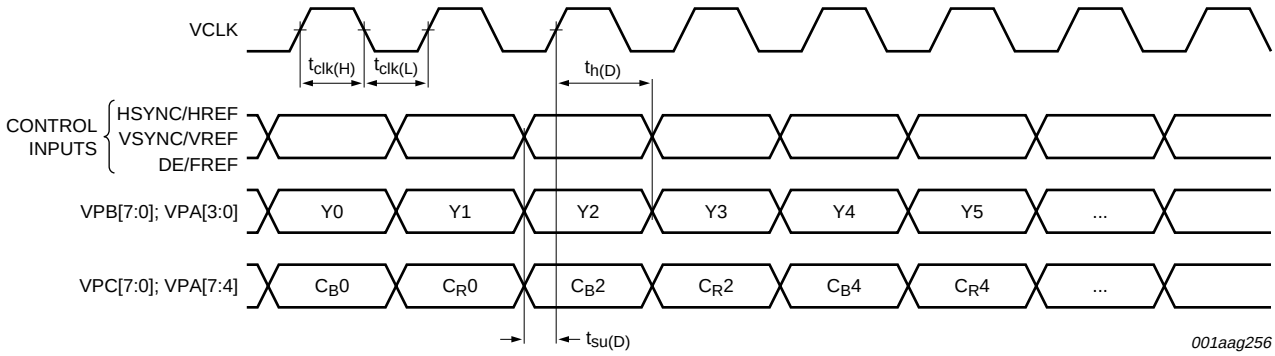


Fig 19. Timing YC_BC_R 4 : 2 : 2 semi-planar external synchronization (rising edge) input

14. Application information

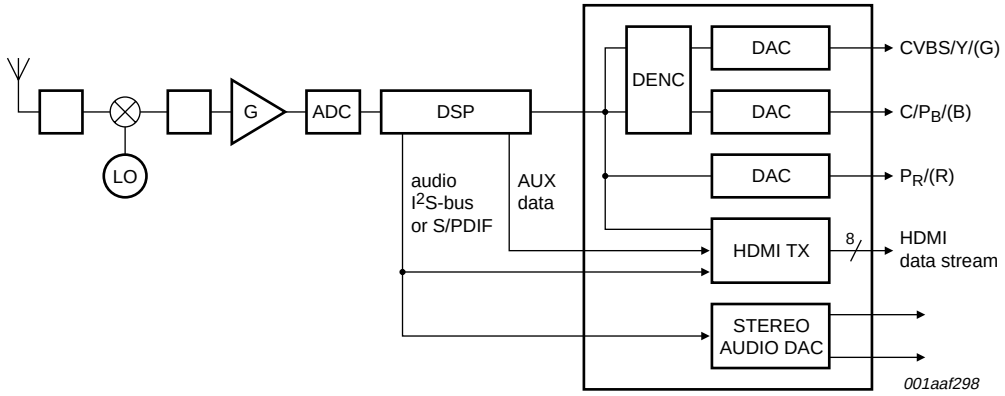


Fig 20. Application diagram for Set-Top Box

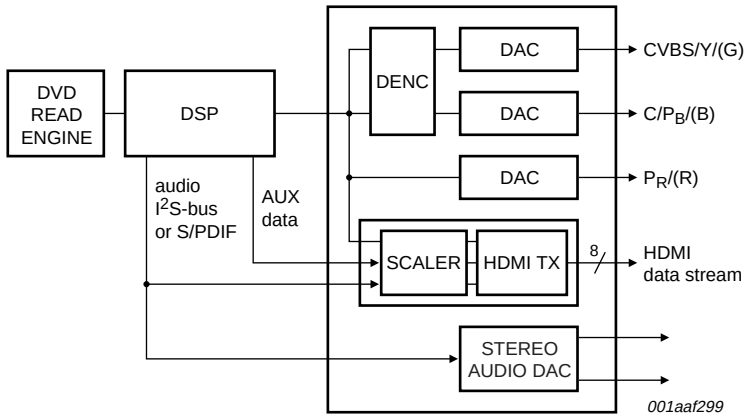


Fig 21. Application diagram for DVD player

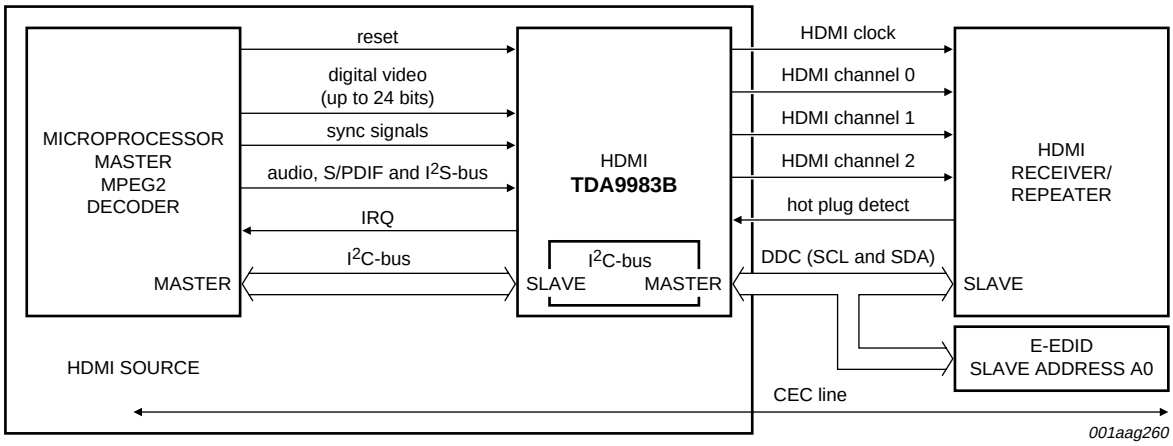
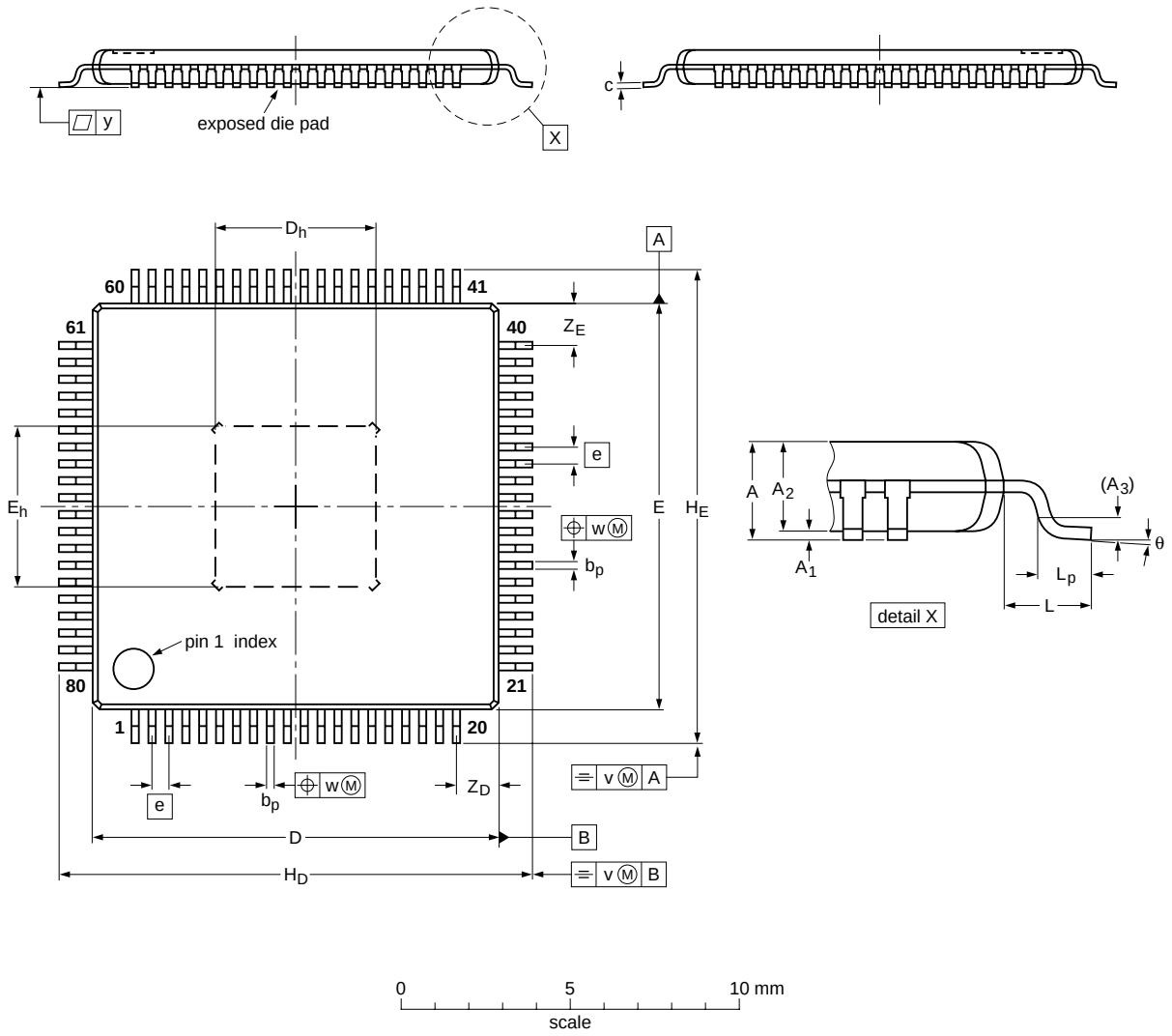


Fig 22. Transmitter connection with external world

15. Package outline

HTQFP80: plastic thermal enhanced thin quad flat package; 80 leads; body 12 x 12 x 1 mm; exposed die pad **SOT841-4**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	12.1 11.9	4.79 4.69	12.1 11.9	4.79 4.69	0.5	14.15 13.85	14.15 13.85	1	0.75 0.45	0.2	0.08	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT841-4		MS-026				~~06-04-25~~ 06-06-20

Fig 23. Package outline SOT841-4 (HTQFP80)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 119 and 120

Table 119. SnPb eutectic process (from J-STD-020C)

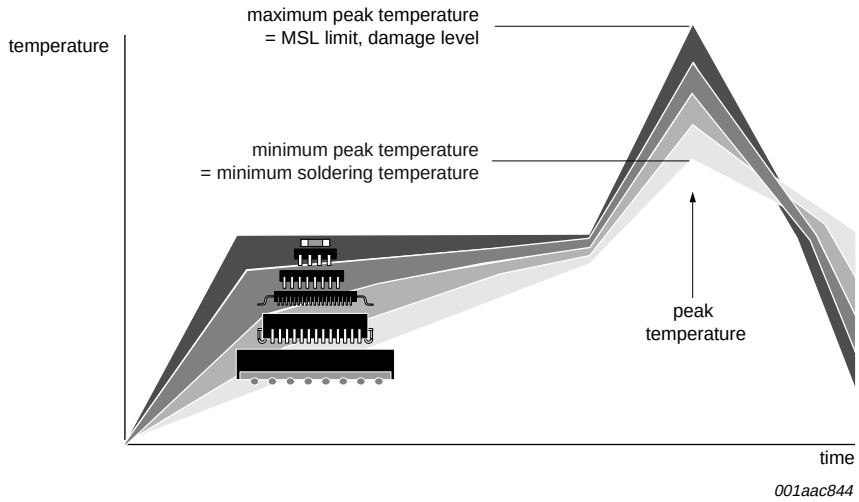
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 120. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.



MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Soldering: additional information

The package of this device supports the reflow soldering process only.

18. Abbreviations

Table 121. Abbreviations

Acronym	Description
AAC	Advanced Audio Coding
AC-3	Active Coding-3
ACP	Audio Content Protection
ADC	Analog-to-Digital Converter
AFD	Active Format Descriptor
ATRAC	Adaptive TRansform Acoustic Coding
AV	Audio Video
CEC	Consumer Electronic Control
CMOS	Complimentary Metal-Oxide Semiconductor
CTS	Cycle Time Stamp
DAC	Digital-to-Analog Converter
DDC	Display Data Channel
DENC	Digital video ENCoder
DSC	Distributed Source Code
DSP	Digital Signal Processor
DTS	Digital Transmission System

Table 121. Abbreviations *...continued*

Acronym	Description
DVB	Digital Video Broadcast
DVC	Digital Video Camera
DVD	Digital Versatile Disc
DVI	Digital Visual Interface
D-VHS	Data-VHS
EAV	End Active Video
EDID ROM	Extended Display Identification Data ROM
E-EDID	Enhanced Extended Display Identification Data
FIFO	First In First Out
HBM	Human Body Model
HDCP	High-bandwidth Digital Content Protection
HDD	Hard-Disk Drive
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition Television
HPD	Hot Plug Detect
ID	Identifier
IRQ	Interrupt ReQuest
ISRC	International Standard Recording Code
KSV	Key Selection Vector
LO	Local Oscillator
L-PCM	Linear Pulse Code Modulation
LSB	Least Significant Bit
LUT	Look-Up Table
LV-TTL	Low Voltage Transistor-Transistor Logic
MSB	Most Significant Bit
PAL	Phase Alternating Line
PCM	Pulse-Code Modulation
PLL	Phase-Locked Loop
PVR	Personal Video Recorder
RGB	Red Green Blue
Rx	Receiver
SAV	Start Active Video
STB	Set-Top Box
S/PDIF	Sony/Philips Digital Interface
TMDS	Transition Minimized Differential Signalling
Tx	Transmitter
UPC/EAN	Universal Product Code/European Assistance Network (GS1)
YUV	Y = luminance, U = normalized blue, V = normalized red
YC_BC_R	Y = luminance, C_B = chroma component blue, C_R = chroma component red

19. Revision history

Table 122. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9983B_1	20080520	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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