Generate Auxiliary Voltages at Low Cost

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When a switching regulator generates the main output voltage, additional regulated outputs may be added using various configurations of coupled inductor or charge-pump circuits.

Frequently, the *lowest possible cost* is the fundamental challenge that engineers encounter when designing power converters. When multiple output voltages are required, it is often tempting to provide one switching regulator for each output voltage. While this approach provides excellent output-voltage regulation, it certainly does nothing to help achieve the top design priority — lowest possible cost.

Fortunately, circuits such as coupled inductors and charge pumps can be easily implemented in traditional switching converters to provide additional output-voltage rails at minimal cost. Using the proper circuit configuration, it is often possible to achieve good voltage regulation along with high efficiency.

Coupled Inductors

Fig. 1 shows three different ways to generate an auxiliary output from a coupled inductor. In all three configurations, current flows in the auxiliary winding only during the on time of the synchronous FET. During this period of the switching cycle, the V_{OUT1} output voltage plus the drain-to-source voltage (V_{GS}) drop of the synchronous FET are impressed across the inductor's primary winding. The FET's voltage drop generally is quite small, usually less than 0.1 V, compared to around 0.5 V if a diode rectifier is used.

The auxiliary output voltage for an inductor with a 1:1 winding ratio is equal to the primary-winding voltage, less the forward-voltage drop of the secondary-side diode, or $V_{OUT2} = V_{OUT1} + V_{FET} - V_D$. The actual V_{OUT2} output voltage obtained is dependent on the load currents in both outputs since the voltage drops of V_{FET} and V_D are current dependent. Additionally, good coupling between the windings is necessary to reduce leakage-inductance effects at higher operating frequencies. Lower switching frequencies and light loading provide the best voltage regulation for V_{OUT2}.

As shown in **Fig. 1**, the ground reference of the auxiliary winding can be connected to any point. In circuit A, the V_{OUT2} ground can be connected to a separate, isolated ground (as shown) or to the V_{OUT1} ground if isolation is not required. In circuit B, the V_{OUT2} ground floats on top

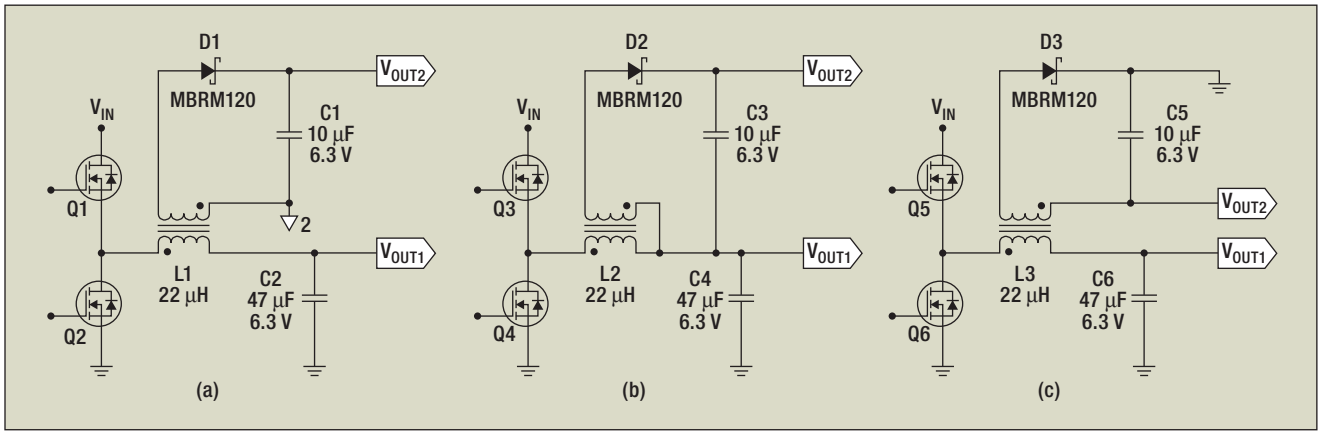

Fig. 1. *Coupled inductors create design flexibility, allowing the auxiliary voltage (V_{OUT2}) to be generated with an isolated (a) or nonisolated (b) ground, or as a negative voltage (c).*

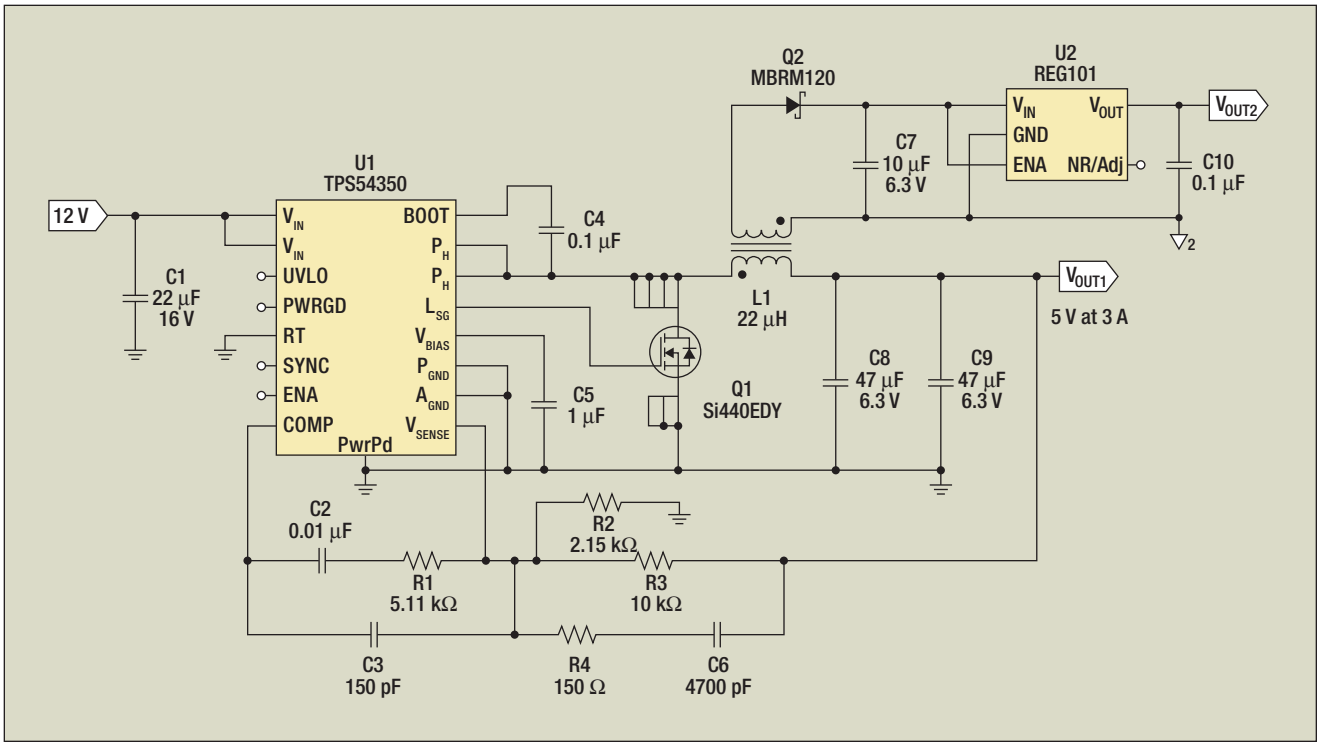

Fig. 2. *An isolated output voltage is achieved by using a coupled inductor in combination with a linear regulator.*

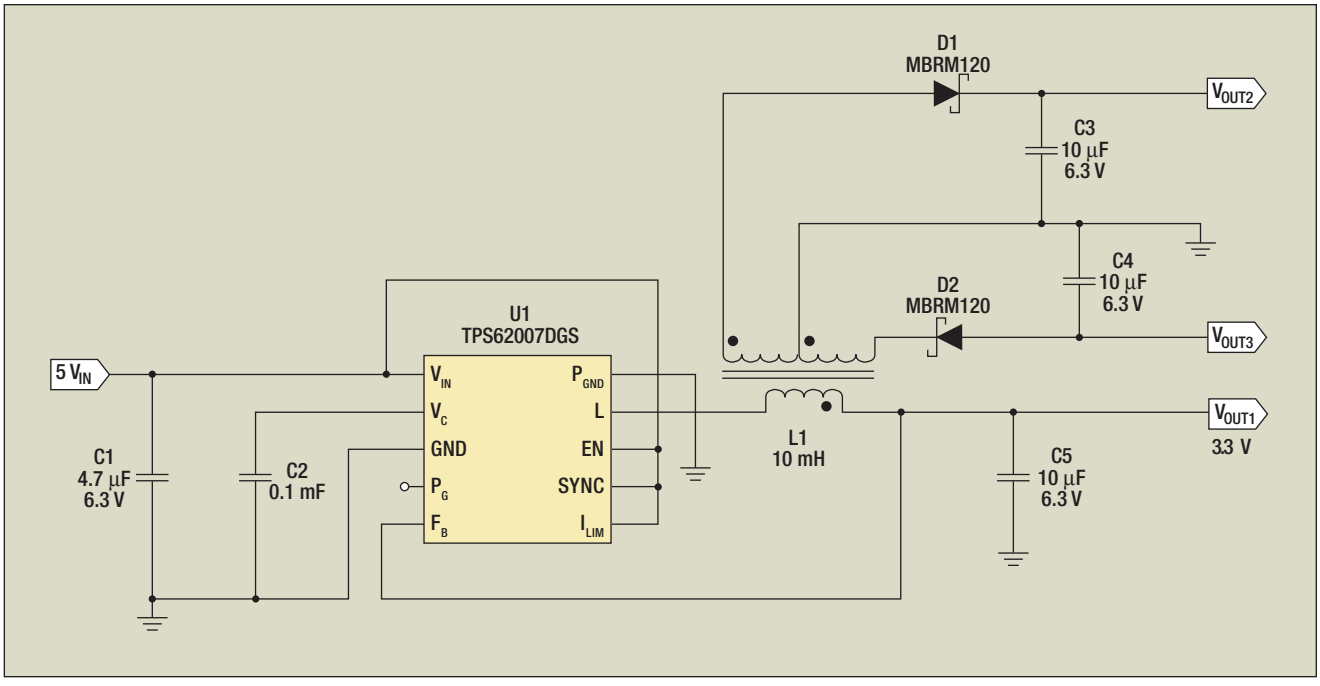

Fig. 3. *A multiwinding coupled inductor supplies positive and negative auxiliary outputs.*

of V_{OUT1}, making the output of V_{OUT2} approximately twice that of V_{OUT1}. In circuit C, the diode's cathode is grounded, making V_{OUT2} a negative output voltage.

Fig. 2 shows an example of an isolated coupled inductor design that uses a linear regulator (U2) to provide a low-current, low-noise, well-regulated output voltage. Standard off-the-shelf coupled inductors are typically bifilar wound and have 1:1 turn ratios. Low-cost custom magnetics also can be easily designed and quickly obtained, providing an avenue for generating unusual turn ratios or multiple output voltages.

Fig. 3 shows an example of a multiple-winding coupled inductor that provides matching positive and negative auxiliary output voltages (V_{OUT2} and V_{OUT3}). Various voltage configurations can be implemented by using the circuit grounding arrangements shown in **Fig. 1**.

While diode rectification on the secondary side of the coupled inductor is easy to implement, the forward-voltage

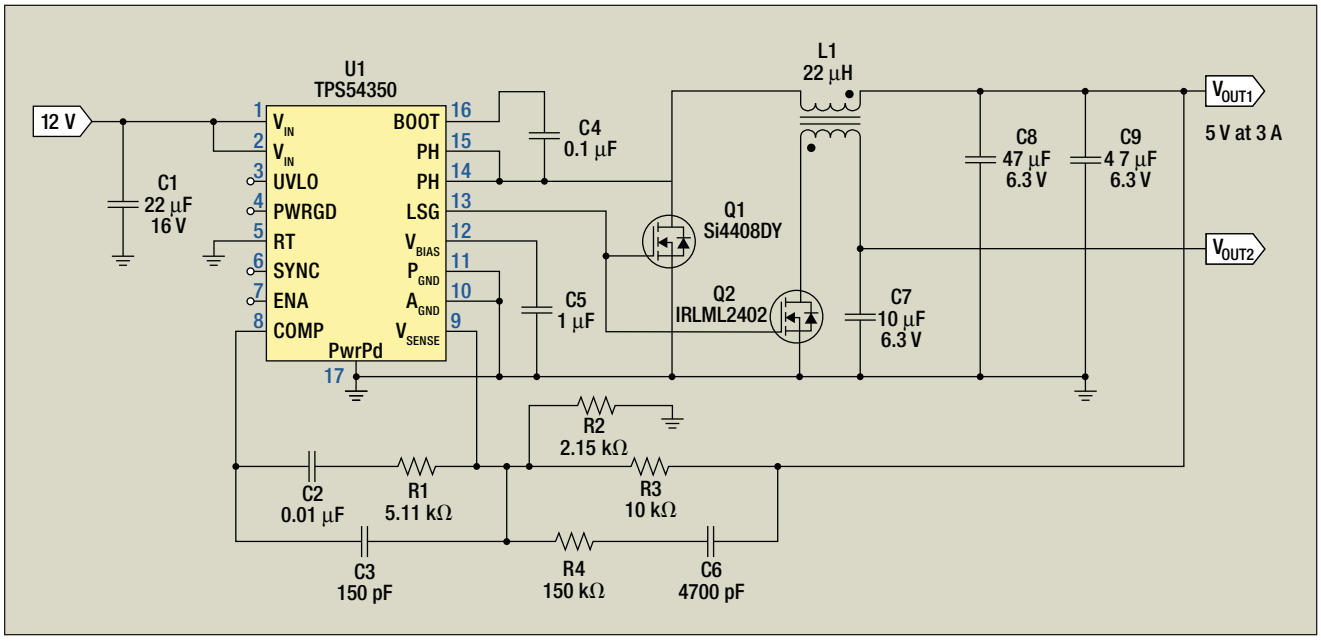

Fig. 4. *Synchronous operation using all n-channel FETs improves the efficiency of V_{OUT2}.*

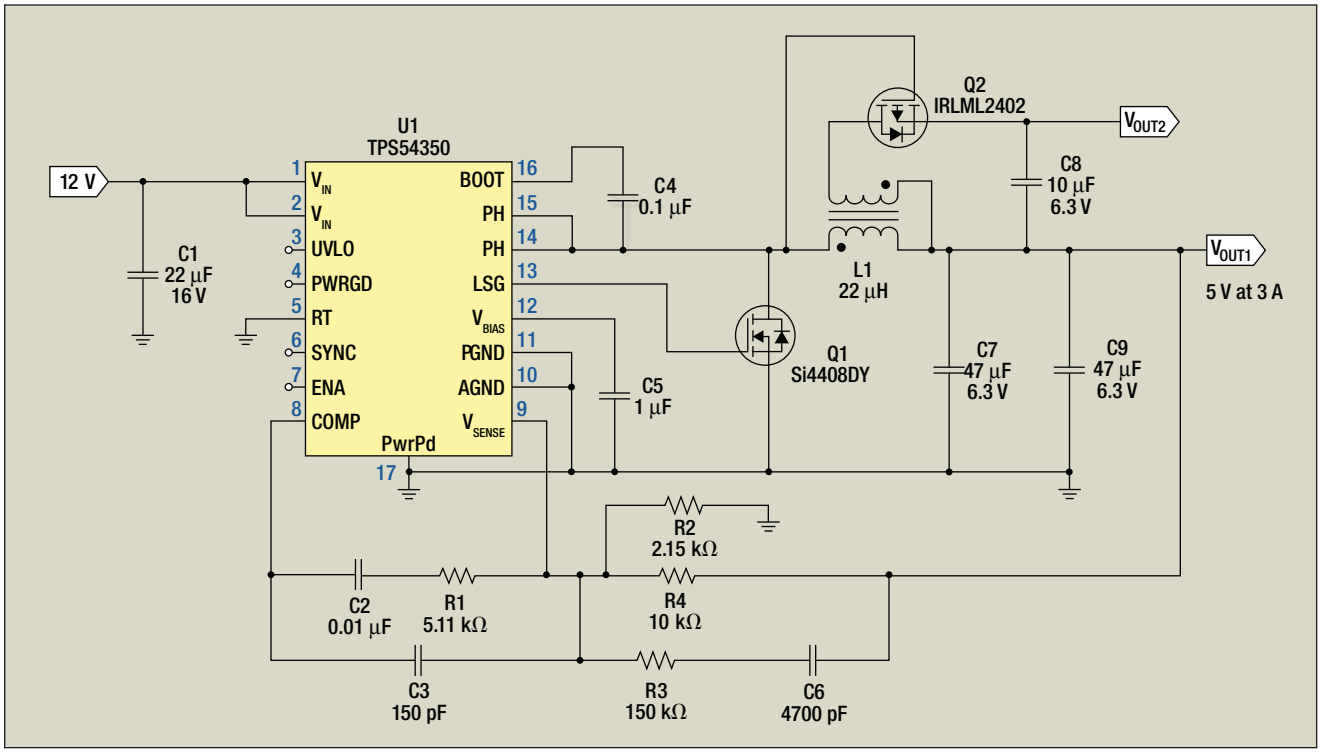

Fig. 5. *Synchronous operation of a coupled inductor using a p-channel FET eliminates the requirement for low-side gate drive for the FET associated with the auxiliary output (V_{OUT2}).*

drop of the diode can introduce a large output-voltage variation over load current and temperature. **Fig. 4** shows a circuit that uses secondary-side synchronous rectification to reduce the voltage variation and FET losses.

When low-resistance FETs are used, FET voltage drops are minimal and the output-voltage regulation for V_{OUT2} improves. Under certain loading conditions, the voltage drops of FETs Q1 and Q2 will perfectly cancel each other, resulting in an output voltage for V_{OUT2} that is equal to V_{OUT1} times the turns ratio of the coupled inductor.

Excellent cross regulation and high efficiency can be achieved with this technique. The drawback is that access to the low-side FET gate-drive signal is required to drive the synchronous coupled-inductor FET. This eliminates the use of synchronous buck controllers that have integrated top *and* bottom FETs. The circuit in **Fig. 5** bypasses this

limitation by using a p-channel FET.

The **Fig. 5** circuit operates identically to that of **Fig. 4**, except the gate drive to the p-channel FET is driven out-of-phase by the switch node, rather than the bottom FET gate drive. Care must be taken when a p-channel FET is used in this configuration that the gate-source voltage available is adequate to ensure full enhancement in steady-state operation.

The maximum turn-on V_{GS} in **Fig. 5** is equal to V_{OUT2}, since the FET switches on when the switch node pulls to ground. This places a limit on the maximum output voltage that V_{OUT2} can be, as many p-channel FETs have maximum V_{GS} ratings of only 8 V or 12 V. A maximum reverse V_{GS} equal to the input voltage (V_{IN}) is applied when the switch node pulls to the input voltage and the output voltage is zero, which occurs at startup.

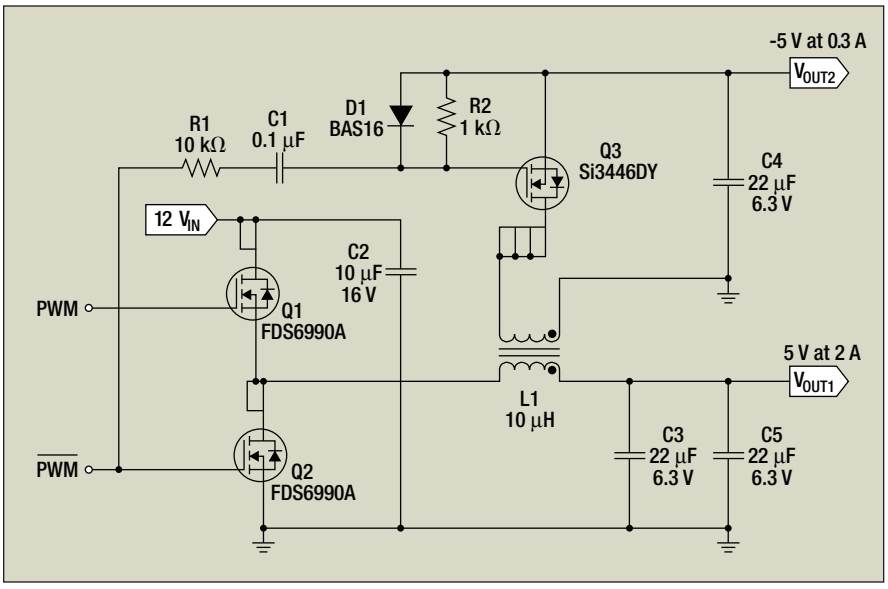

Fig. 6. *A coupled inductor can produce a negative output voltage using a synchronous n-channel FET for rectification.*

Fig. 6 shows a synchronous version of the circuit shown in **Fig. 1c**, using an n-channel FET for the auxiliary output. The gate-drive voltage for Q3 is derived from the gate-drive voltage of bottom FET Q2, allowing both FETs to switch in phase with each other. Capacitor C1 ac-couples this switching signal, but blocks its dc average level. Diode D1 conducts only during the negative swing of the Q2 drive voltage, clamping Q3's gate voltage to 0.7 V below the source and turning it off.

During the positive swing of the Q2 drive voltage, V_{GS} for Q3 is equal to the Q2 gate-drive voltage, less a diode drop, turning it on. The use of 2.5-V_{GS} threshold parts may be necessary if the gate-drive voltage is 4.5 V to 5 V. Without D1, the positive V_{GS} would vary with duty cycle, creating a situation where FET Q3 may not have enough drive voltage to turn on properly.

Charge Pumps

The circuit in **Fig. 7** is a boost converter with a charge pump that generates a negative auxiliary output voltage. The charge-pump circuit is composed of C2, C4, D3 and D4. When the FET turns off in a boost converter, the stored energy in the inductor is transferred to the output capacitor and load through diodes D1 and D2. At the same time, D4 conducts and C2 is charged to the output voltage plus a diode drop.

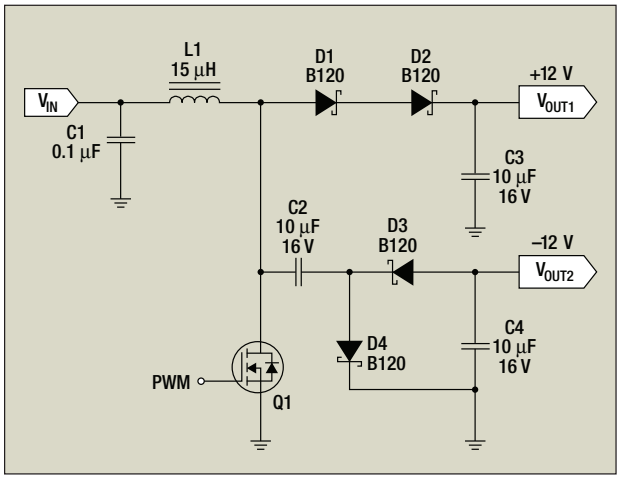

Fig. 7. *When a boost converter is used to generate the main output (V_{OUT1}), a charge pump can be added to generate a complementary, negative output voltage (V_{OUT2}).*

When the FET turns on again, the voltage on C2 pulls the charge-pump output negative through D3. The two diodes in the boost converter (D1 and D2) are necessary to cancel the forward-voltage drops of the two diodes in the charge pump (D3 and D4). Excellent voltage regulation is achieved for light loads on the (negative) charge-pump output.

The circuit in **Fig. 8** is a charge pump that boosts the V_{OUT2} output voltage to the input voltage plus the V_{OUT1} output voltage. When the internal synchronous FET of the TPS62007 controller switches to ground, it charges C3 to the V_{OUT1} output voltage, less one diode drop. Then the internal control FET turns on, pulling U1 pin 9 to V_{IN}. This action forces the charge stored in C3 into output-capacitor C5.

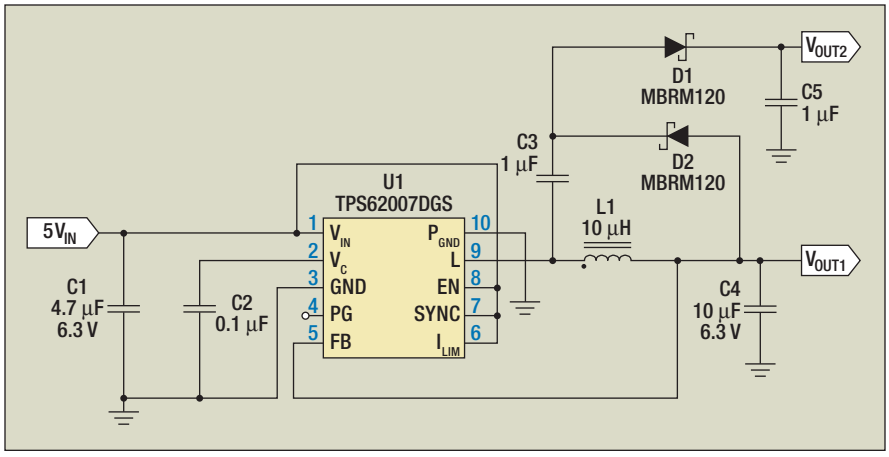

Fig. 8. *A charge-pump circuit can produce an auxiliary output voltage (V_{OUT2}) equal to the main output voltage (V_{OUT1}), plus the input voltage minus two diode drops.*

As with most charge pumps, there are two diode drop reductions in the output voltage in **Fig . 8**. This circuit is useful in applications where the input voltage is well regulated or where the auxiliary output can feed the input to a linear regulator for a lower output voltage.

Fig. 9 is a variation of **Fig. 8**, but provides a negative output voltage at V_{OUT2}. The output voltage of the charge pump is equal to the inverted input voltage, less two diode drops.

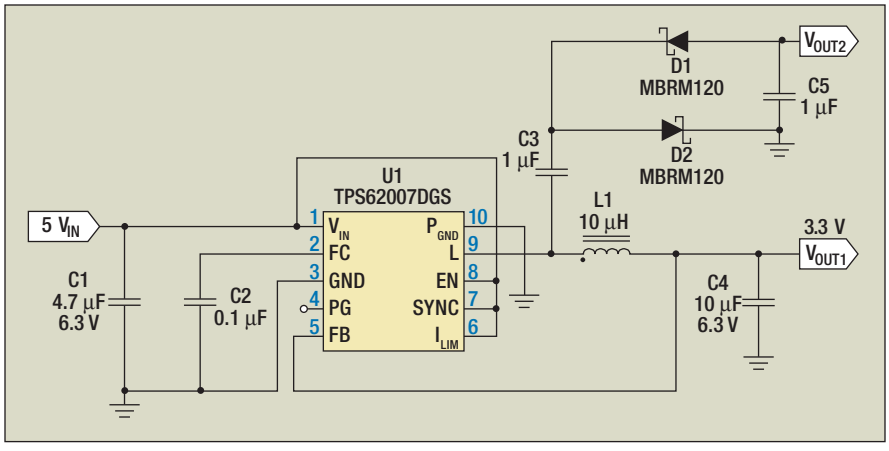

Fig. 9. *An inverting charge pump provides a negative output voltage nearly equal to the positive input voltage. (The absolute values of V_{IN} and V_{OUT2} differ by two diode drops.)*

The circuit in **Fig. 10** is a multiple-output flyback using a stacked-winding transformer. Regulation is achieved by feedback from output V_{OUT2}. The addition of diode D1 and C9 creates a negative-output V_{OUT4} that is equal in magnitude to V_{OUT2}.

Energy is transferred to all outputs only during the off time of FET Q1. During this interval, a negative voltage

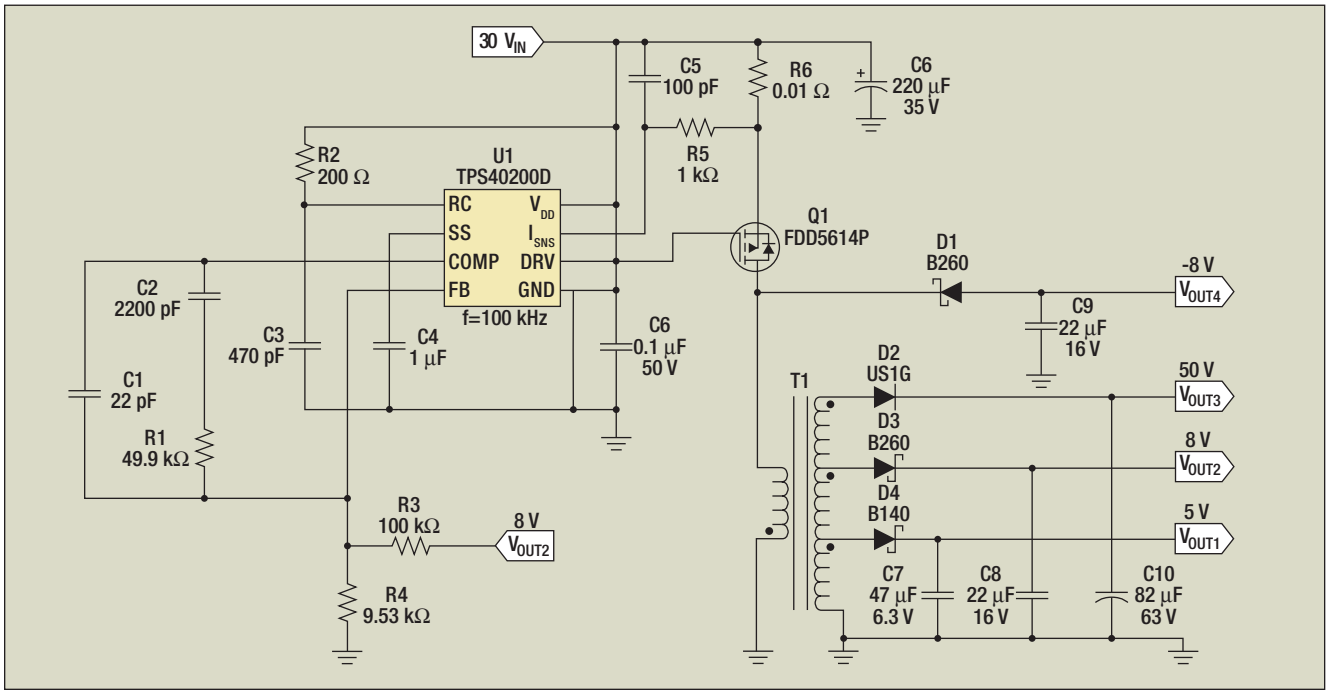

Fig. 10. *A buck-boost converter joined with a flyback generates a series of auxiliary voltages (V_{OUT2}, V_{OUT3} and V_{OUT4}).*

equal to V_{OUT2} is imposed across the primary winding, due to a 1:1 turns ratio between the primary winding and the V_{OUT2} stacked winding. With a negative V_{OUT2} clamped across the primary winding, diode D1 charges capacitor C9, resulting in a voltage on output V_{OUT4} that is closely matched to V_{OUT2}. **PETech**