A 90–240 MHz Hysteretic Controlled DC-DC Buck Converter With Digital Phase Locked Loop Synchronization

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***Abstract*—This paper reports a digital phase locked loop (D-PLL) based frequency locking technique for high frequency hysteretic controlled dc-dc buck converters. The proposed converter achieves constant operating frequency over a wide output voltage range, eliminating the dependence of switching frequency on duty cycle or voltage conversion range. The D-PLL is programmable over a wide range of parameters and can be synchronized to a clock reference to ensure proper frequency lock and switching operation outside undesirable power supply resonance bands. The stability and loop dynamics of the proposed converter is analyzed using an analog equivalent PLL behavioral model which describes the dc-dc converter as a voltage-controlled oscillator (VCO). We demonstrate a 90–240 MHz single phase converter with fast hysteretic control and output conversion range of 33%–80%. The converter achieves an efficiency of 80% at 180 MHz, a load response of 40 ns for a 120 mA current step and a peak-to-peak ripple less than 25 mV. The circuit was implemented in 130 nm digital CMOS process.**

***Index Terms*—DC-DC converter, hysteretic, buck, constant frequency, digital PLL, CMOS.**

I. Introduction

POWER delivery systems for high performance microprocessors must cope with high peak current demands, fast current transients, and stringent supply voltage tolerances [1]. In order to meet these requirements, near-load power delivery solutions based on localized step-down switch-mode voltage regulator modules over (3D-stacked), next to or within the processor die have been proposed [2], [3]. While a variety of converter topologies are suitable, highly integrated buck converter embodiments of the hysteretic pulse-width modulation (PWM) controller have been shown to achieve peak efficiencies greater than 80% at switching frequencies above 100 MHz, enabling 2–3 orders of magnitude reduction in capacitor (and inductor) size and extremely fast load response times of 1–5 ns [4]. The hysteretic controller shown in Fig. 1(a) is based on a simple feedback loop that achieves fast load response without stability issues. The hysteretic controller consists of a comparator with hysteresis $\mathrm{V_H}$ and a simple RC network connected to the inductor windings to sense the inductor current via the feedback voltage $\mathrm{V_{FB}}$. Changes in output voltage are coupled to the comparator via the feedback network (R_F, C_F), creating a near immediate response via the negative feedback action of the comparator. The simplicity of the design stems from the fact that neither error amplifier nor a clock generator is required as in the case of the widely used PWM controller. Moreover, the hysteretic controller does not require phase compensation to improve the converter's dynamic response. The switching frequency of the hysteretic controlled buck converter can be derived from the slope of V_{FB} and the hysteretic window V_H, which can be approximated as [5]

$$f_S = \frac{D \cdot (1 - D)}{\tau_{\mathrm{RC}}(V_H/V_{\mathrm{IN}}) + \tau_D} \tag{1}$$

where V_{IN} is the input voltage to the converter, D is the PWM signal duty cycle set by the desired output voltage V_O, τ_{RC} equals $R_F C_F$ of the feedback network, and τ_D corresponds to the finite controller propagation delay due to the controller itself and the drivers and output bridge. From (1), the maximum switching frequency occurs when $D = 0.5$, or $f_{\mathrm{MAX}} = 0.25/(\tau_{\mathrm{RC}}(V_H/V_{\mathrm{IN}}) + \tau_D)$. Since D sets the output conversion ratio V_O/V_{IN}, the switching frequency exhibits a strong dependence on the output voltage. For instance, for a conversion range of $D = 0.2$ to $D = 0.8$, the switching frequency varies from 0.64 f_{MAX} to f_{MAX}. This dependence of switching frequency on output voltage can cause switching noise generated by the converter to fall in power supply resonance bands (due to parasitic package inductance interconnects and on-die decoupling capacitances), thereby inducing voltage excursions in the power supply network that are compromising to the overall reliability and operation of the devices [6].

Thus, it is highly desirable to synchronize the dc-dc converter to an external clock reference or one that is supplied from within the chip by the processor. A variety of hysteretic PWM controlled synchronization methods have been proposed. Synchronization signals can be injected directly into the reference voltage of the hysteretic comparator [4], but this requires careful control of the injected signal amplitude, shape and frequency to achieve proper frequency lock. The multiphase voltage-mode hysteretic controller reported in [7] utilizes a synchronization scheme that limits the output conversion range to 1/N of the input voltage, where N is the number of converter phases, and therefore requires larger input voltage when the number of phases increases. The DLL based hysteretic controller design proposed in [8] shows a flexible multiphase

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synchronization scheme with a large output voltage range, but similar to approaches presented in [4] and [7], it does not maintain a constant switching frequency when the conversion ratio changes. To solve this problem, some frequency compensation techniques have been published recently for voltage mode (V-mode) hysteretic controllers [9], [10] and quasi-V^2 hysteretic controllers [11]. In [9], an adaptive-on-time circuit adjusts the converter on-time according to the input voltage, achieving a nearly constant frequency operation. However, this approach does not compensate for frequency changes caused by the output voltage and furthermore does not allow for external synchronization. In contrast, the adaptive delay compensation techniques proposed in [10] and [11] provide frequency lock by comparing the dc-dc converter switching frequency to a constant reference. In [10], the reference is supplied by a constant analog voltage, with bias accuracy and noise performance being major design issues. A more robust digital approach presented in [11] requires sampling the converter switching frequency (i.e., 3 MHz) using a high frequency clock (i.e., 150 MHz), and is therefore not suitable for ultra-high frequency dc-dc converters (>100 MHz).

Closed loop frequency stabilization methods of hysteretic PWM converters using a phased-lock loop (PLL) have been proposed by these and other authors [12]–[14]. The basic idea is to adjust one or more internal parameters of the converter itself to lock the converter's switching frequency to an external clock reference using the negative feedback action of the PLL. To stabilize the frequency, one can adjust the peak, average [13] or slope [14] of the sensed inductor current ripple used for hysteresis control, or alternatively the controller delay can be used as the control mechanism [12]. The latter provides an additional degree of freedom to set the switching frequency since the noise sensitive ripple current signal is not directly adjusted. In this work, a digital PLL (D-PLL) synchronization scheme is used to achieve wide and accurate frequency control at very high operating frequencies unlike previously reported methods [10], [11], [13], [14]. The proposed D-PLL based hysteretic converter operates similar to a PWM converter within the loop bandwidth of the PLL, and maintains a simple feedback network that allows for a fast load response. Moreover, the use of a digital PLL shows superior noise immunity and scalability compared to analog counterparts such as analog PLLs or analog frequency control loops. Owing to the digital nature of the PLL, all parameters, including the frequency, divide ratios and filter coefficients are digitally programmable, allowing for detailed system-level programmability and control. To validate the proposed technique, a single phase current-mode hysteretic PWM buck converter was implemented in 1.2 V 130 nm digital CMOS process to achieve 90–240 MHz frequency lock operation [12]. This work presents additional circuit details and measurements and formalizes the stability analysis for this type of converter. In Section II, we present an overview of the proposed synchronization scheme and a detailed stability analysis of the PLL controlled hysteretic converter. Circuit implementation details and mixed signal simulations are discussed in Section III. Measurement results and concluding remarks are presented in Section IV and V, respectively.

II. Analysis of a Phased Lock Loop (PLL) Synchronized and Hysteretic Controlled DC-DC PWM Converter

Fig. 1(b) shows a simplified schematic of the proposed PLL synchronized hysteretic controlled dc-dc buck converter. The standalone hysteretic controlled dc-dc converter is modeled as a free-running oscillator with frequency f_s defined by (1) that nominally depends on the duty cycle (D), the time constant $(\tau_{\rm RC})$ and the overall controller delay (τ_D). Since D sets the conversion range, and $\tau_{\rm RC}$ affects both the load response via the high-pass feedback network $R_F C_F$ and the ripple voltage via the hysteretic window V_H, a voltage controlled delay line is inserted in the controller's feedback path to adjust the oscillating frequency. The converter switching frequency can be re-written as

$$f_S = \frac{D \cdot (1-D)}{\tau_{\rm RC}(V_H/V_{\rm IN}) + \tau_D + \Delta\tau} \tag{2}$$

where $\Delta\tau$ is the delay due to the delay line. In order to frequency lock the converter to an external reference, the output of the hysteretic comparator $({\rm CK_{HYS}})$ is divided down and compared against a low frequency clock reference $({\rm CK_{REF}})$ using a phase/frequency detector. The outputs of the detector are fed to a charge-pump (CP) and loop filter (LF) to produce a control variable $({\rm V_{CTRL}})$ that sets the delay line delay and the dc-dc switching frequency. Thus the dc-dc converter with delay line control can be viewed as a voltage controlled oscillator (VCO) and the overall loop as a PLL.

The closed-loop response of the PLL synchronized dc-dc converter can be approximated in the s-domain by a second-order analog charge-pump PLL (CP-PLL) with the VCO representing the hysteretic dc-dc converter itself. Unlike [13], the analysis presented here uses delay as the controlled parameter to set the frequency. The block diagram for the model is shown in Fig. 2. The analysis assumes a continuous time approximation which is valid for PLL bandwidths about one decade or more below the operating frequency. In order to derive representative VCO parameters for PLL stability analysis, the voltage-to-frequency characteristic of the dc-dc converter is linearized about its operating point. It follows that for a fixed output voltage under steady state dc-dc converter operation, the duty cycle D remains approximately constant and so do the filter and fixed loop delay values $\tau_{\rm RC}$ and τ_D, respectively. Defining $\tau_F = \tau_{\rm RC}(V_H/V_{\rm IN}) + \tau_D$ as the fixed time constant term in (2), and assuming the amount of delay $\Delta\tau$ that is added by the delay line is small compared to τ_F (i.e., $\Delta\tau/\tau_F < 1$), (2) can be approximated using a Taylor series expansion as

$$\begin{aligned} \omega_S &= \frac{2\pi D \cdot (1-D)}{\tau_F}\left[1 + \frac{\Delta\tau}{\tau_F}\right]^{-1} \\ &\approx \frac{2\pi D \cdot (1-D)}{\tau_F}\left[1 - \frac{\Delta\tau}{\tau_F}\right] \end{aligned} \tag{3}$$

where $\omega_S = 2\pi f_S$ (rad/s) and f_s is the converter switching frequency. Letting $\omega_{\rm FR} = 2\pi {\rm D}(1-{\rm D})/\tau_F$ (the nominal oscillation frequency) and $\Delta\tau = K_{\rm DL} V_{\rm CTRL}$, where $K_{\rm DL}$ is the gain of the delay line and $V_{\rm CTRL}$ is the control voltage, (3) can be written as

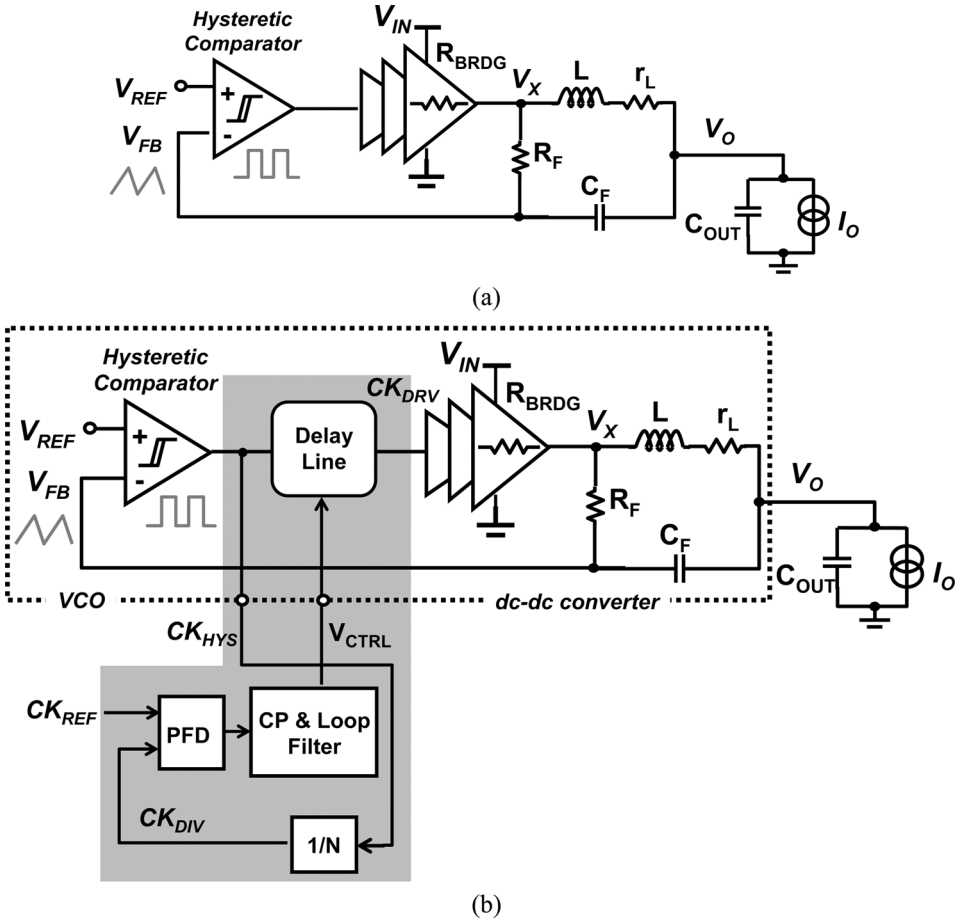


Fig. 1. Hysteretic controlled dc-dc converter (a) conventional single phase topology and (b) proposed PLL synchronized hysteretic controlled buck converter.

$$\omega_s = \omega_{\mathrm{FR}} - \left[\frac{2\pi D\cdot(1-D)\cdot K_{\mathrm{DL}}}{\tau_F^2}\right]\cdot V_{\mathrm{CTRL}} \tag{4}$$

Since the frequency is proportional to the applied control voltage V_{CTRL}, integrating (4) with respect to time yields the excess phase (φ_{out}) at the output of the VCO representing the hysteretic converter. As the VCO integrates the output frequency to form the output phase, the VCO transfer function can be expressed in s-domain as $\varphi_{\mathrm{out}}(s)/V_{\mathrm{CTRL}}(s) = K_{\mathrm{VCO}}/s$, where K_{VCO} is the VCO gain given by

$$K_{\mathrm{VCO}} = \frac{2\pi D\cdot(1-D)\cdot K_{\mathrm{DL}}}{\tau_F^2} \tag{5}$$

The closed loop response relating the output phase $\varphi_{\mathrm{out}}(s)$ to the input phase $\varphi_{\mathrm{in}}(s)$ of the charge-pump PLL model [15] in Fig. 2 is given by

$$\begin{aligned} H(s) &= \frac{\varphi_{\mathrm{out}}(s)}{\varphi_{\mathrm{in}}(s)} \\ &= \frac{K_{\mathrm{loop}}(RCs+1)}{s^2 + K_{\mathrm{loop}}RCs + K_{\mathrm{loop}}} \\ &= \frac{2\varsigma\omega_n s + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \end{aligned} \tag{6}$$

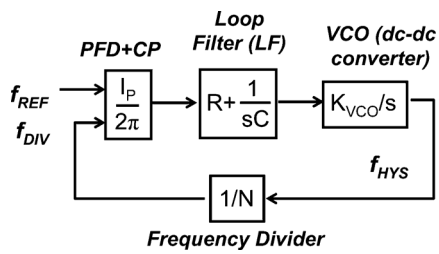


Fig. 2. Equivalent s-domain model of proposed PLL synchronized hysteretic controlled dc-dc buck converter. The hysteretic dc-dc converter is modeled as a VCO in the charge-pump PLL.

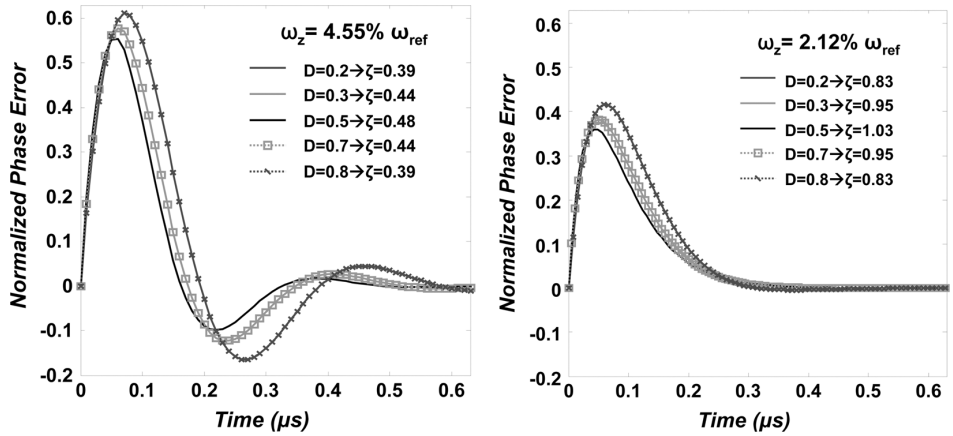
where $\mathrm{K_{loop}} = \mathrm{I_{CP}K_{VCO}}/(2\pi\cdot \mathrm{C}\cdot N)$ is the open loop gain, $\mathrm{I_{CP}}$ is the charge pump current, R and C are the loop filter resistance and capacitance, respectively, N is the divide ratio, ζ is the damping factor and ω_{n} is the loop bandwidth.

Substituting (5) into $\mathrm{K_{loop}}$, the damping factor (ζ) and loop bandwidth (ω_{n}) in (6) can be expressed as

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{\mathrm{CP}}C}{N}}\cdot\frac{\sqrt{D\cdot(1-D)\cdot K_{\mathrm{DL}}}}{\tau_F} \tag{7a}$$

$$\omega_n = \frac{2\cdot\zeta}{R\cdot C} \tag{7b}$$

As seen from (7), D and τ_{F} affect both the damping factor and bandwidth of the PLL synchronized dc-dc converter. Increasing τ_{RC} (or $\mathrm{R_F C_F}$) in the high-pass filter feedback network



(a) (b)

Fig. 3. Phase error response to a frequency step versus converter duty cycle for two loop filter settings (a) of $\omega_z = 4.55\% \cdot \omega_{\rm ref}$ and (b) $\omega_z = 2.12\% \cdot \omega_{\rm ref}$, where ω_z and $\omega_{\rm ref}$ are the zero and reference frequencies, respectively.

reduces ζ since $\tau_{\rm F}$ equals $\tau_{\rm RC}(V_{\rm H}/V_{\rm IN})+\tau_D$, but also provides a faster load response as the output voltage droop coupling to $\rm V_{FB}$ of the hysteretic comparator is increased (see Fig. 1(b)) [8]. Similarly, ζ decreases for high or low conversion ratios corresponding to large or small values of D, respectively, or for large $\rm V_H/V_{IN}$. Fig. 3 shows the phase error response to a frequency step at various duty cycles (or conversion ratios) for two different loop filter settings. Assuming a duty cycle range of 0.2 to 0.8, the maximum decrease in damping factor is only $1-2\sqrt{D\cdot(1-D)}$ or 20%. Similar changes in $\tau_{\rm RC}$ or $(V_H/V_{\rm IN})$ can be accounted for by proper setting of the loop filter parameters [16]. Therefore, the stability of the PLL synchronized dc-dc converter can be ensured by the charge-pump and loop filter settings to accommodate a wide range of dc-dc converter design parameters.

III. Circuit Implementation of D-PLL Synchronized Hysteretic DC-DC Converter

A block diagram schematic of the proposed D-PLL synchronized hysteretic dc-dc converter is shown in Fig. 4. The hysteretic comparator consists of comparator A1 with resistive feedback network $\rm R_{H1}$-$\rm R_{H2}$ to set the hysteretic window $\rm V_H = V_{IN}R_{H1}/(R_{H1}+R_{H2})$. A resistor $\rm R_D$ is added in the control loop to adjust the output impedance for improved load response [17]. The output clock $(\rm CK_{HYS})$ generated by the hysteretic comparator is divided down N × M times, where N and M are the corresponding division ratios of the dividers. The resulting divided down clock $(\rm CK_{DIV})$ is compared against an external reference clock $(\rm CK_{REF})$ using a bang-bang type phase frequency detector (PFD). A digital proportional-integral (PI) loop filter acts on the early/late information from the PFD to generate a control word that is fed to a sigma delta modulator and decoder to adjust the DCDL delay. The first order sigma-delta is clocked at 1/M of the $\rm CK_{HYS}$ frequency and used to enhance the delay resolution of the DCDL. To ensure stable operation, the bandwidth of the DPLL is set much smaller than the hysteretic converter loop by proper choice of digital loop filter settings. The DCDL output feeds to a non-overlapping clock generator circuit to drive the high-side and low-side integrated output bridge. A serial interface programs the proportional and integral gains in the loop filter, the divide ratios, the hysteretic comparator window height $\rm V_H$, and an on-chip load circuit. Owing to its digital implementation, the proposed D-PLL synchronization controller is inherently more immune to noise and easily scalable compared to its analog counterparts [10], [14], [18]; in fact, many of the components can be digitally synthesized. Moreover, the D-PLL controller does not require high frequency sampling clocks as in ADC based approaches [11], and is thus suitable for ultra-high frequency (>100 MHz) converter designs.

A. Digital Phased Locked Loop (D-PLL) Design

Fig. 5 shows the block diagram of the D-PLL. A bang-bang PFD compares the rising edges of the $\rm CK_{REF}$ and $\rm CK_{DIV}$ and generates a 1-bit early/late signal for the digital proportional-integral (PI) loop filter. The loop filter consists of a 19-bit accumulator with 2-bit integral gain (K_I) and a 3-bit proportional gain (K_P) control. The KP/KI ratio in the PI filter is used to adjust the stability of the loop by setting the position of the zero introduced by the proportional path [19]. A bit selector (SEL) selects 11 out of 19 bits from the output of the PI filter (i.e., $[10:0], [11:1], \ldots$) to control the DCDL. Out of the 11-bit digital filter's output, 3 bits are used by the sigma-delta to generate a bit-stream which controls one of the fine delay cells in the DCDL. The 8 remaining bits at the output of the selector along with the sigma-delta output form a 9-bit control word (A[0:8]), where A[0] represents the bit-stream of the first order sigma-delta. In the DCDL, two 3-to-8 decoders control a coarse delay line and the three LSB's of the control word directly control the fine delay cells. The sigma-delta is a 3-bit accumulator with the carry out of the final adder producing the bit-stream. Programmable dividers generate the necessary clocks for the PFD, sigma-delta and digital loop filter. The sigma delta is clocked at a programmable divide-by-M ratio, whereas the loop filter and PFD operate at a divide-by-NxM ratio locked to the reference clock frequency. The sigma delta can be operated at 1/4, 1/8, 1/16 or 1/32 of the output frequency depending upon the 2-bit control signal (DIV_SEL). With the exception of the PFD and

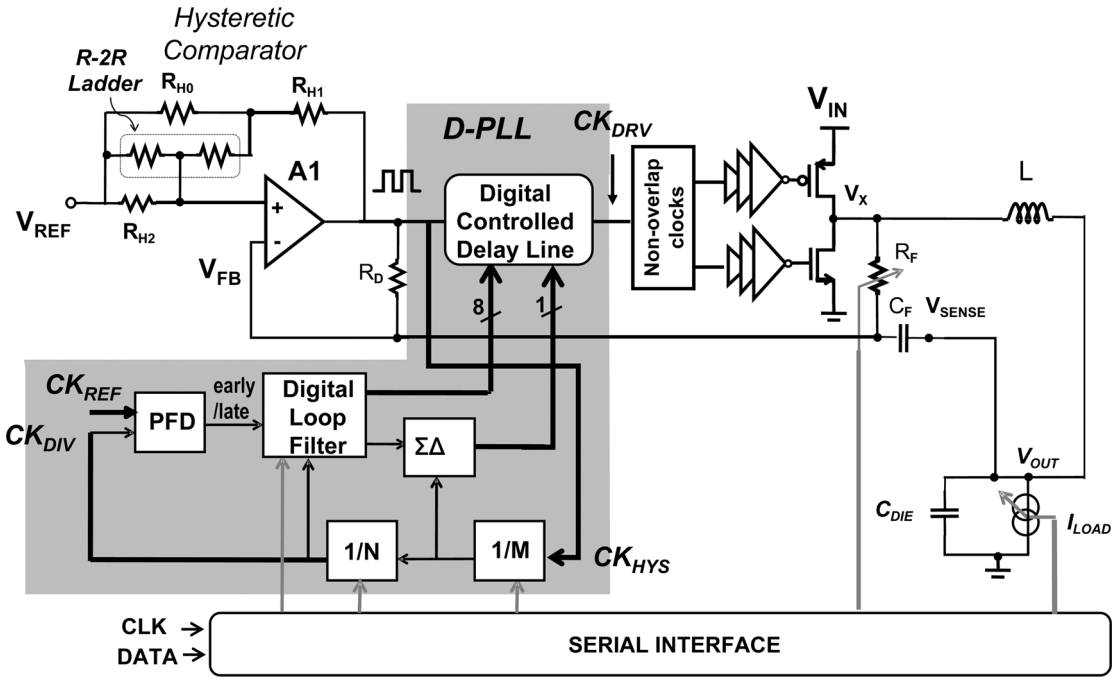


Fig. 4. Block-diagram of D-PLL synchronized hysteretic controlled buck converter.

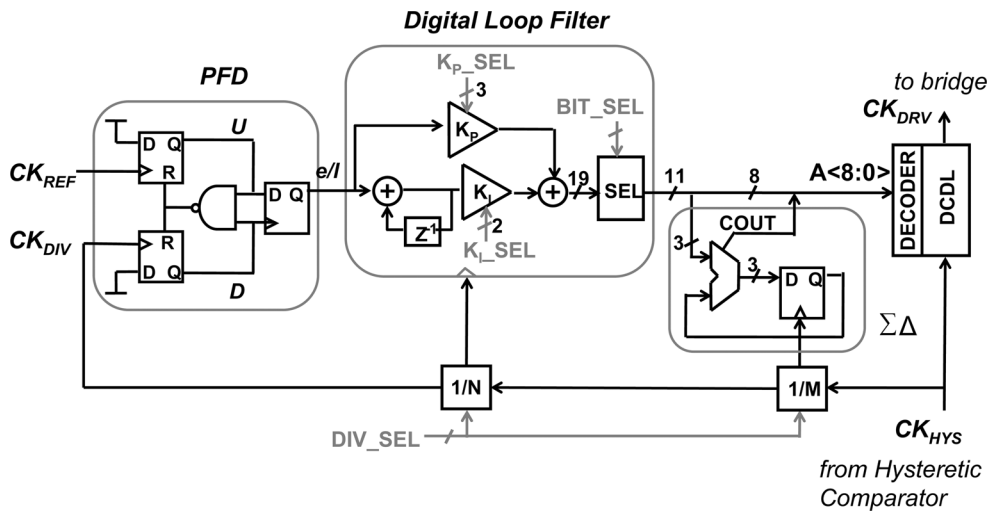


Fig. 5. Simplified block diagram of D-PLL.

DCDL, automatic synthesis and place and route tools were employed to implement the DPLL.

The DCDL as shown in Fig. 6 consists of two tuning stages: a coarse tuning stage and a fine tuning stage. The coarse tuning delay chain is made up of 63 delay buffers plus one additional dummy buffer at the end that is not used. Each delay buffer in the coarse stage consists of two tri-state inverters with a fixed delay of about 40 ps to produce a coarse delay range of approximately 0–2.52 ns. The 64 delay buffers are divided into 8 delay groups (D_0-D_7). Two 3-to-8 decoders act together to generate the coarse delay using the 6 MSBs (A[8:3]) of the control word. Three bits A[8:6] select an output from the delay groups (D_0-D_7) and two bits A[5:3] select the corresponding output from within each delay group. The fine tuning stage is implemented using an inverter with 3 tri-states (1X, 1X, 2X) in parallel, adding a 0–40 ps tunable delay to the DCDL. The bit-stream from the sigma-delta (A[0]) and 2 LSB's (A [1], A [2]) control the three tri-state gates.

B. Hysteretic Comparator

A standard comparator A1 composed of three differential stages with pMOS loads followed by a differential to single-ended output stage and rail-to-rail buffer is used to implement the hysteretic comparator, as shown in Fig. 7. A common mode feedback (CMFB) circuit sets the output level equal to about half of the supply voltage by adjusting the tail current of the input stage using transistors M_{0F}-M_{1F} [18]. The comparator provides a simulated gain of $\sim$45 dB, 3 dB bandwidth of $\sim$1.2 GHz and propagation delay of less than 300 ps when the input

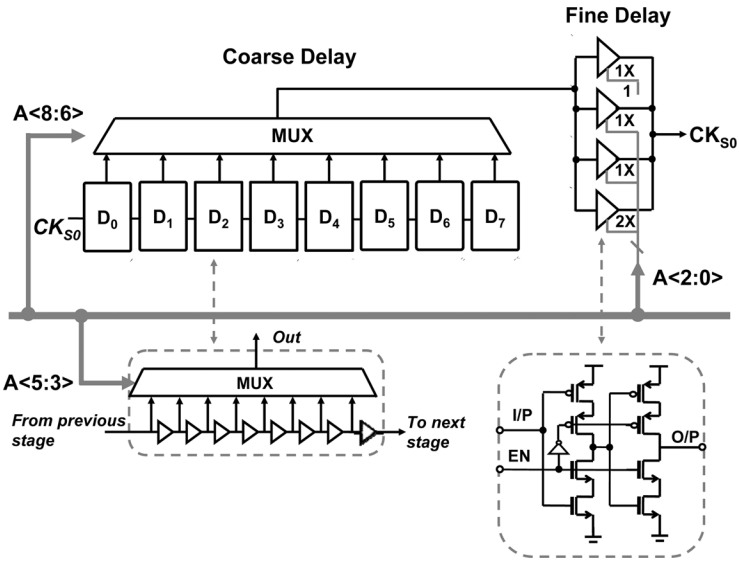


Fig. 6. Block level schematic of digital-controlled delay line (DCDL).

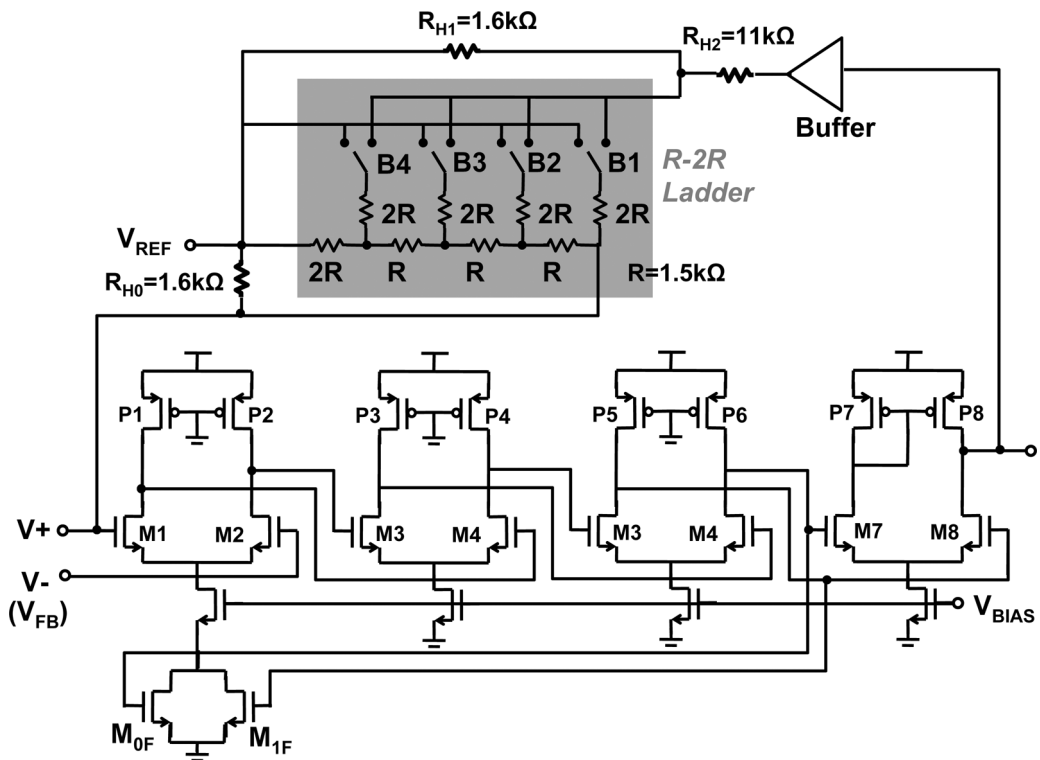


Fig. 7. Schematic of hysteretic comparator.

is 10 mV. Resistors RH0–RH2 along with the R–2R ladder implements a digitally controlled resistive network to set the hysteretic window [4]. Digital control bits B[1:4] from a serial interface are used to set the R–2R ladder resistance to vary the hysteretic window from 1/80 to 1/10 of V_{IN}.

C. Output Bridge

The output bridge was sized to achieve high efficiency at load currents of $\sim$0.2 A and switching frequency of $\sim$100 MHz. As shown in Fig. 8(a), the output stage and associated drivers are each divided into 17 cells that snap together to form the composite output bridge structure. Each cell measures 20 μm in width and contains distributed power grids for V_{IN} and GND, input decoupling capacitance, low-side nMOS and high-side pMOS drivers and output switches that connect to the output node V_X. Input decoupling cells are placed between the drivers and the output switches to widen power traces and decrease current density. The output bridge, including drivers, decoupling capacitance and power switches, measures 350 μm by 270 μm.

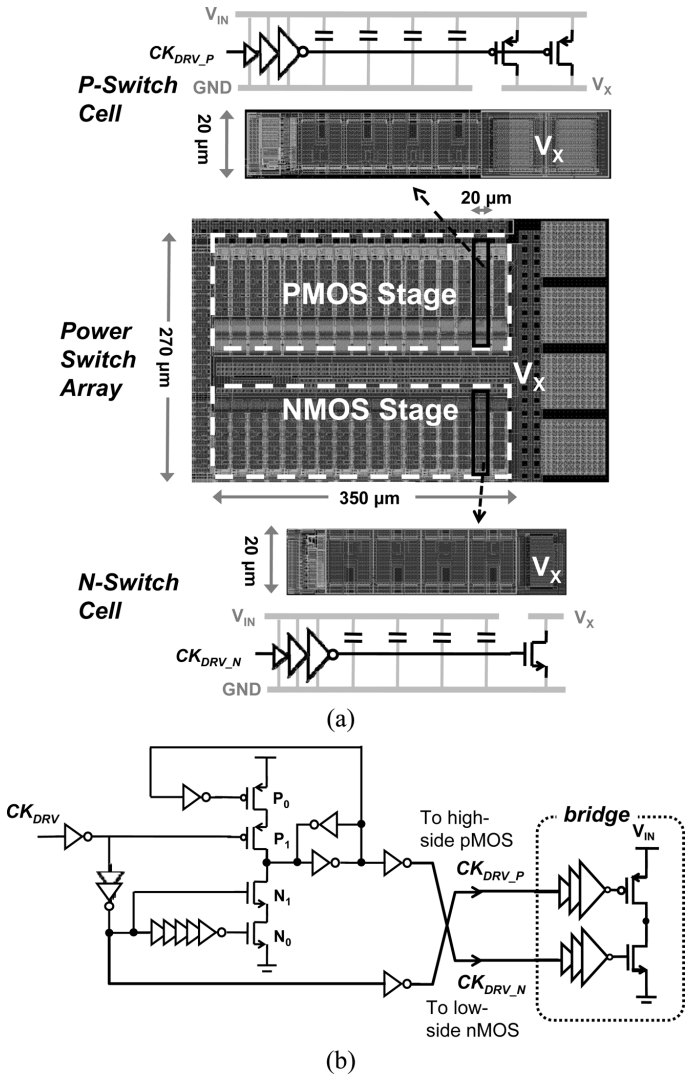


Fig. 8. DC-DC converter output stage: (a) layout of power switches and drivers and (b) schematic of pre-driver with non-overlapping low and high side clocks.

The power switches alone occupies 0.021 mm^2, or approximately 22% of the total area. The peak bridge current density is $\sim$11.4 A/mm^2 for a maximum output current of $\sim$240 mA.

As shown in Fig. 8(b), a pre-driver is used to generate non-overlapping drive signals for a fixed dead-time between low and high side output switches, and thereby minimize short circuit current losses in the output bridge. A negative (hi-to-lo) transition of $\mathrm{CK_{DRV}}$ (from the DCDL output) generates a corresponding lo-to-hi transition in both $\mathrm{CK_{DRV-P}}$ and $\mathrm{CK_{DRV-N}}$, wherein $\mathrm{CK_{DRV-N}}$ is slightly delayed for a high-side pMOS dead-time of $\sim$60 ps. Similarly, a positive (lo-to-hi) edge in $\mathrm{CK_{DRV}}$ causes $\mathrm{CK_{DRV-P}}$ to lag $\mathrm{CK_{DRV-N}}$ for a low-side nMOS switch dead-time of $\sim$40 ps.

D. On-Chip Load

The load response of the high-frequency dc-dc converter is validated using an integrated on-chip load capable of generating load transients with programmable ramp time and current steps, as shown in Fig. 9. The on-chip current step generator consists of eight programmable current sources, each with 3-bit control,

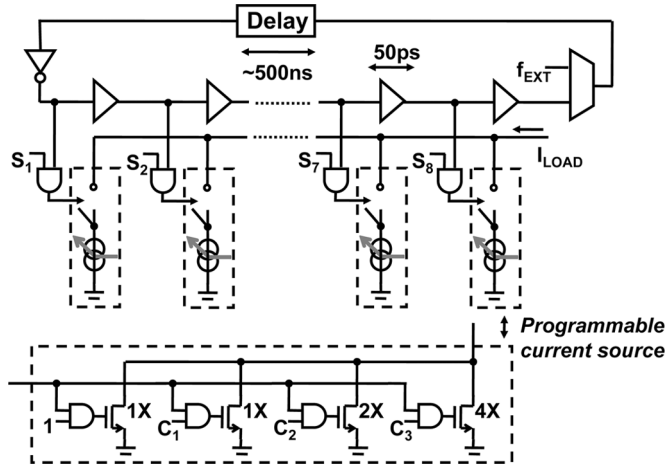


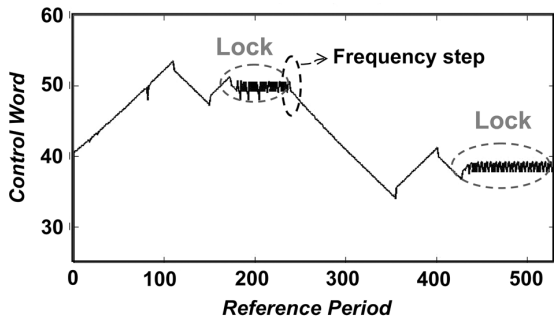
Fig. 9. On-chip load with programmable rise time and current steps.

triggered either by an internal ring oscillator or by an external clock $(\mathrm{f_{EXT}})$. Fast rising and falling edges are generated by sequentially enabling or disabling the current sources staggered by a delay of $\sim$50 ps. The resulting load step has a programmable ramp time of 50 ps to 400 ps and maximum step current of 120 mA (or one half the peak load current of the dc-dc converter). The maximum current transient that can be generated is $\sim$0.3 A/ns.

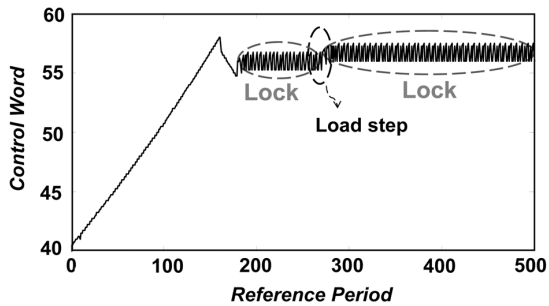
E. Mixed Signal Simulations

Since the linearized CP-PLL model introduced in Section II is not strictly applicable to bang-bang PLLs due to the hard nonlinearity introduced by the early/late phase information from the binary PFD, one has to resort to time stepped simulations to precisely validate the loop dynamics. However, simple closed-form expressions can be applied to determine design parameters such as the loop filter proportional (KP) and integral (KI) gains from their analog counterparts (R and C) that simplify the design and analysis of digital bang-bang PLLs. The interested reader can refer to [20], [21] for further information on this subject. In order to validate the stability of the proposed system, detailed simulations of the D-PLL synchronized hysteretic buck converter were carried out using a SpectreVerilog mixed-signal simulation environment. All components of the D-PLL, except the delay line, were replaced by Verilog code. Transistor level schematics were employed for the delay line and all analog blocks in the dc-dc converter.

Fig. 10(a) shows the digital loop filter control word response versus reference clock cycles for an example simulation setup where an input frequency step is applied after the D-PLL attains lock at start-up. The simulation consisted of an initial reference clock frequency of 40 MHz, division factor N of 4, integral path gain of 0.5 and proportional path gain of 3. After the D-PLL attains initial lock, the input reference clock frequency is changed from 40 MHz to 33.33 MHz, causing the D-PLL to loose lock momentarily, and then to regain lock after approximately 200 reference clock cycles. Fig. 10(b) shows the response to a load step of 80 mA when the reference clock frequency is fixed at 45 MHz, $\mathrm{N} = 4$ and $\mathrm{KP/KI} = 5/0.3$. Since the average voltage at the output of the dc-dc converter is reduced by the voltage drop



(a)



(b)

Fig. 10. Mixed-signal simulations depicting transient response of the D-PLL synchronized dc-dc converter at start-up and after (a) a frequency step is applied to the input of the PFD and (b) a current step is applied to the output of the dc-dc converter.

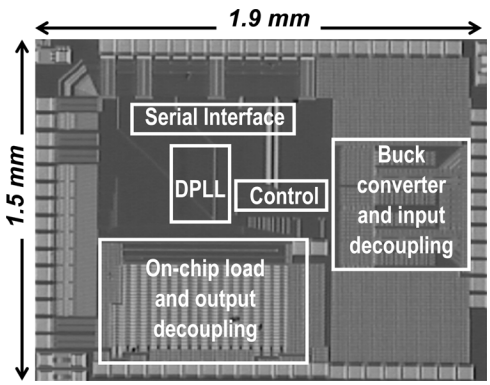


Fig. 11. Die photograph.

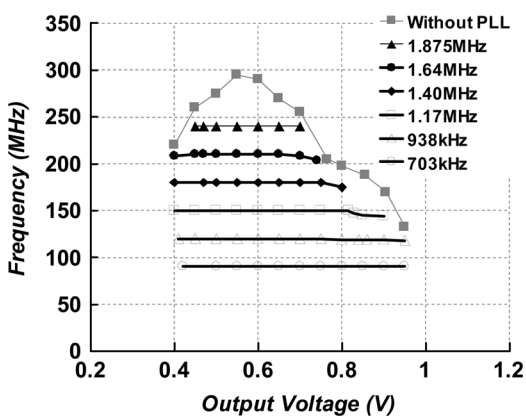


Fig. 12. Measured dc-dc converter switching frequency versus output voltage before and after enabling the D-PLL.

across the bridge resistance and inductor resistance, loading the converter with current causes a droop that is compensated by a change in duty cycle D. In turn, since D affects the switching frequency of the hysteretic controller as presented in (1), a current step appears as a frequency step to the D-PLL (i.e., this frequency step can be referred to the input of the PFD). The D-PLL adjusts the control word to compensate for the change in frequency (in this case an increase in frequency) and remains stable despite changes in output loading. Thus, the effect of large signal transients in the dc-dc converter can be captured by corresponding changes in frequency and/or phase at the input of the PLL, and the resulting PLL dynamics are determined by the tracking and acquisition characteristics set by the loop filter parameters [15], [16].

IV. Measurement Results

An integrated dc-dc buck converter with hysteretic control loop and D-PLL based synchronization was fabricated in standard 130 nm digital CMOS process. Fig. 11 shows the die photo. The buck converter is operational from 90 MHz to 240 MHz and occupies approximately 0.34 mm^2, which includes the DCDL, controller and a 0.7 nF on-chip input decoupling capacitor. The D-PLL without the DCDL measures 320 μm by 200 μm. The converter was evaluated at different frequencies using various external SMT size-0805 air core inductors ranging from 8.2 nH to 24 nH and output decoupling chip capacitors ranging from 25 nF to 220 nF. The external inductors, although small in value, were not integrated on-die or embedded as part of a 3D-stack as post-CMOS metallization and TSV processing was not available for fabricating high quality inductors.

A. Frequency Locking Performance

In order to evaluate the frequency locking performance of the D-PLL synchronization scheme, the converter's switching frequency was measured at various output voltages for a fixed input voltage $V_{\rm IN}$ of 1.2 V, and external LC filter of 8.2 nH ($Q \sim 25$) and 20 nF. As shown in Fig. 12, when the DPLL is disabled and the DCDL is set for the minimum delay, the converter's switching frequency exhibits a characteristic dependence on output voltage (or duty cycle) as approximated by (1). To test the DPLL, we set the divide ratio to 128 and varied the reference frequency from approximately 703 kHz to 1.875 MHz in 30 MHz/128 increments. The corresponding measurements show that the output switching frequency is locked to the input reference over a wide range of 90 MHz to 240 MHz. The output voltage range over which the DPLL locks is bounded by the maximum free-running switching frequency set by the hysteretic converter. Thus the output voltage range decreases as the frequency is increased. The jitter histogram of the divided down clock ($CK_{\rm DIV}$) and the multiplied clock or bridge output signal (V_X) are shown in Fig. 13. $CK_{\rm DIV}$ shows an RMS and peak-to-peak jitter of 10.4 ps and 83 ps, respectively. The switching node V_X at the bridge output includes the delay of noisy power train stages (see Fig. 4), thus resulting in higher RMS and peak-to-peak jitter of 42.5 ps and 244 ps, respectively.

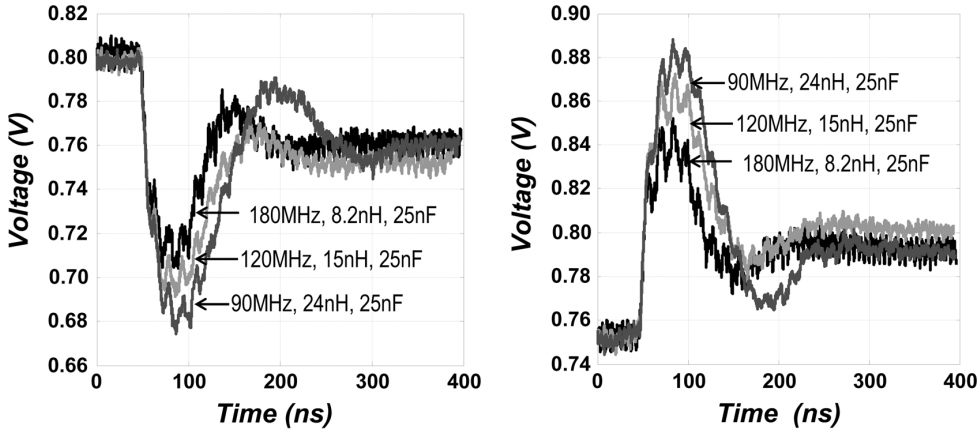


Fig. 15. Measured load response to a 0.12 A (a) low-to-high and (b) high-to-low current step for 1.2 V/0.8 V conversion ratio and output capacitance of 25 nF.

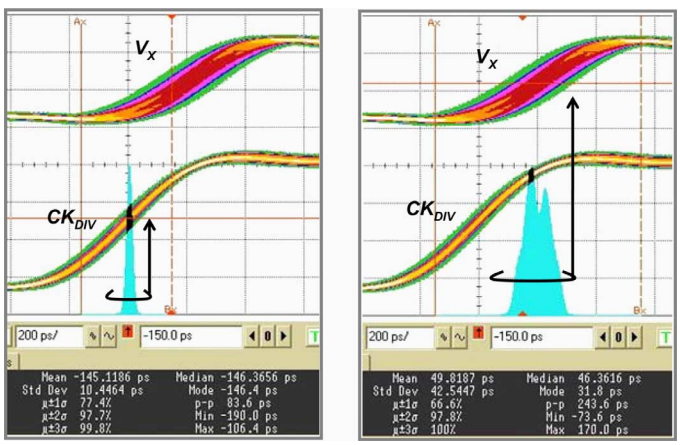


Fig. 13. Jitter histogram of (a) D-PLL divided clock ($\mathrm{CK_{DIV}}$) and (b) the switching node ($\mathrm{V_X}$) at the output of the bridge.

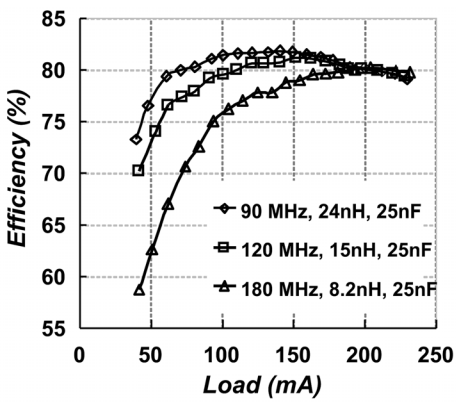


Fig. 14. Measured dc-dc converter efficiency at 90 MHz, 120 MHz and 180 MHz.

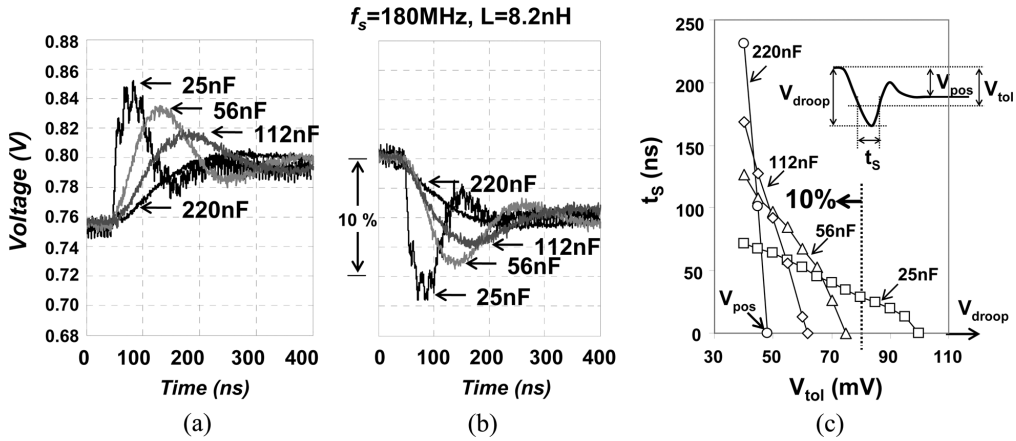
B. Efficiency

The converter's power efficiency versus load current was measured at switching frequencies of 90 MHz, 120 MHz and 180 MHz and conversion ratio of 1.2 V/0.8 V, as shown in Fig. 14. The peak efficiency at 90 MHz and 120 MHz was ∼81% for a load current of ∼150 mA. At 180 MHz and external filter of 8.2 nH and 25 nF the peak efficiency was ∼80% for a load current of 200 mA. Increasing the load current decreases the efficiency due to higher resistive losses associated with the ripple current in the inductor, whereas at lighter loads the switching frequency losses associated with the bridge dominate. Because larger inductors exhibit higher series resistance and hence higher conduction losses, as the output current loading is increased the efficiency of a converter with larger inductor and lower switching frequency drops off faster than that of a converter with a smaller inductor and higher switching frequency.

C. Load Transient Response

Fig. 15 shows the converter transient response to a 120 mA load step measured at 90 MHz, 120 MHz and 180 MHz with corresponding inductor values of 24 nH, 15 nH and 8.2 nH, respectively. The output capacitor was set to 25 nF for all cases. The current step was generated using a programmable on-chip load with a ramp time of 100 ps. The resulting output voltage is about 0.8 V when the converter is loaded with 80 mA and approximately 0.75 V when loaded with 200 mA. The voltage droop for both low-to-high and high-to-low current steps was ∼100 mV at 180 MHz and ∼130 mV at 90 MHz. The resulting undershoot/overshoot exhibits a similar response initially due to the slew rate of current in the effective series inductance (ESL) of the output capacitor. The output shows a steady-state voltage error of about 50 mV due to the resistive response introduced by voltage positioning [17]. The measured ripple voltage is less than ∼25 mV and the load response is ∼40 ns.

Fig. 16 illustrates the effect of output decoupling on transient response for a 180 MHz converter with 8.2 nH filter inductor. As shown in Fig. 16(a) and (b), decreasing the L/C ratio reduces the voltage droop and increases the load response time. The voltage droop is less than 10% for output decoupling of 56 nF or higher. Fig. 16(c) shows the time $\mathrm{t_S}$ the converter remains outside a specified voltage tolerance window $\mathrm{V_{tol}}$ for different output decoupling. The maximum voltage droop for each case occurs at $\mathrm{t_S} = 0$ corresponding to the x-axis intercept in Fig. 16(c). For a specified voltage tolerance, there is a tradeoff between the time the output is outside the desired voltage tolerance window and



(a) (b) (c)

Fig. 16. Effect of output decoupling on load response for 180 MHz converter with $L = 8.2$ nH (a) low-to-high and (b) high-to-low current step for 1.2 V/0.8 V conversion ratio and (c) time t_s output remains outside voltage tolerance window V_{tol}.

TABLE I
PERFORMANCE SUMMARY

Technology	130nm CMOS
DC-DC converter area	0.42mm^2
Bridge area, A_{BRDG}	0.03mm^2
Decoupling Capacitance	20nF
Inductance, L	8.2nH
Input voltage, V_{IN}	1.2V
Output voltage, V_{OUT}	0.4V~0.96V
Switching frequency, f	90M~240M
Maximum current, I_{MAX}	240mA
Current density, I_{MAX}/ A_{BRDG}	8 A/mm^2
V_{IN}=1.2V, V_{OUT}=0.8V, f=180MHz	
Voltage Droop @ 0.12A step	100mV
Efficiency (peak)	80%
Efficiency @ I_{MAX}	77.5%

the size of the output decoupling. For instance, a voltage tolerance of about 60 mV is met with 112 nF output decoupling. However, if the output decoupling is decreased to 25 nF, the output remains outside the 60 mV window for about 50 ns. At 220 nF, the converter achieves a maximum tolerance of about 50 mV, which is limited by the steady-state error voltage introduced by voltage positioning (V_{pos}). In the present design, the voltage positioning resistor is fixed and cannot be adjusted to lower the steady-state voltage error.

D. Performance Summary

Table I summarizes the measured performance of the hysteretic buck converter with D-PLL synchronization. At 180 MHz, 1.2 V/0.8 V input/output conversion, 200 mA load current and external filter of 8.2 nH and 25 nF, the converter achieves a peak efficiency of 80%. Table II shows a comparison with previously reported integrated buck converters with different types of hysteretic control loops. Among the reported converters, [4], [8] and this work employ current-mode (C-mode) hysteretic control while operating in the 10–100 MHz frequency range. Compared to [4] and [8], this work compensates for the frequency change by updating the delay line in the hysteretic control loop. In this case, the hysteretic converter, inherently a variable frequency converter, operates similar to a fixed frequency PWM converter within the loop bandwidth of D-PLL. Other frequency compensation techniques for voltage mode (V-mode) hysteretic controllers [9], [10] and quasi-V^2 hysteretic controllers [11] have been recently reported. However, [9] lacks frequency synchronization and does not compensate for changes in frequency due to changes in output voltage or conversion ratio. Both [10] and [11] provide closed loop frequency control by comparing to a reference voltage or digital control word. In this work, the D-PLL based controller provides accurate frequency synchronization and achieves high operating frequencies for reduction in LC passive components size and fast transient response [4], [8], [22]–[25].

V. CONCLUSION

We demonstrate a bang-bang D-PLL frequency locking technique for ultra-high frequency hysteretic controlled dc-dc buck converters. The D-PLL locks the converter operating frequency to a clock reference to eliminate the dependence of switching frequency on output conversion voltage. A voltage or digitally controlled delay element inserted within the hysteretic control loop is used to control the converter's switching frequency. An equivalent linear system representation is employed to model the hysteretic loop as a voltage controlled or digitally controlled oscillator. Linear system analysis shows that when the oscillator (i.e., hysteretic buck converter) is placed inside a PLL, the stability of the system is primarily determined by the PLL parameters (i.e., loop filter, division ratio, etc), and weakly dependent on the dc-dc converter parameters (i.e., duty cycle, current loading, etc). Thus the stability of the PLL is ensured for wide frequency locking of the hysteretic dc-dc buck converter. Both analog and digital PLL designs, as well as linear and binary bang-bang loops, are feasible. Moreover, the proposed synchronization scheme can implement the hysteretic control loop as a fixed frequency PWM controller or an auto-selectable-frequency PFM controller [26]. By adjusting the D-PLL division ratio N, the converter switching frequency can be scaled by binary weighted multiples of the fundamental to reduce switching

TABLE II
PERFORMANCE COMPARISON

	[9]	[10]	[11]	[8]	[4]	This Work
Year	2007	2007	2009	2007	2005	2008
Control Loop	V-mode hysteretic	V-mode hysteretic	Quasi-V^2 hysteretic	C-mode hysteretic	C-mode hysteretic	C-mode hysteretic
Fixed Freq.	Yes	Yes	Yes	No	No	Yes
Freq. Ref.	No	Voltage	Digit	No	No	Clock
Tech.[um]	0.5	0.35	0.5	0.5	0.09	0.13
# phases	1	1	1	4	4	1
V_{IN}[V]	1.4-4.2	3.0	2.7	4.8	1.2	1.2
V_{OUT}[V]	0.5	1.5	1.5	3.3	0.9	0.8
f[MHz]	~0.14	~0.85	0.78	30	233	180
Peak Eff.[%]	83	94.5	85.6	83	83.2	80
L_{TOT} [µH]	1	4.7	3.9	0.22x4	0.0068x4	0.008
C[µF]	20	10	47	0.008-0.05	0.0025	0.002
I_{MAX}[mA]	250	500	800	1000	300	240
Area[mm^2]	N/A	1.67	4.5	3.3	0.14	0.42

losses and improve light load efficiency while maintaining a predictable spectrum at the output.

A hysteretic controlled dc-dc buck converter with the proposed D-PLL based synchronization scheme was implemented in 130 nm 1.2 V digital CMOS process. The converter operates over a wide frequency range of 90–240 MHz and achieves a conversion range of 33% to 80%, or 0.4 V to 0.96 V. Using a single inductor ($8.2\text{ n} \sim 24$ nH) and 25 nF capacitor, the converter achieves a load response of 40 ns to a 120 mA step, and a peak efficiency of 80% at 180 MHz for load current of 200 mA.

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