AN1089
APPLICATION NOTE

CONTROL LOOP MODELING OF L6561-BASED TM PFC

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This paper provides a model and a tool for evaluating and improving the control loop characteristics of L6561-based PFC preregulators in boost topology and operated in Transition Mode (TM).

Such a subject is now becoming topical since TM PFC preregulators are more and more used in systems other than electronic lamp ballast where the input voltage range is limited and the load current is almost constant.

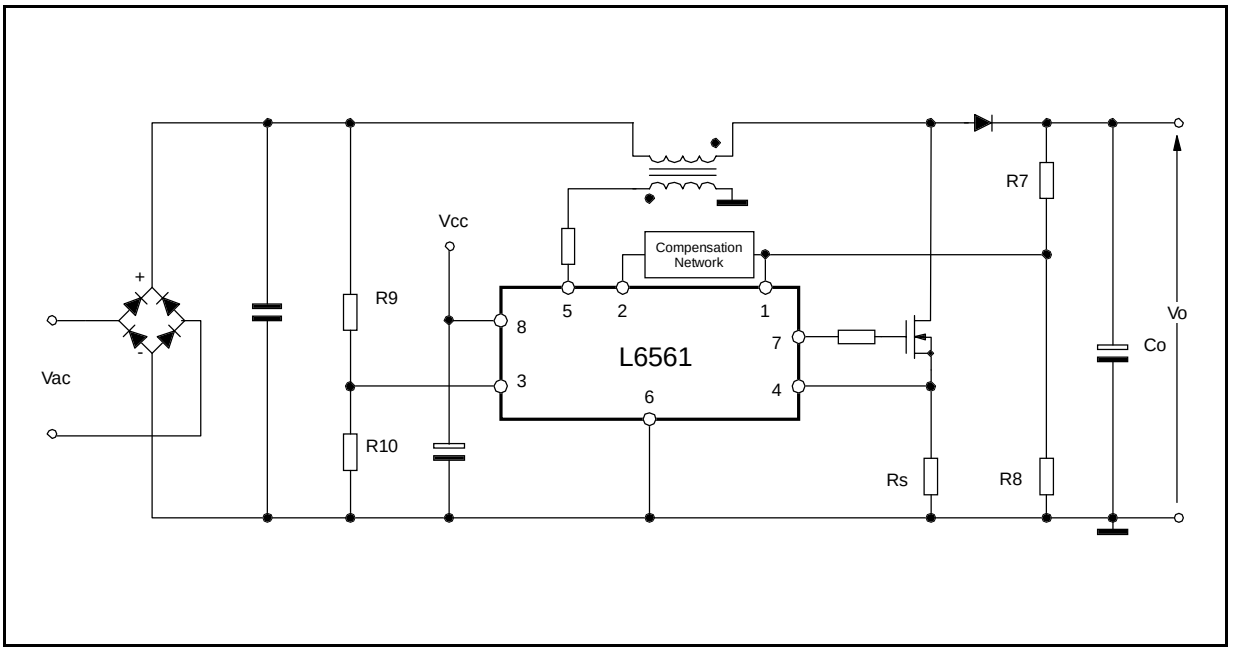
The ability to operate under large variations of both input voltage and load current, as well as the use of TM PFC systems as preregulators for switching converters, requires a more accurate design of the control loop. The goal will be not only to ensure a narrow bandwidth in order to achieve a high Power Factor, but also to have enough phase margin so as to make sure the system is stable over a large range of operating conditions.

INTRODUCTION

PFC preregulators based on the boost topology working in Transition Mode (TM, see fig. 1) have been widespread in electronic lamp ballast systems. This kind of equipment almost always works under a single mains supply (110 or 220 VAC, with some tolerance) and the use of a PFC preregulator is mainly aimed at optimising the downstream half-bridge lamp driver and improving their inherent extremely poor PF.

The PFC preregulator sees the downstream stage as a constant load, so it is requested to work under a limited range of operating conditions. From the control loop standpoint, this means that the frequency compensation of the error amplifier can be very simple, typically just a feedback capacitor. Its capacitance will be high enough to ensure the crossover frequency of the open loop gain is low, so as to achieve a high PF (see Ref. [1]).

Figure 1. Typical L6561-based TM PFC preregulator



Things get more complicated when an electronic ballast can supply two lamps and is required to work even if one lamp is not used or is exhausted, so that it is expected to work at half load as well.

The L6561, thanks to its highly linear, wide dynamics multiplier, extends the use of TM PFC boost pre-regulators to applications that experience a wide range of operating conditions, both in terms of input voltage variations and load change. High power (60 to70 W) AC-DC adapters for portable equipment and computer monitor SMPS' are the most noticeable examples.

This, however, calls for a more accurate design of the control loop than the one illustrated in Ref.[1]. The control goal will no longer be to achieve only a low crossover frequency but also an adequate phase margin. Besides ensuring stability over a large variety of operating conditions, this is necessary to prevent dangerous oscillations of the output voltage as a result of load changes.

PFC Boost Preregulator Control Loop

To the aim of finding a compensation network able to achieve the above mentioned control goal, it is necessary to get an insight into the control loop of such systems. This can be synthesised as shown in the block diagram of fig. 2.

Figure 2. Control loop of a PFC Preregulator: Block Diagram

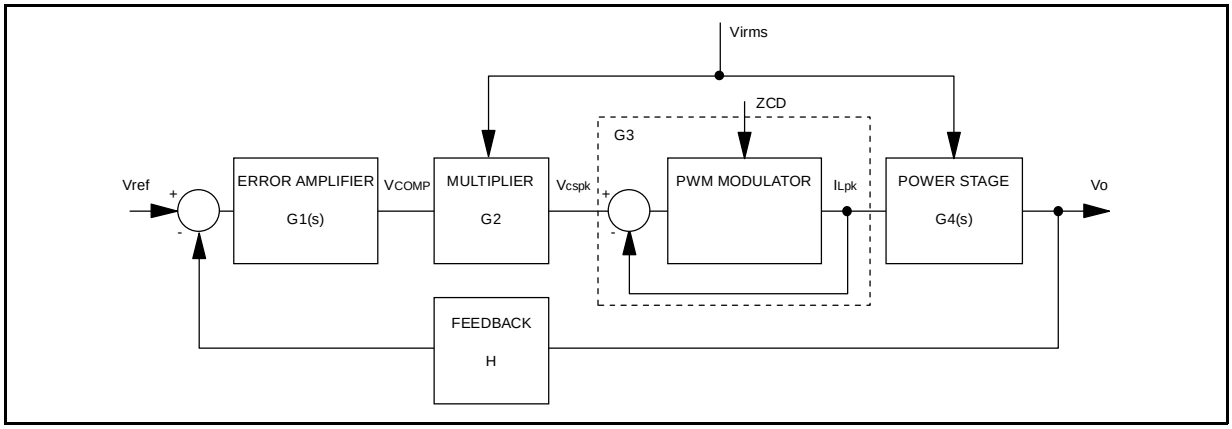


Figure 3. Control loop of a PFC Preregulator: electrical circuit and main quantities

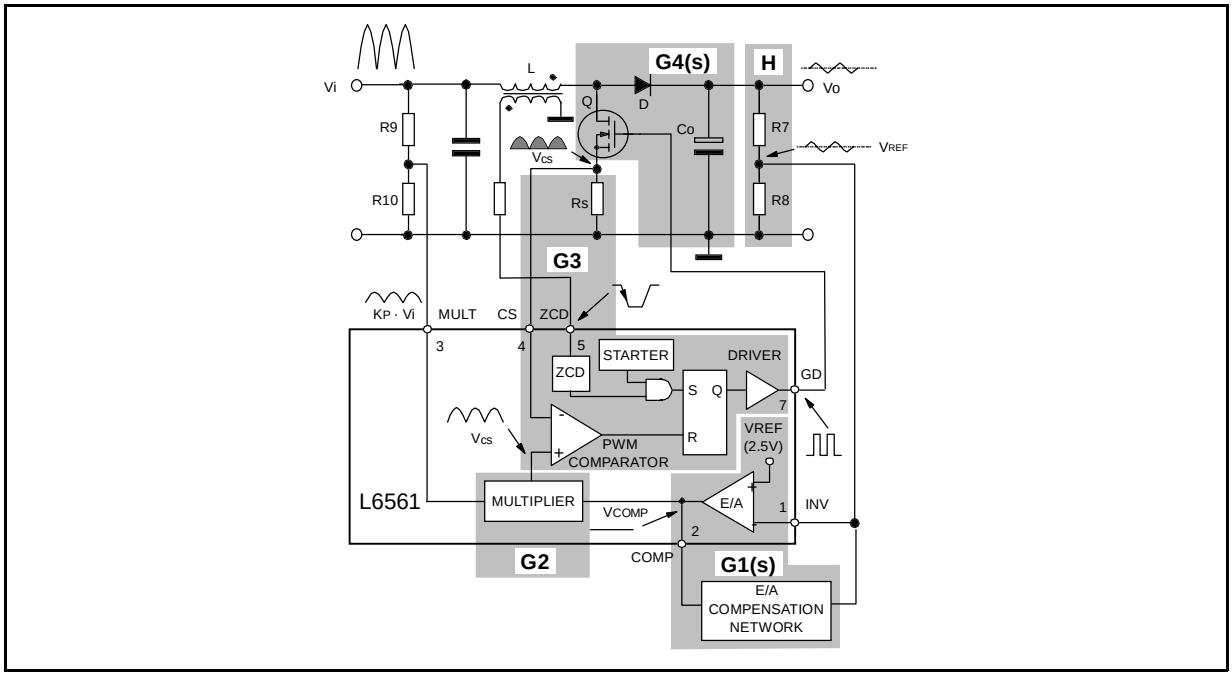


Fig. 3 illustrates how the various blocks of fig. 2 relate with the electrical circuit, both external and inside the L6561. For details on the internal circuit and its operation please refer to Ref. [1].

The loop gain of PFC preregulators must have a very low crossover frequency (fc) so as to maintain V_{COMP} (Error Amplifier output) fairly constant over a given line cycle and ensure a high PF.

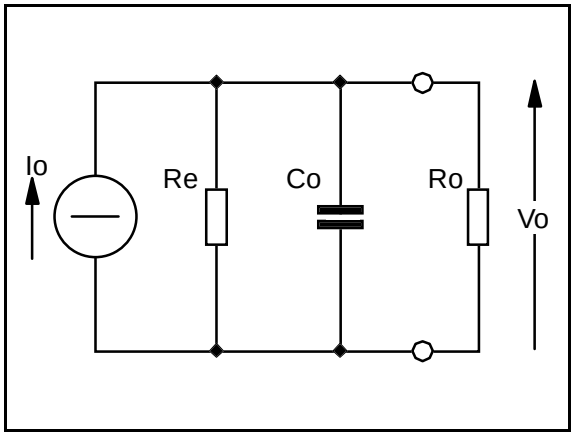
As a rule of thumb, fc should not exceed 20-25 Hz at maximum mains voltage.

This allows to assume that the control action takes place on the peak amplitude (or, which is the same, the RMS value) of the various quantities inside the loop.

The first step is to determine the transfer function of the power stage, G4(s), defined as:

$$G4(s) = \frac{dV_o}{dI_{Lpk}} = \frac{dV_o}{dI_o} \cdot \frac{dI_o}{dI_{Lpk}}$$

Figure 4. Power stage model,G4(s)



where Vo is the DC output voltage, Io the DC output current and I_{Lpk} is the peak value of the inductor current.

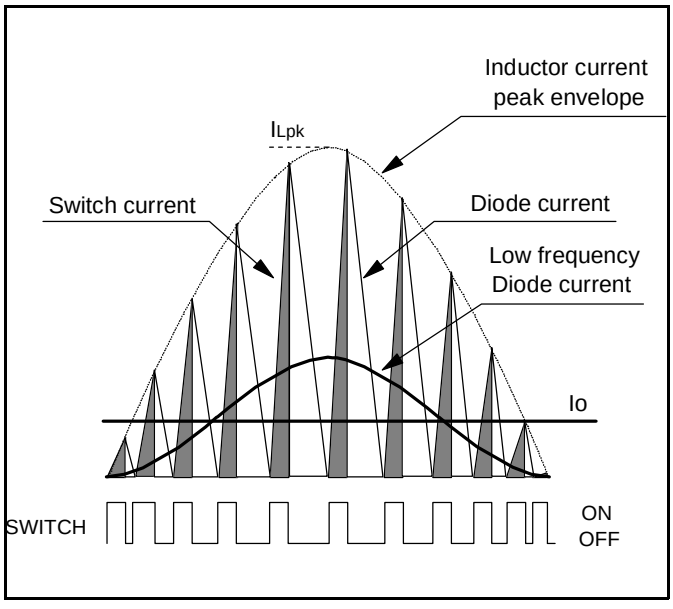
Under the above assumption, the power stage can be modeled as illustrated in fig. 4: a controlled current source (with a shunt resistor Re) that drives the output bulk capacitor Co and the load resistance Ro (= Vo / Io). The zero due to the ESR associated with Co is far beyond the crossover frequency thus it is neglected.

The current source can be characterised with the following considerations: the low frequency component of the boost diode current is found by averaging the discharge portion of the inductor current (the white triangles of fig. 5) over a given switching cycle.

The low frequency current, averaged over a mains half-cycle yields the DC output current Io:

$$I_o = \frac{1}{2} \cdot \overline{(1 - D) \cdot I_{Lpk} \cdot \sin\theta} = \frac{1}{2} \cdot \frac{\overline{\sqrt{2} \cdot V_{irms} \cdot \sin\theta \cdot I_{Lpk} \cdot \sin\theta}}{V_o} = \frac{\sqrt{2}}{4} \cdot \frac{V_{irms} \cdot I_{Lpk}}{V_o}$$

Figure 5. Boost PFC currents



where D is the switch duty cycle, θ is the instantaneous phase angle of the mains voltage and V_{irms} its effective (RMS) value.

The AC model illustrated in fig. 4 can be found by calculating the total differential of the above expression of Io. A few algebraic manipulations would show that the shunt resistor Re always equals the DC load resistance Ro, thus it changes depending on the power delivered by the system. Now it is necessary to consider two separate cases.

If the load is purely resistive (or equivalent to a resistor, like in the case of a lamp ballast circuit), the AC load resistance equals Ro. The parallel of this resistance with Re, combined with the output bulk capacitor, gives origin to a pole located at:

$$\omega_p = \frac{2}{R_o \cdot C_o}$$

which is usually in the range of 1 to 5 Hz.

In case the PFC preregulator provides a DC bus supplying a downstream switching converter, the load should be regarded as a "constant power" load rather than a resistor. In fact, as long as a switching converter is in regulation, the power it demands of the source is practically independent of the input voltage (converter's efficiency changes very little).

In this case, the AC load resistance is equal to -Ro (if the DC bus decreases the current demanded of the PFC increases, whence the negative sign). As a result, the parallel combination with Re tends to infinity and the two resistances cancel. The current source drives only the output capacitor and the pole location tends to zero. In the end, G4(s) will be given by:

$$G4(s) = \begin{cases} \frac{\sqrt{2}}{8} \cdot \frac{V_{irms}}{V_o} \cdot \frac{R_o}{1 + s \cdot \frac{R_o \cdot C_o}{2}} & \text{(resistive load)} \\ \frac{\sqrt{2}}{4} \cdot \frac{V_{irms}}{V_o} \cdot \frac{1}{s \cdot C_o} & \text{(constant power load)} \end{cases}$$

The gain of the PWM modulator, G3, which includes the current loop, is simply:

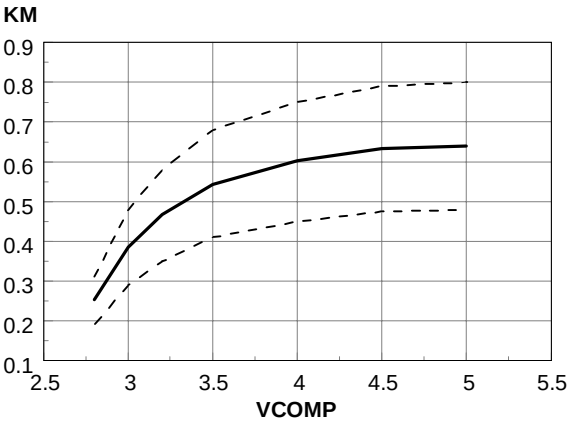
$$G3 = \frac{dI_{Lpk}}{dV_{cspk}} = \frac{1}{R_s}$$

where R_S is the sense resistor connected between the source of the external MOSFET and ground (across which the L6561 reads the inductor current through pin 3).

To calculate the transfer function G2 of the multiplier block, one can consider that a variation ΔV_{COMP}, due to a line and/or load change, modifies the peak amplitude Vcspk of the rectified sinusoid at the output of the multiplier.
Therefore:

$$G2 = \frac{dV_{cspk}}{dV_{COMP}} = K_M \cdot K_P \cdot \sqrt{2} \cdot V_{irms}$$

Figure 6. Plot of K_M vs. E/A output



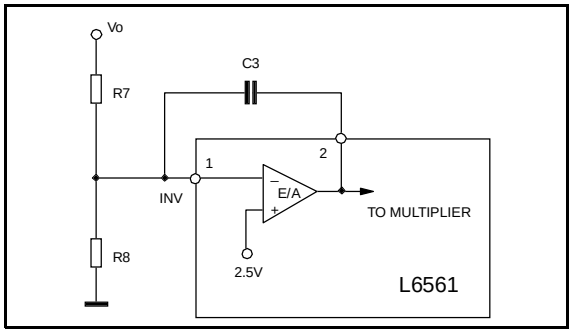
where K_M is the gain of the multiplier and K_P the partition ratio of the resistor divider that feeds a portion of the input voltage into pin 3.

The electrical characteristics of the L6561 specify K_M = 0.6 ±25% (@V_{COMP} = 4V, including temperature) but actually K_M decreases for low values of V_{COMP}. In fig. 6 the typical value of K_M is plotted against V_{COMP} along with the tolerance limits. Since V_{COMP} gets lower when the mains voltage is high, this variation of K_M partly compensates for the increase of G2 with V_{irms}, thus providing a mild voltage feedforward effect.
If one wants to take this non-linearity into account, he or she should linearise the large-signal multiplier gain in the neighborhood of the quiescent point of the error amplifier, so as to get the small-signal gain (km). Please refer to [1] and the Appendix for the relevant calculation technique.
Ultimately, the control-to-output transfer function will be:

$$G(s) = \frac{dV_O}{dV_{COMP}} = G2 \cdot G3 \cdot G4(s) = \begin{cases} \frac{1}{4} \cdot \frac{km \cdot K_P \cdot V^2_{irms}}{V_O} \cdot \frac{R_o}{R_s} \cdot \frac{1}{1 + s \cdot \frac{R_O \cdot C_O}{2}} & \text{(resistive load)} \\ \frac{1}{2} \cdot \frac{km \cdot K_P \cdot V^2_{irms}}{R_s \cdot V_O} \cdot \frac{1}{s \cdot C_O} & \text{(constant power load)} \end{cases}$$

where the small-signal multiplier gain km could be assumed equal to K_M for simplicity.

Figure 7. Typical compensation scheme in PFC preregulators for lamp ballast



From the above equations, it is apparent that the gain of the control-to-output function is strongly dependent on the input voltage, despite the slight compensation provided by K_M. For design purpose, G(s) will have to be considered at the maximum mains voltage, where the gain is maximum and the loop bandwidth is maximum as well.

The feedback block is usually made up of a simple resistor divider (see fig. 7). Only the upper resistor R7 is significant to the loop gain (the lower resistor R8 just sets the value of Vo). It is then convenient to assume H=1 and to consider R7 as a part of the error amplifier block G1(s).

Error Amplifier Compensation

In PFC preregulators that supply an electronic lamp ballast the error amplifier is compensated typically as shown in fig. 7 (see also Ref. [2] and [3]).

For this kind of load this circuit gives satisfactory results. It may not be acceptable, however, in other systems where stability must be ensured over a wide range of input voltage and load current, and does not work at all when the PFC preregulator supplies a switching converter.

Figure 8 shows the suggested compensation schemes for both the cases under consideration.

With a resistive load the loop can be stabilised by adding a pole in the origin plus a low frequency zero that compensates the pole of the control-to-output gain (network a). Ideally, this can give the desired bandwidth with 90° phase margin as well as high DC gain for good load regulation.

With a constant power load the control-to-output gain has a pole in the origin thus the DC gain of the error amplifier should be externally limited with a feedback resistor. If not, a second pole in the origin would be introduced, which would result in a system whose stability might be critical.

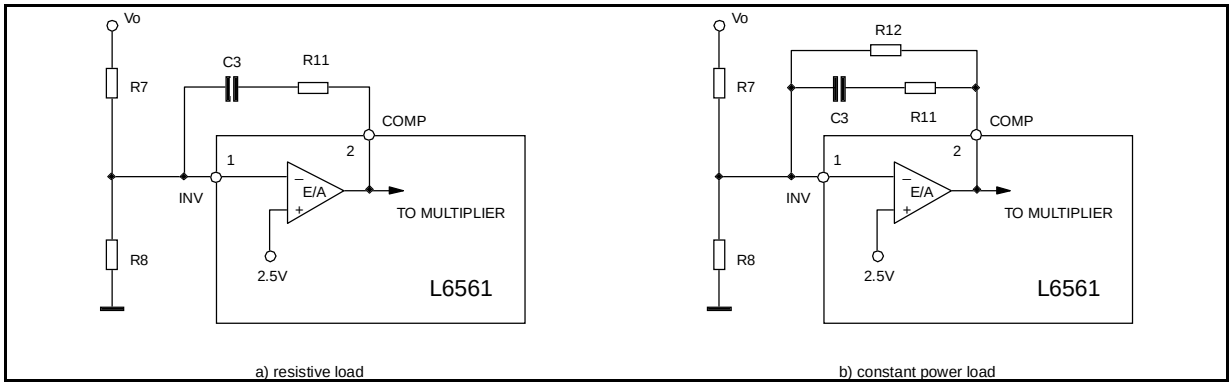
Limiting the gain goes to the detriment of preregulator's load regulation but this has not a serious impact on the overall system since the downstream converter will easily compensate for that.

The compensation network (b) adds a pole-zero couple that both makes the gain roll off at low frequency (so as to cross the 0 dB axis at low frequency) and boosts the phase in the neighborhood of the crossover frequency (so as to increase phase margin).

The transfer functions of the compensation networks of fig. 8 a) and b) are respectively:

$$G1(s) = \frac{dV_{COMP}}{dV_O} = \begin{cases} \dfrac{1 + s \cdot C3 \cdot R11}{s \cdot C3 \cdot R7} & \text{(circuit a – resistive load)} \\ \dfrac{R12}{R7} \cdot \dfrac{1 + s \cdot C3 \cdot R11}{1 + s \cdot C3 \cdot (R11 + R12)} & \text{(circuit b – constant power load)} \end{cases}$$

Figure 8. Suggested compensation networks for TM boost PFC



As a tool to ease the design of L6561's E/A compensation networks in TM boost PFC preregulators, the Appendix contains a Mathcad® file gathering the theory above illustrated and performing all the necessary calculations.

Conclusions

This paper gets an insight into the control loop of TM controlled Boost PFC preregulators based on the L6561 PFC controller. This reveals that the simple feedback capacitor used to compensate the error amplifier in preregulators for lamp ballast may not be adequate in systems that may experience large variations in input voltage and/or load current. Moreover it leads to an unstable loop if the load is a switching converter. Appropriate compensation schemes are suggested for both cases and a calculation tool (Mathcad® file) is provided so as to make control loop design easier in such systems.

References

[1] "L6561, Enhanced Transition Mode Power Factor Corrector", (AN966)

[2] "L6569 - L6561 Lighting Application with PFC" (AN991)

[3] "Electronic Ballast with PFC Using L6574 and L6561" (AN993)

[4] "Design Equations of High-Power-Factor Flyback Converters Based on the L6561" (AN1059)

[5] "Flyback Converters with the L6561 PFC Controller" (AN1060)

Appendix

This Mathcad® file allows to design the control loop and performs a stability analysis of PFC preregulators in boost topology operated in Transition Mode and controlled by the L6561.

Highlighted equations indicate data that must be manually entered. These data are supposted to be known to the user as a result of the design of the PFC preregulator (the use of the PFC design software included in the CD-ROM "Linear and Switching Voltage Regulators" is recommended). The example values are taken from the L6561 demo board circuit.

PFC Converter Data:

Output Voltage	$V_O := 400$	V
Output Capacitor	$C_O := 47$	µF
Sense Resistor	$R_s := 0.41$	Ω
Output Overvoltage Threshold	$OVP := 40$	V
Expected Efficiency	$\eta := 0.9$	

Multiplier Biasing:

Input Divider Upper Resistor	$R_{up} := 1240$	kΩ
Input Divider Lower Resistor	$R_{low} := 10$	kΩ

Analysis Setpoint:

Mains RMS Voltage	$V_{irms} := 264$	V
Output Power	$P_O := 80$	W

Preliminary calculations & Service Variables:

Equivalent Load Resistance $R_o := \frac{V_O^2}{P_O}$ $R_O = 2 \cdot 10^3$ Ω

Input Divider Gain $KP := \frac{R_{low}}{R_{low} + R_{up}}$ $KP = 8 \cdot 10^{-3}$

Large-signal Multiplier Gain: $KM(V_{COMP}) := 0.651 \cdot (1 - 85.29 \cdot e^{-1.776 \cdot VCOMP})$

Error Amplifier Quiescent Point: $V_{COMP} := 4$

$$V_{COMP} := \text{root}\left(2.5 + \frac{2 \cdot P_o \cdot R_S}{\eta \cdot KM(V_{COMP}) \cdot KP \cdot V_{irms}^2} - V_{COMP}, V_{COMP}\right)$$

$V_{COMP} = 2.898$ [V]

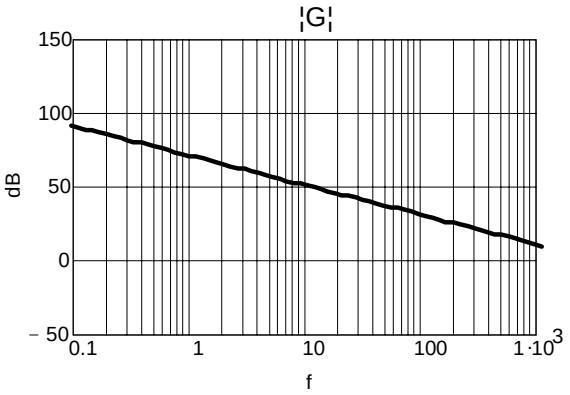
Small signal Multiplier Gain $km := \frac{d}{dV_{COMP}} [KM(V_{COMP}) \cdot (V_{COMP} - 2.5)]$

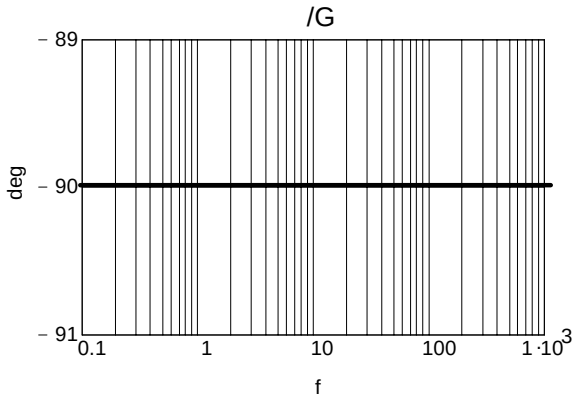
$km = 0.557$

$j := \sqrt{-1}$ $n := 100$ $Dec := 6$ $w := 0,1..n$ $\omega(w) := 10^{w \cdot \frac{Dec}{n} - 1}$ $f := 1$

Control-to-Output Transfer Function (constant power load):

$$G(\omega) := \frac{km \cdot KP \cdot V_{irms}^2}{2 \cdot V_O} \cdot \frac{1}{R_S} \cdot \frac{10^6}{j \cdot \omega \cdot C_O}$$



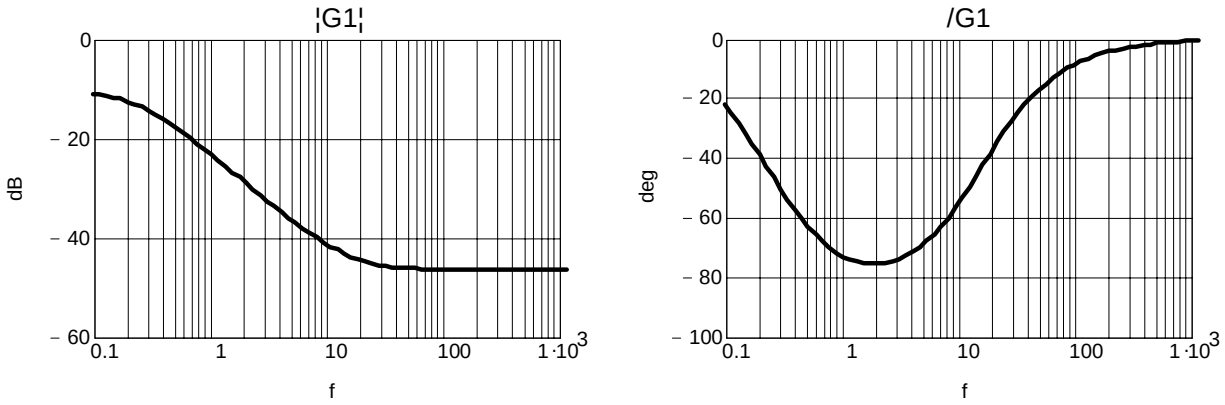


Compensated E/A Transfer Function (constant power load, refer to fig.8b)

DC gain ($\Delta V_O/\Delta V_{COMP}$):	$G_O := 0.30$	
Pole:	$p := 0.23$	Hz
Zero:	$z := 15$	Hz

Transfer Function:

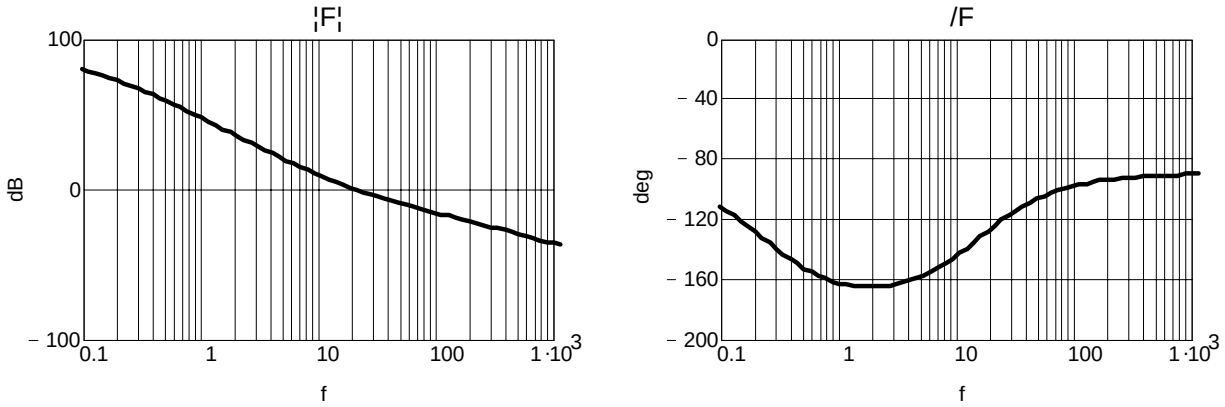
$$G1(\omega) := G_O \cdot \frac{1 + j \cdot \frac{\omega}{2 \cdot \pi \cdot z}}{1 + j \cdot \frac{\omega}{2 \cdot \pi \cdot p}}$$



Open Loop Transfer Function (constant power load):

$$F(\omega) := G(\omega) \cdot G1(\omega)$$

$$\Phi F(\omega) := \arg(F(\omega)) \cdot \frac{180}{\pi}$$



Crossover Frequency:

$fc := |root(|F(2 \cdot \pi \cdot f)| - 1, f)|$

$fc = 18.836$ Hz

Phase Margin:

$\Phi := 180 + \Phi F(2 \cdot \pi \cdot fc)$

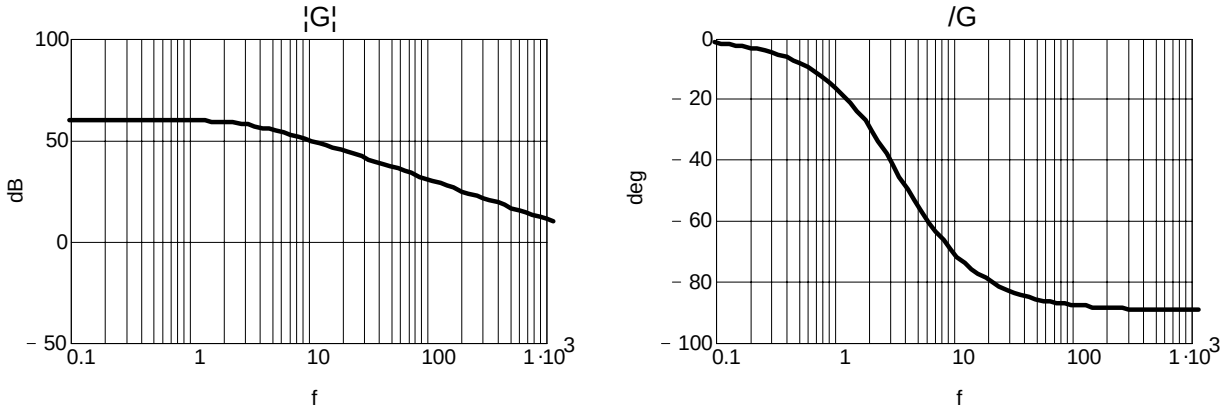
$\Phi = 52.167$ °

Feedback Network Implementation (constant power load, refer to fig. 8b):

Output Divider Upper Resistor	$R7 := \frac{OVP}{40} \cdot 10^3$		
	$R7 = 1 \cdot 10^3$		kΩ
Output Divider Lower Resistor	$R8 := \frac{2.5}{V_O - 2.5} \cdot R7$	R8 = 6.289	kΩ
Parallel Feedback Resistor:	$R12 := G_O \cdot R7$	R12 = 300	kΩ
Series Feedback Capacitor	$C3 := \frac{10^6}{2 \cdot \pi \cdot R12} \cdot \left(\frac{1}{p} \cdot \frac{1}{z}\right)$		
	$C3 = 2.271 \cdot 10^3$		nF
Series Feedback Resistor	$R11 := \frac{10^6}{2 \cdot \pi \cdot z \cdot C3}$	R11 = 4.672	kΩ

Control-to-Output Transfer Function (resistive load):

$$G(\omega) := \frac{km \cdot KP \cdot V_{irms}^2}{4 \cdot V_O} \cdot \frac{R_O}{R_s} \cdot \frac{1}{1 + j \cdot \omega \cdot C_O \cdot \frac{R_O}{2} \cdot 10^{-6}}$$



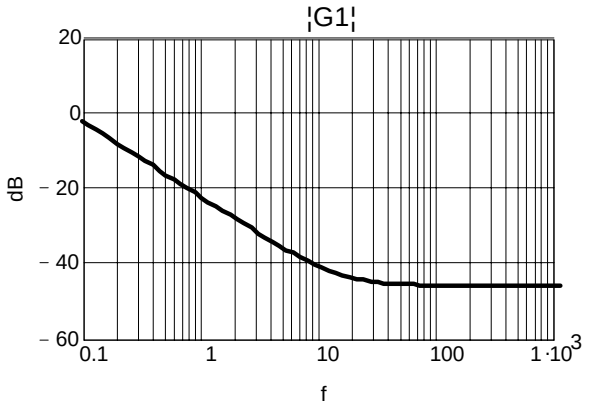
Pole Location:	$p := \frac{10^6}{\pi \cdot R_O \cdot C_O}$	p = 3.386	Hz

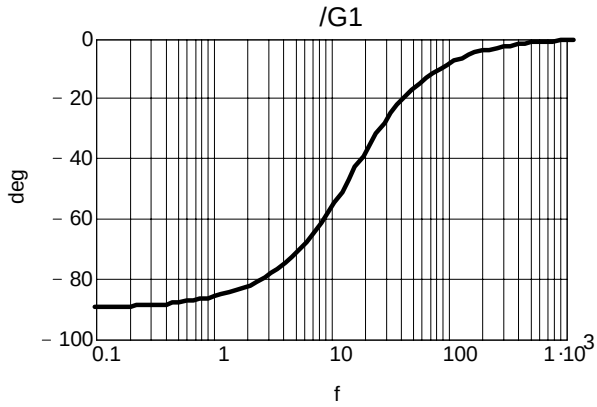
Compensated E/A Transfer Function (resistive Load, refer to fig. 8a):

High Frequency Gain: $G_h := 0.005$

Zero: $z := 15$ Hz

Transfer Function: $G1(\omega) := G_h \cdot 2 \cdot \pi \cdot z \cdot \frac{1 + j \cdot \frac{\omega}{2 \cdot \pi \cdot z}}{j \cdot \omega}$

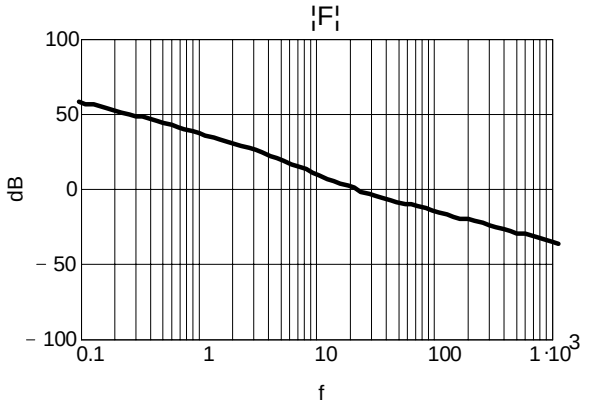


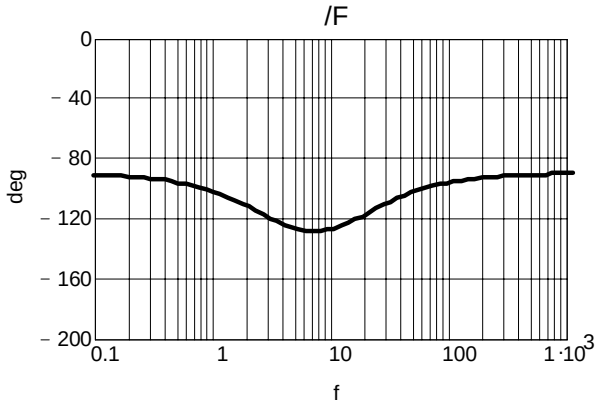


Open Loop Transfer Function (resistive load)

$$F(\omega) := G(\omega) \cdot G1(\omega)$$

$$\Phi F(\omega) := \arg(F(\omega)) \cdot \frac{180}{\pi}$$





Crossover Frequency: $fc := |root(|F(2 \cdot \pi \cdot f)| - 1, f)|$

$fc = 19.805$ Hz

Phase Margin:	$\Phi := 180 + \Phi F(2 \cdot \pi \cdot fc)$		
	$\Phi = 62.563$		°

Feedback Network Implementation (resistive load, refer to fig. 8a):

Equivalent Load Resistance	$R7 := \frac{OVP}{40} \cdot 10^3$	$R7 = 1 \cdot 10^3$	kΩ
Output Divider Lower Resistor	$R8 := \frac{2.5}{V_O - 2.5} \cdot R7$	R8 = 6.289	kΩ
Series Feedback Capacitor	$C3 := \frac{10^6}{2 \cdot \pi \cdot z \cdot Gh \cdot R7}$	$C3 = 2122 \cdot 10^3$	nF
Series Feedback Resistor	$R11 := \frac{10^6}{2 \cdot \pi \cdot z \cdot C3}$	R11 = 5	kΩ