MITSUBISHI LSIs

M50530-XXXFP

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

DESCRIPTION

The M50530-XXXFP is an LSI for a dot matrix liquid crystal display control drive which has been developed by making use of the silicon gate CMOS process, and can control multi-digit data and directly drive a dot matrix liquid crystal display of 256 font types including alphanumerics, kana characters and symbols by a simple control from μc and μp.

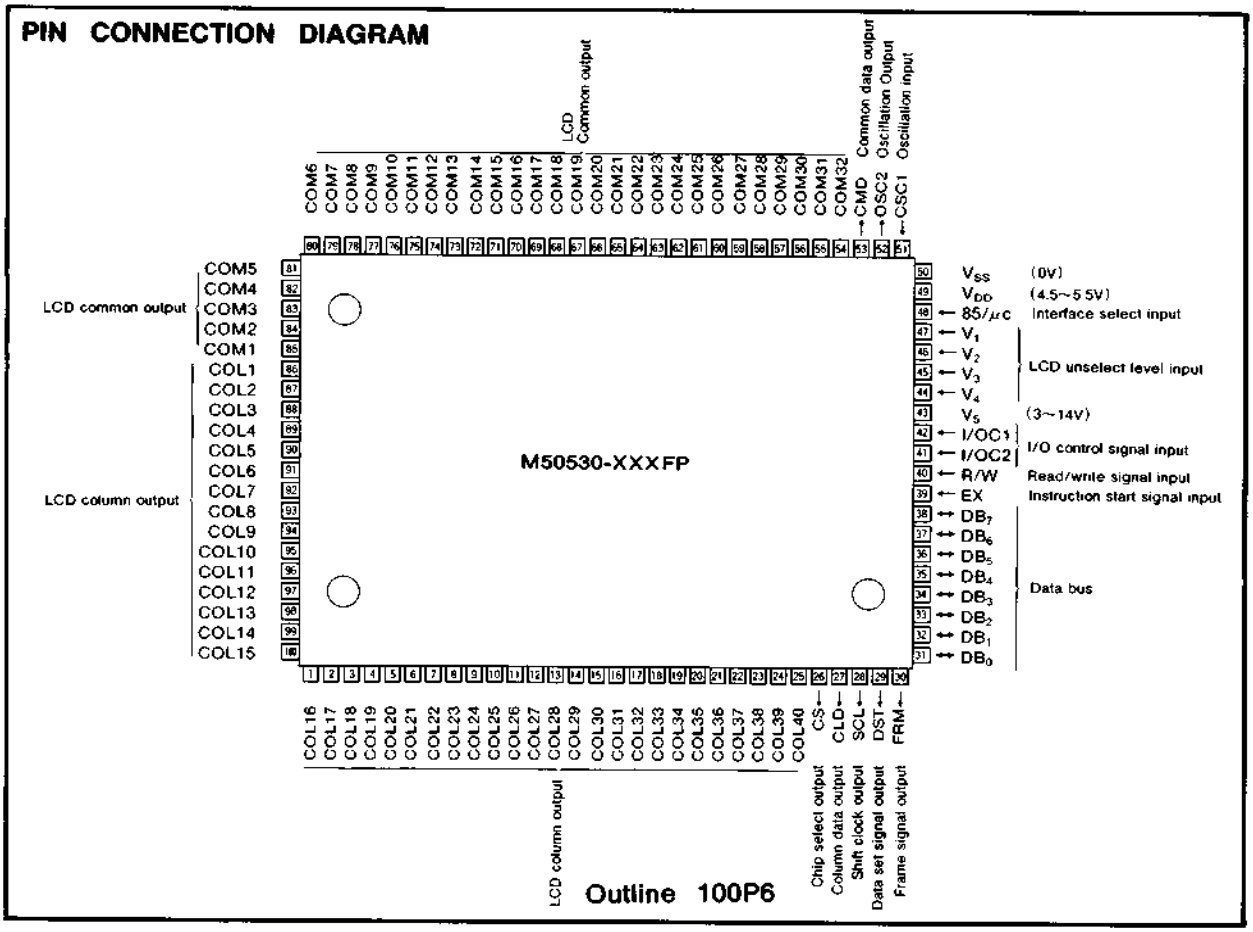
The M50530-XXXFP offers a system for controlling and driving a dot matrix liquid crystal display, and also expands the number of display digits by the simultaneous use of the IC for the liquid crtstal drive, M50521FP or M50524FP.

By using the M50530-XXXFP it has been possible to create a liquid crystal display system which is compact, has low power consumption and is very versatile.

FEATURES

- Interfacing (It is possible to interface directly with a 4-bit μc and an 8-bit μc. It is possible to interface directly with 8085 μp.)
- Characters (256 font types with 5×8 dots or 5×12 dots (cursor is common to both))
- Memory (Generally for a display data RAM and for a character generation RAM, it is possible to use a total of 256 words, with 9 bits to a word, and to select one configuration out of the 4 types described below that offer maximum and minimum configurations.)
  - ◦ Display Data RAM (hereafter referred to as DD RAM)
    9 bits to a word (of these, 1 bit is used to underline)
    ·····4 types from a maximum of 256 words to a minimum of 160 words
  - ◦ Character generator RAM (hereafter referred to as CG RAM)
    5×7 dots·····4 types from a minimum of 0 to a maximum of 12 characters
    or 5×11 dots·····4 types from a minimum of 0 to a maximum of 6 characters
  - ◦ Character generator ROM (hereafter referred to as CG ROM)
    5×7 dots·····4 types from a maximum of 256 to a minimum of 244 characters
    or 5×11 dots·····4 types from a maximum of 256 to a minimum of 250 characters

PIN CONNECTION DIAGRAM



Outline 100P6

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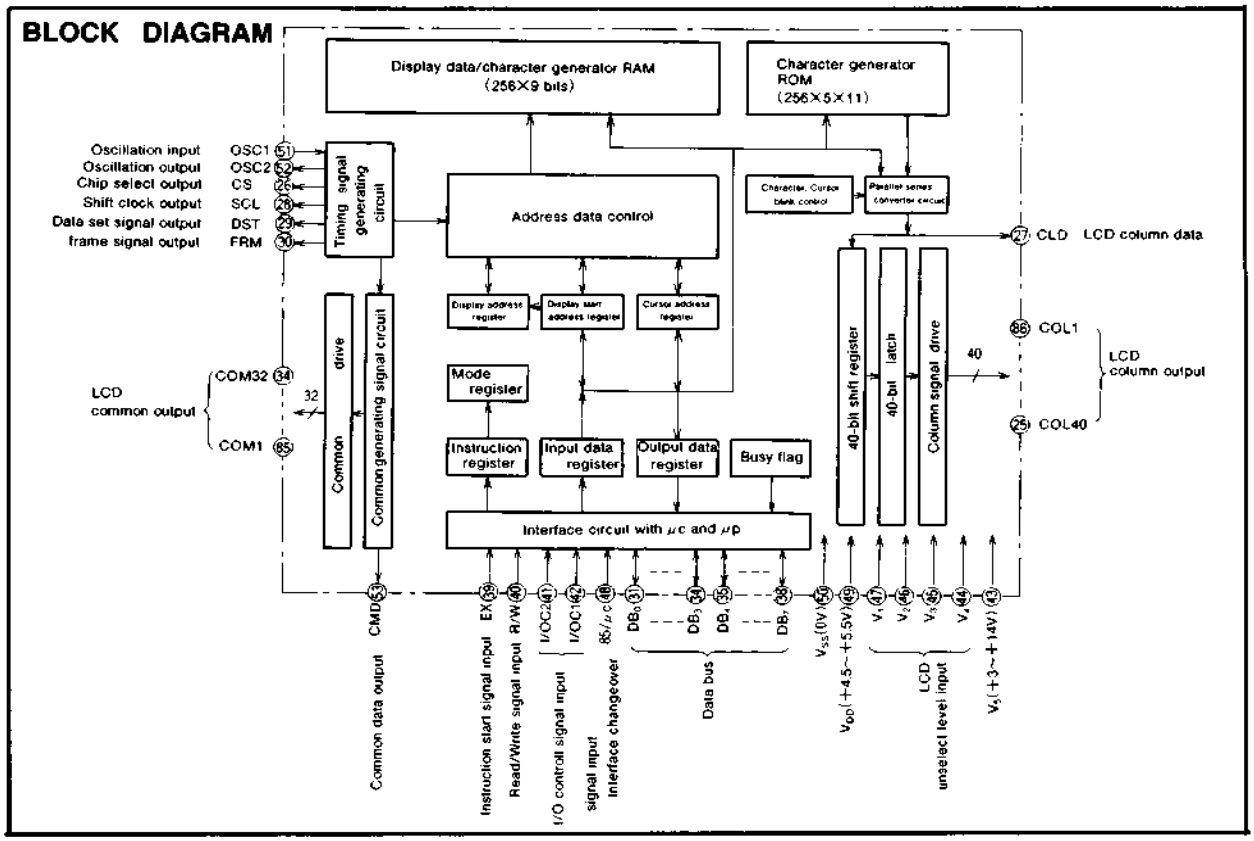
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

- Instructions (The following comprehensive instructions are given.)
  - Cursor address set-up for DD/CG RAM
  - Display start address set-up
  - Data write and read from RAM
  - Display shift and cursor shift
  - Interface changeover between 8-bit μc/4-bit μc
  - Font changeover between 5×8 dots /5×12 dots
  - Duty changeover between (1/8, 1/12), (1/16, 1/24), and (1/32, 1/48)
  - Selection between DD/CG RAM configurations
  - Underline set-up for each character
  - Display ON/OFF, cursor display ON/OFF, underline display ON/OFF, character blink, and cursor blink
  - Blink frequency set-up
  - Display address home and cursor address home
  - Clearing entire display
- Display difgit No. :
  - 1 chip system (8 digits for 1 line, 8 digits for 2 lines, and 8 digits for 4 lines)
  - Maximum system configuration (The 4 following types of maximum system configuration are available for 1 line, 2 line, and 4 lines respectively.)
    1 line 256 digits, 244 digits, 192 digits, and 160 digits
    2 lines ·· 128 digits, 112 digits, 96 digits, and 80 digits
    4 line····· 64 digits, 56 digits, 48 digits, and 40 digits
- Internally provided for liquid crystal display drive circuit
  - Common signal : 32 lines (corresponds to 4-line portion for 1/32 duty)
  - Column signal : 40 lines (corresponds to 8-digit portion for 5 lines per digit)
  - By using the IC for the liquid crystal drive M50521FP or M50524FP, it is possible to expand the display to the maximum number of digits.
- Automatic reset at power cut-off
- Built-in oscillator (An external resistor or an external ceramic filter)
  - Oscillation frequency 2.58MHz (for a frame frequency of about 70Hz)
- Column data transfer speed (1.29Mbit/set [for oscillation frequency of 2.58MHz])
- Blink frequency (About 0.5Hz, 1Hz, 2Hz, and 4Hz [for oscillation frequency of 2.58 MHz])
- Supply voltage for logic circuit : (+4.5~5.5 V)
- Output voltage of liquid crystal drive : (+3~14 V)
- On-resistance of liquid crystal drive : 500Ω (14V) and 2kΩ (5 V), maximum
- Low power consumption : Silicon gate CMOS process
- Package : 100-pin plastic flat QUIP, lead pitch 0.65mm

APPLICATION

OA apparatus (portable personal computer, electical typewriter e.t.c), Information apparatus (Telephone, Fax e.t.c).

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The LSI M50530-XXXFP is controlled by instructions from a μc or μp on the outside. In other words, the μc or μp takes the role of master processor and M50530-XXXFP takes the role of slave processor. M50530-XXXFP can control completely the liquid crystal display (LCD).

When transferring data between the μc or μp and the internal RAM within the M50530-XXXFP first the RAM address is set by an instruction in the cursor address register, then, either external data is written by an instruction in the internal RAM via the internal input data register or data is read by an instruction from the RAM to the outside via the output data register.

M50530-XXXFP has various execution condition modes for instructions such as function construction, display, reading, writing etc. In this way, the efficiency of execution of the instruction has been improved. These different modes are stored by the mode setting instructions in the mode register, and they are used in subsequent instructions as execution conditions.

When RAM data is displayed by LCD, the address of the RAM data to be displayed as the first digit on the left-hand side of the LCD is set with the display start address. First, set by instruction the first digit in the display start address register to the RAM address desired for display. Data is displayed by LCD from this address to successively higher digits.

As regards the LCD drive, a common signal is generated in the timing generation circuit on the scanning side to drive the common side of the LCD via the common signal drive.

The RAM data for display, designated by the address in the display address register is read on the column data side as a character code. The data is then converted to a character pattern in the character generator of the ROM or RAM.

Then, by sending the 5-bit data in the line, which corresponds to the common scanning signal in the line matrix of the character pattern, to the shift register as a column signal, the column side of the LCD is driven via the column singal drive.

In order to display all of the display data by LCD: 1) the display address register is incremented for each of the common signals; 2) display data is read successively from the RAM; 3) column signals for all lilnes of the display are sent, by repeated conversion and transfer, to the column drive; and 4) the column side is driven.

The LCD operation is independent of the execution of an instruction from the outside and is processed within a prescribed time, so that no flickering will be generated in the display regardless of the presence of instructions being executed.

One chip of the M50530-XXXFP can directly drive an 8-digit LCD for 1 line, 2 lines, and 4 lines. However, if a LCD with more digits is desired, it is necessary to connect an external IC for the LCD drive; either M50521FP or M50524FP. These ICs for LCD drive can drive a LCD as a common signal drive or column signal drive. Furthermore, when a large number of these ICs are used, the system is designed such that the data signals can be received only by the IC that is supplied with the chip select signal. This design allows the system can be operated with low power consumption.

The LCD contents are present for a prescribed frame time which is determined by the oscillation frequency, and the time is constant independent of the line number of the display, duty ratio, digit number of the display, and character font.

TERMINAL DESCRIPTION

Pin	Name	I/O	Function
85/μc	Interface changeover signal	I	This is used as a signal for changing over the interface between μc and μp. It should be set to "1" for 8085μp and to "0" for μc mode.
I/OC1	Input/output control signal	I	In the μc mode, this is used as the control signal for sending an instruction from the μc to the M50530-XXXFP, and is used as part of the instruction code. In the 8085μp mode, it is connected to the $\overline{WR}$ signal of the 8085μp.
I/OC2	Input/output control signal	I	In the μc mode, this is used as the control signal for sending an instruction from the μc to the M50530-XXXFP, and is used as part of the instruction code. In the 8085μp mode, it is connected to the IO/M signal of the 8085μp.
R/W	Write/read signal	I	In the μc mode, this is used as the control signal for sending an instruction from the μc to the M50530-XXXFP, and is used as part of the instruction code. It is set to "0" for write instruction and to "1" for read instruction. In the 8085μp mode, it is connected to the RD signal of the 8085μp.
EX	Instruction start signal	I	In the μc mode, this is used as the signal for the μc to cause the M50530-XXXFP to start the execution of an instruction. In the 8085μp mode, it is connected to the ALE signal of the 8085μp.
DB_7~ DB_4	Data bus	I/O	Thses represent the 4 upper lines of the 8 line data buses. They are in tri-state bidirectional mode which enables inputting as well as outputting. These are used for instruction data transfer between the M50530-XXXFP and the μc or μp. When interfacing with the μc is 4 bits, the lower 4 bits data are also transferred by these 4 lines of data buses. The DB_7 is also used for reading a busy flag.
DB_3~ DB_0	Data bus	I/O	These are the 4 lower lines of the 8 line data buses. They are in tri-state bidirectional mode which enables inputting as well as outputting. These are used for instruction data transfer between the M50530-XXXFP and the μc or μp. When interfacing with the μc is 4 bits, these 4 lines are not used.
DST	Data set signal	O	Signal for setting serial data sent to the drive IC to a latch.
SCL	Shift clock signal	O	Clock for successively shifting a serial data set sent to drive IC.
FRM	Frame signal	O	Display frame signal. Used as a changeover signal for driving the liquid crystal by AC power.
CS	Chip select signal	O	Signal for selecting the column drive IC. Data will be transferred only to the drive IC to which this signal is supplied.
CMD	Common data signal	O	Common data signal to be sent to the common drive IC. Connected to chip select of the drive IC
CLD	Column data signal	O	Column data signal to be sent to column drive IC Sends a character pattern serially. Value "0" corresponds to non-selection while "1" corresponds to selection.
COM1~ COM32	LCD Common signal	O	Common signal for driving the scanning side of the liquid crystal. Common signals that are not used are all given the non-select waveform. For instance, if the duty is 1/16, then COM17 to COM32 will always be given non select waveforms.
COL1~ COL40	LCD Column signal	O	Column signal for driving the data side of the liquid crystal. Drives the respective 8-digit portion of the RAM display data of the display start address for each line.
OSC1, OSC2	Oscillation input/output	I/O	Terminal for oscillating internal clock. Connected to a resistor or a ceramic filter. Clock input from outside is supplied to OSC1.
V_1~V_5	Power supply(LCD)	I	Power supply for driving liquid crystal display. Voltages V_{SS}, V_1, V_4, and V_5 are common while V_{SS}, V_2, V_3, and V_5 are for column.
V_{DD}	Power supply(Logic)	I	Power supply for the logic circuit, +5V
V_{SS}	Power supply(GND)	I	Ground power supply, 0V

FUNCTIONAL EXPLANATION OF EACH BLOCK

In the description below, the following abbreviations will be used:
Display data RAM : DD RAM
Character generator RAM : CG RAM
Character generator ROM : CG ROM
Display data/character generator RAM : DD/CG RAM
In abbition, the designations of instructions will follow the abbreviations given in the instruction list. Use will also be made of the instruction code names in the instruction list.
The relationship between the binary logic values and the voltage levels is as given below.
Binary number 0 : Low voltage level
Binary number 1 : High voltage level
Furthermore, the following notations will be employed.
( )n means that the numerical value within the parentheses is that of the n-ary notation, namely, the number system in which n is used as the radix.
R( )n means the content of the RAM address ( )n.
It should be noted that unless otherwise stated, numerical values without suffix are meant for decimal notation.
For instance,
$(8F)_{16} \equiv (10001111)_2 \equiv (143)_{10} \equiv 143$, and
$R(8F)_{16} \equiv R(10001111)_2 \equiv R(143)$ means the content of the address 143 fo the RAM.

1 INTERFACE CIRCUITS FOR μc AND μp

These are the circuits for controlling input and output when instructions and data are transferred between the M50530-XXXFP and external μc or μp that control the M50530-XXXFP.
By means of the input signal 85/μc, it is possible to select either 8085 μp or μc as an external control.
When μc is selected, it is further possible to select 8-bit μc or 4-bit μc by the instruction SF. For the transfer of an instruction code from the 8-bit μc to the M50530-XXXFP, the input signals I/OC1, I/OC2, R/W, and the input/output signals DB_7 to DB_0, are used and the input signal EX are used for starting the execution of the instruction. For the transfer of an isntruction code from the 4-bit μc to the M50530-XXXFP, the input signals I/OC1, I/OC2, R/W, and the input/output signals DB_7 to DB_4, are used twice. The input signal EX are also used twice for starting the execution of the instruction. In other words, in the 8-bit μc, the data buses DB_7 to DB_0 with 8 bits are used, and in the case of the 4-bit μc, the data buses DB_7 to DB_4 with 4 bits are used.
When the 8085 μp is selected, by connecting the signals AD_7 to AD_0, ALE, RD, WR, and IO/M of the 8085 μp to the signals DB_7 to DB_0, EX, R/W, I/OC1 and I/OC2, respectively, of the M50530-XXXFP, it is possible to control directly the M50530-XXXFP by producing an instruction code for M50530-XXXFP using the input/output instructions for 8085 μp.
The external μc and μp and the M50530-XXXFP operate asynchronously. Accordingly, there is no need for the inputs from the μc and μp to be synchronous with the internal clock of M50530-XXXFP. Furthermore, the handling of the interface for the signals from the external μc and μp, or the execution of the instructions from the μc and μp, will in no way affect the LCD processing within M50530-XXXFP. Therefore, no flickering will be generated in the display due to inputs from the μc and μp.

2 BUSY FLAG

When the M50530-XXXFP is executing an instruction, the busy flag will show $(1)_2$.
When the busy flag is at $(1)_2$, no instruction from the μp or μc will be accepted. Therefore, it is necessary to give an instruction to M50530-XXXFP after confirming that the busy flag is $(0)_2$.
However, the busy flag read instruction alone, RB, can always be used even when another instruction is being executed, and by using the instruction RB, the condition of the busy flag can be read from DB_7 and DB_3.

3 INSTRUCTION REGISTER AND MODE REGISTER

An instruction from the μp or μc enters the instruction register via the μc and μp interface circuits. The instruction is executed when its content has been decoded.
Among the included instructions are those which can set up the following modes.
Instruction SF : 8-bit/4-bit interface
5 × 8 dots / 5 × 12 dots font display line number, RAM region
Instruction SE : Cursor shift mode, display shift mode
Instruction SD : Display mode, blink mode
Instruction SU : Underline write mode
Instruction SB : Blink frequency
The mode register stores the information of these modes. These modes are used as conditions for execution of the instructions.

4 INPUT REGISTER AND OUTPUT REGISTER

The input data is entered into the input data register by the write instructions WC, WS, WD, and WU, and is transferred to the interior upon execution of the instruction.
Output data is outputted from the output data register to the μp or μc by the read instructions RC, RS, and RD. The output data for these instructions is prepared beforehand in the output data register.

5 CURSOR ADDRESS REGISTER

This is the register for specifying the DD/CG RAM address. In order to write data into the RAM using the instruction WD, or read data from the RAM using the instruction RD, or

add an underline to the RAM using instruction WU, it is necessary to set, beforehand, the address of the RAM in the cursor address register. With the instruction WC it is possible to set data in the cursor address register. Also the content of the cursor address register can be read using the isntruction RC.

By incrementing (+1) or by decrementing (−1) the content of the cursor address register using the instruction MA, it is possible to shift the cursor address to the RAM in the upward or the downward direction.

After writing or reading the data using the instructions WD or RD and the entry mode has been specified by the instruction SE, the content of the cursor address register can be automatically incremented (+1) or decremented (−1) as shown in table 1.

Table 1. Instruction SE and cursor address

Instruction SE CSR CONDITION (W)	(R)	Automatic INC/DEC of the Cursor Address
0	0	No automatic inc or dec
0	1	Inc or dec after execution of instruction RD
1	0	Inc or dec after execution of instruction WD
1	1	Inc or dec after execution of instruction RD and WD

The increment and decrement of the cursor address register are executed within the display data region and the character generator region, respectively, of the RAM.

The Fig. 1 is an example (of 4 kinds of configurations) in which the RAM is divided into the display data region and

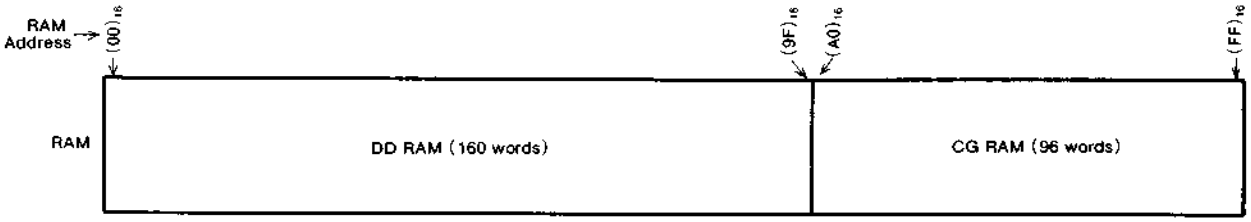


Fig.1 Example of dividing RAM

the character generation region. The increment and the decrement of the cursor address is as shown on the boundaries of the respective regions are as shown in table 2.

Table 2. Cursor Address

RAM Region	Cursor Address		
	Before inc/dec	After inc	After dec
DD RAM	$(00)_{16}$	$(01)_{16}$	$(9F)_{16}$
	$(9F)_{16}$	$(00)_{16}$	$(9E)_{16}$
CG RAM	$(A0)_{16}$	$(A1)_{16}$	$(FF)_{16}$
	$(FF)_{16}$	$(A0)_{16}$	$(FE)_{16}$

The boundary conditions in the increment and the decrement of the cursor address are displayed in 2 lined and 4 lines so that the conditions will remain the same as in the above table even when the RAM region is further subdivided.

6 DISPLAY START ADDRESS REGISTER

This is the register for determining the relative relationship between the position of the displayed character in the LCD and the address of the DD RAM in which the character is written.

The content of the display start address register designates the address of the RAM in which the character code of the character to be displayed in the first digit on the left end of the LCD.

The range of the display start address varies with the size of the RAM region and the number of displayed lines.

In the case of 2-line display, the display start addressed for the first line and the second line have a common value, and in the case of 4-line display, the display start addresses for the first through fourth lines have a common value. In the case of display of more than 2 lines, the value of the display start address of the first line is used as the value of the display start address. Accordingly, the range of the display start address is given depending upon the size of the RAM region and the number of display lines, as table 3.

Table 3. Range of display start address

Instruction SF		DD RAM Region	Range of Display Start Address		
RA_1	RA_0		1-line Display	2-line Display	4-line Display
0	0	256 words $(00)_{16}$~$(FF)_{16}$	$(00)_{16}$~$(FF)_{16}$	$(00)_{16}$~$(7F)_{16}$	$(00)_{16}$~$(3F)_{16}$
0	1	224 words $(00)_{16}$~$(DF)_{16}$	$(00)_{16}$~$(DF)_{16}$	$(00)_{16}$~$(6F)_{16}$	$(00)_{16}$~$(37)_{16}$
1	0	192 words $(00)_{16}$~$(BF)_{16}$	$(00)_{16}$~$(BF)_{16}$	$(00)_{16}$~$(5F)_{16}$	$(00)_{16}$~$(2F)_{16}$
1	1	160 words $(00)_{16}$~$(9F)_{16}$	$(00)_{16}$~$(9F)_{16}$	$(00)_{16}$~$(4F)_{16}$	$(00)_{16}$~$(27)_{16}$

By setting a display start address in the display start address register with the instruction WS, it is possible to display starting with the first digit of the LCD, from an arbitrary address of the DD RAM.

The content of the display start address register can be read with the instruction RS.

By incrementing (+1) or decrementing (−1) the content of the display start address register with the instruction MA, the position of the liquid crystal display with respect to the

RAM can be shifted upward or downward.
After writing or reading the data with the instruction WD or RD, it is possible to automatically increment (+1) or decrement (−1) the content of the display start address register by designating the entry mode with the instruction SE. This is shown in table 4.

Table 4. Instruction SE and display start address

Instruction SE DSP CONDITION (W)	(R)	Automatic inc/dec of Display Start Address
0	0	No automatic inc or dec
0	1	Inc or dec after execution of the instruction RD
1	0	Inc or dec after execution of the instruction WD
1	1	Inc or dec after execution of the instructions RD and WD

The increment and the decrement of the content of the display start address register are executed within the data region for the first line in the display data region of the RAM.
The relation between the RAM address and the content of the display start address register will now be explained, when the RAM is divided into 160 words of DD RAM and 96 words of the CG RAM (one of the 4 possible configurations).

An example of the case of 1-line of LCD (for 160 words of DD RAM and 96 words of CG RAM) ; Fig. 2.

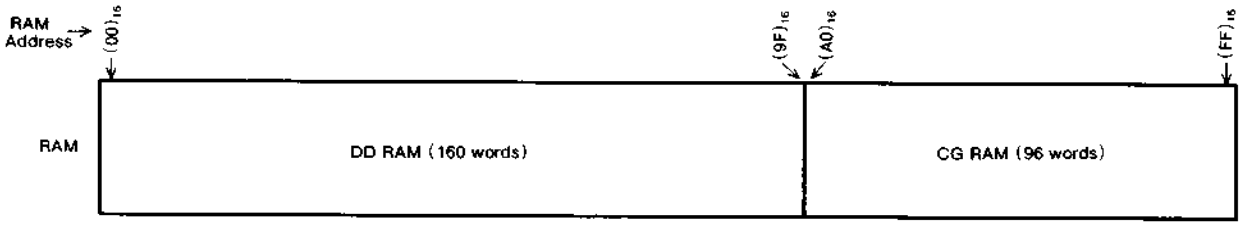


Fig.2 DD/CG RAM

When the content of the display start address register is $(17)_{16}$, the liquid crystal display will be as Fig. 3.

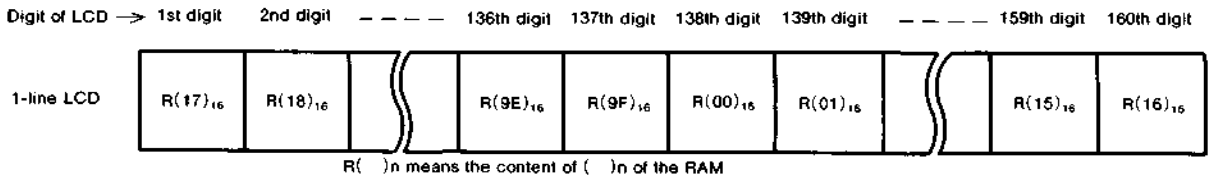


Fig.3 Example of display address

Here, if the content of the display start address register is incremented (+1), the result becomes $(18)_{16}$, and the LCD display will be given by Fig. 4.

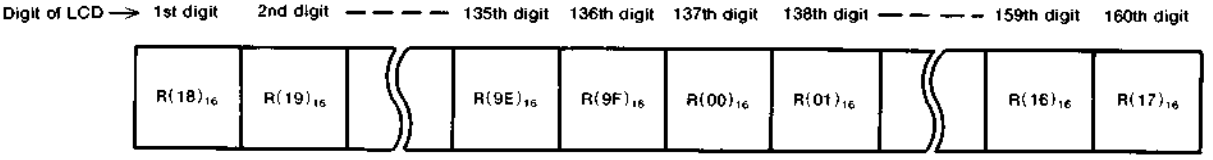


Fig.4 Example of display address

Visually, the content of the displayed content looks as if it is shifted to the left. Similarly, when the content of the display start address register is decremented, the displayed content looks as if it is shifted to the right. When the display start address is situated on the boundary of the display data region of the RAM, if the display start address is incremented or decremented, the result will be as shown in table 5.

Table 5. Change of display start address

Display Start Address		
Before inc/dec	After inc	After dec
$(00)_{16}$	$(01)_{16}$	$(9F)_{16}$
$(9F)_{16}$	$(00)_{16}$	$(9E)_{16}$

An example of the case of 2-line of LCD (for 160 words of DD RAM and 96 words of CG RAM) ; Fig. 5.

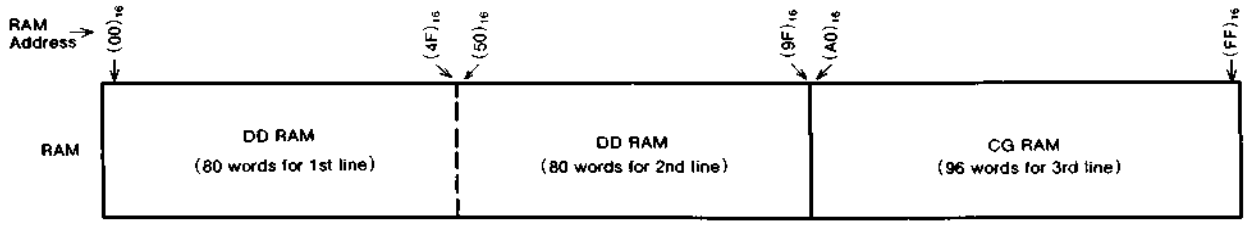


Fig.5 DD/CG RAM

When the content of the display start address register is $(17)_{16}$, the LCD is given by Fig. 6.

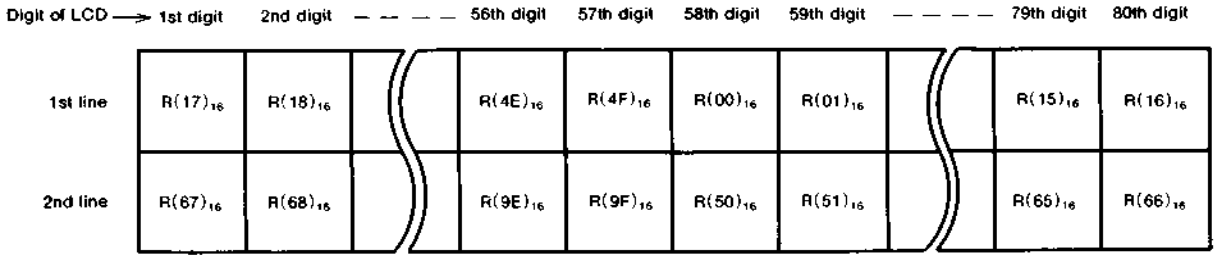


Fig.6 Example of display address

When the content of the display start address register is incremented, the result becomes $(18)_{16}$, and the LCD becomes as shown in Fig. 7

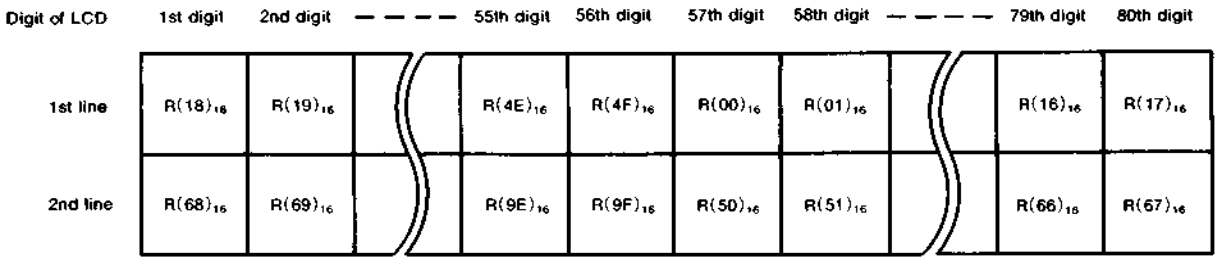


Fig.7 Example of display address

The displayed contents of the first and the second lines look visually as if they are simultaneously shifted to the left. Similarly, if the content of the display start address register is decremented, the displayed contents of the first and the second lines look as if they are shifted simultaneously to the right. When the display start address is situated on the boundary of the display data region of the first line of the RAM, by incrementing or decrementing the display start address the result becomes as shown in table. 6.

Table 6. Change of display start address

Display Start Address		
Before inc/dec	After inc	After dec
$(00)_{16}$	$(01)_{16}$	$(4F)_{16}$
$(4F)_{16}$	$(00)_{16}$	$(4E)_{16}$

Case of 4-line LCD (for 160 words of DD RAM and 96 words of CG RAM) ; Fig. 8.

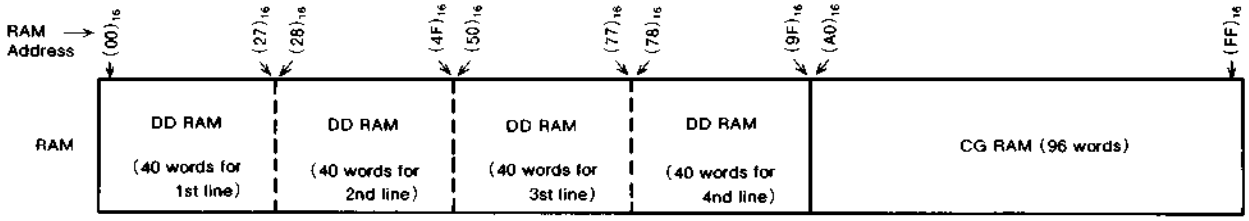


Fig.8 DD/CG RAM

When the content of the display address register is $(17)_{16}$, LCD will be as Fig. 9:

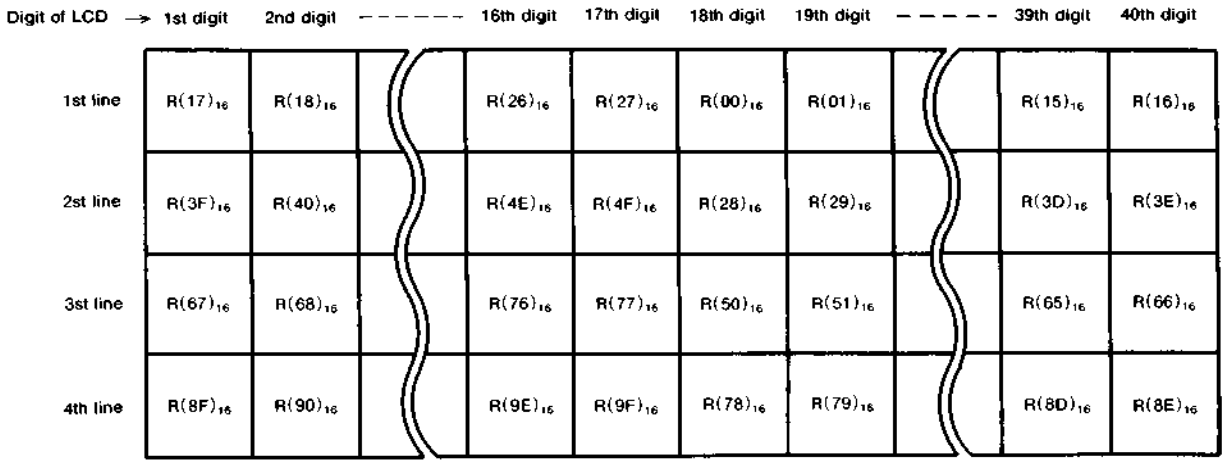


Fig.9 Example of display address

When the content of the display start address register is incremented, the result is $(18)_{16}$, and the LCD will be given by Fig. 10

Digit of LCD →	1st digit	2nd digit	— — —	15th digit	16th digit	17th digit	18th digit	— — —	39th digit	40th digit
1st line	$R(18)_{16}$	$R(19)_{16}$		$R(26)_{16}$	$R(27)_{16}$	$R(00)_{16}$	$R(01)_{16}$		$R(16)_{16}$	$R(17)_{16}$
2st line	$R(40)_{16}$	$R(41)_{16}$		$R(4E)_{16}$	$R(4F)_{16}$	$R(28)_{16}$	$R(29)_{16}$		$R(3E)_{16}$	$R(3F)_{16}$
3st line	$R(68)_{16}$	$R(69)_{16}$		$R(76)_{16}$	$R(77)_{16}$	$R(50)_{16}$	$R(51)_{16}$		$R(66)_{16}$	$R(67)_{16}$
4th line	$R(90)_{16}$	$R(91)_{16}$		$R(9E)_{16}$	$R(9F)_{16}$	$R(78)_{16}$	$R(79)_{16}$		$R(8E)_{16}$	$R(8F)_{16}$

Fig.10 Example of display address

The displayed content of the first, second, third and fourth lines look visually as if they are shifted sumultaneously to the left. Similarly, if the content of the display start address register is decremented, the displayed contents of the first, second, third and fourth lines look as if they are shifted simultaneously to the right. When the display start address is situated on the boundary of the display data region of the first line of the RAM, if the display start address is incremented or decremented, the result will be given by table 7

Table 7. Change of display start address

Display Start Address		
Before inc/dec	After inc	After dec
$(00)_{16}$	$(01)_{16}$	$(27)_{16}$
$(27)_{16}$	$(00)_{16}$	$(26)_{16}$

7 DISPLAY ADDRESS REGISTER

Thig is the register for designating the address of a displayed data of the RAM to be displayed by the liquid crystal.

To read all of the displayed data of the RAM during the times for the respective common signals, convert them to a character pattrern, and transfer them to the column driver; the content of the display address register is continuously and successively changed from the display start address, and the RAM address is scanned and designated.

8 ADDRESS DATA CONTROL

This is to execute display processig, instruction processing, and more for the address and data of the RAM and the ROM by controlling the cursor address register, display start address register, display address register, and so forth.

9 DISPLAY DATA/CHARACTER GENERATOR RAM (DD/CG RAM)

This is the RAM for storing the data and the character fonts for the character generator to be displayed by the liquid crystal.There are altogether 256 words, each word consisting of 9 bits. The 256 word RAM can be divided into a region to be used for display data (DD RAM) and a region to be used by the character generator (CG RAM). The division of the RAM into the DD RAM and the CG RAM is carried out by the instruction SF, and there are 4 kinds of divisions (table 8):

Table 8. Instruction SF and RAM word number

Instruction SF		RAM Word Number(9bits for a word)	
RAM		DD RAM	CG RAM
RA_1	RA_0		
0	0	256 words	0 words
0	1	224 words	32 words
1	0	192 words	64 words
1	1	160 words	96 words

9-1 Display Data RAM (DD RAM)

When 9 bits of a word in the RAM are used as a display data, 8 bits are used for display character code and the remaining 1 bit is used for underline display.

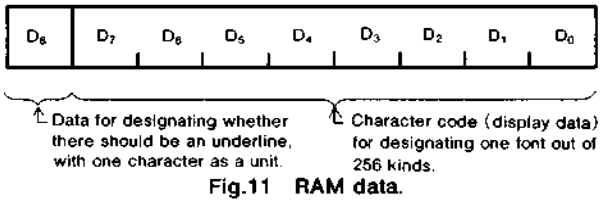


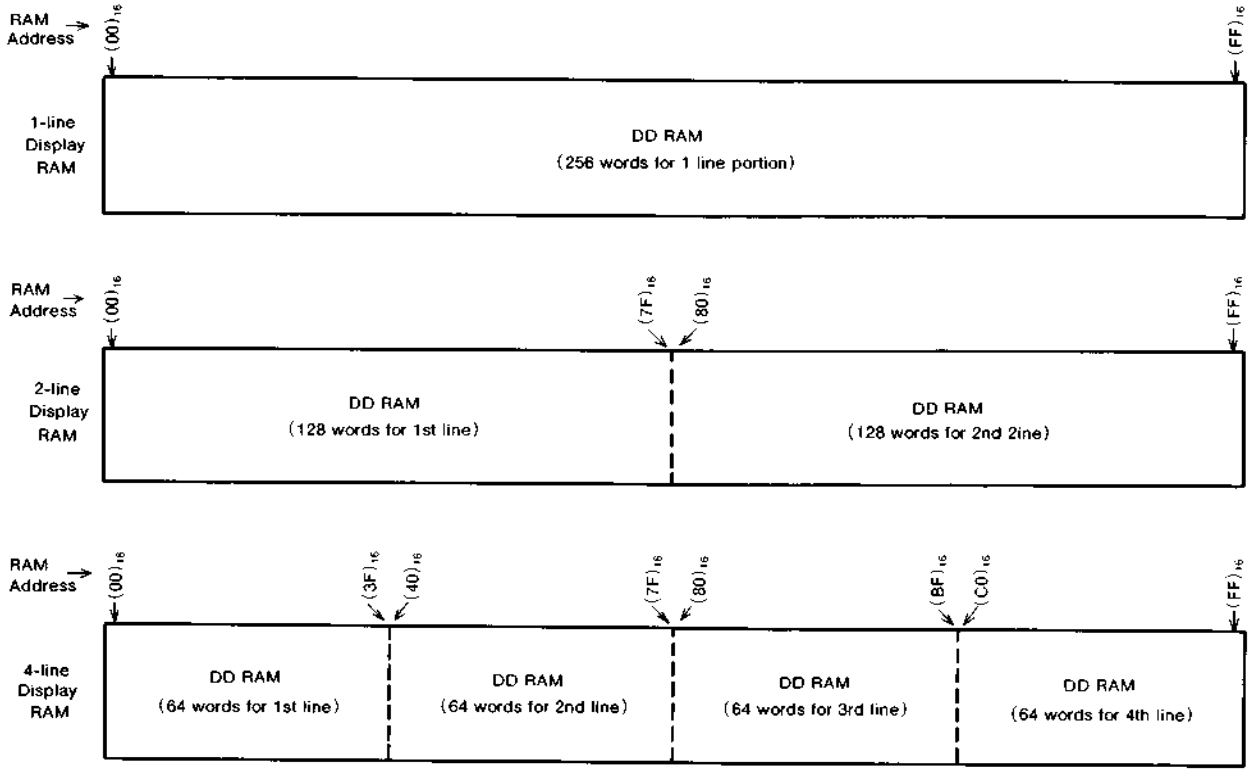
Fig.11 RAM data.

The DD RAM is given the composition of table 9 by the duty which designates one of 1-line display, 2-line display, and 4-line display, and the font setting instruction SF.
Next, the addresses for each display line of the DD RAM and the addresses of the CG RAM will be shown in the diagram (9-1-1 ~ 9-1-4) for each of these 4 kinds of RAM composition.

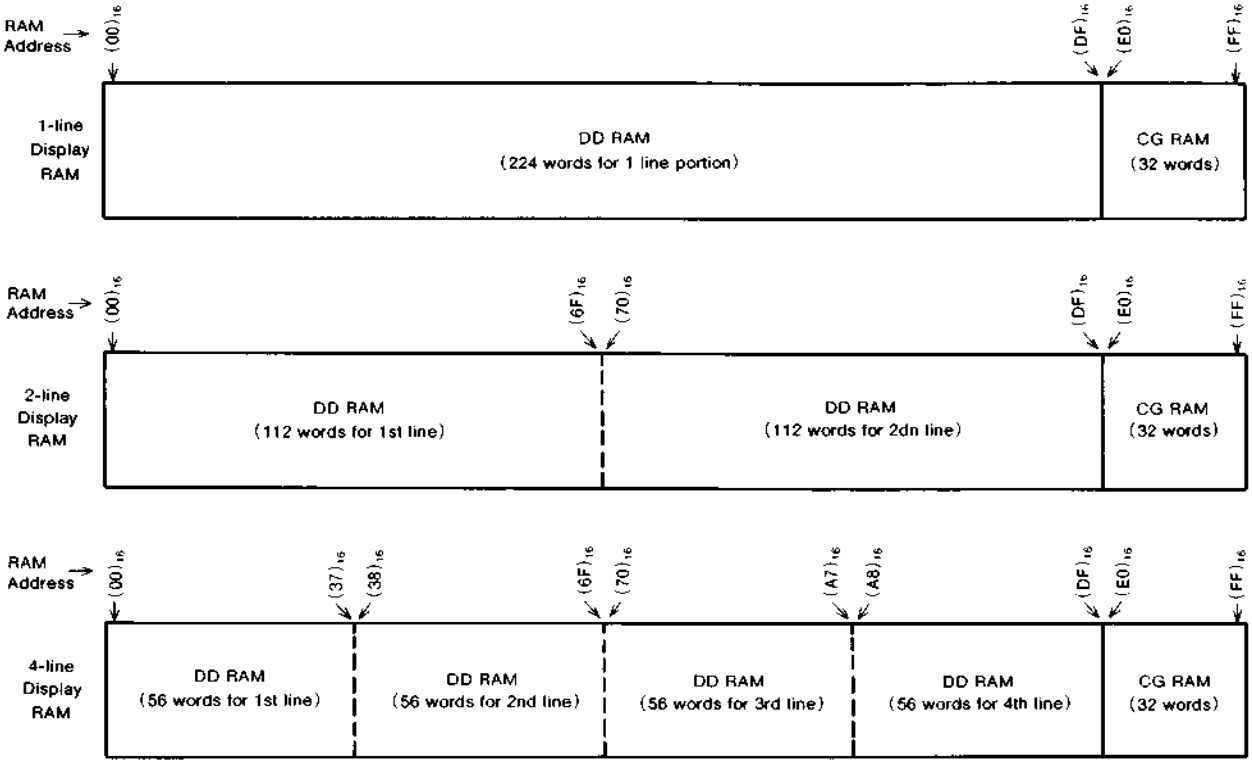
Table 9. Instruction SF and RAM composition

Instruction SF			1-line Display	2-line Display	4-line Display
Font		1	Duty 1/8	Duty 1/16	Duty 1/32
8/12		0	Duty 1/12	Duty 1/24	Duty 1/48
	DT_1		0	0	1
RA_1	D_{T_0} / R_{A_0}		0	1	0
0	0		1 line×256 words	2 line×128 words	4 line× 64 words
0	1		1 line×224 words	2 line×112 words	4 line× 56 words
1	0		1 line×192 words	2 line× 96 words	4 line× 48 words
1	1		1 line×160 words	2 line× 80 words	4 line× 40 words

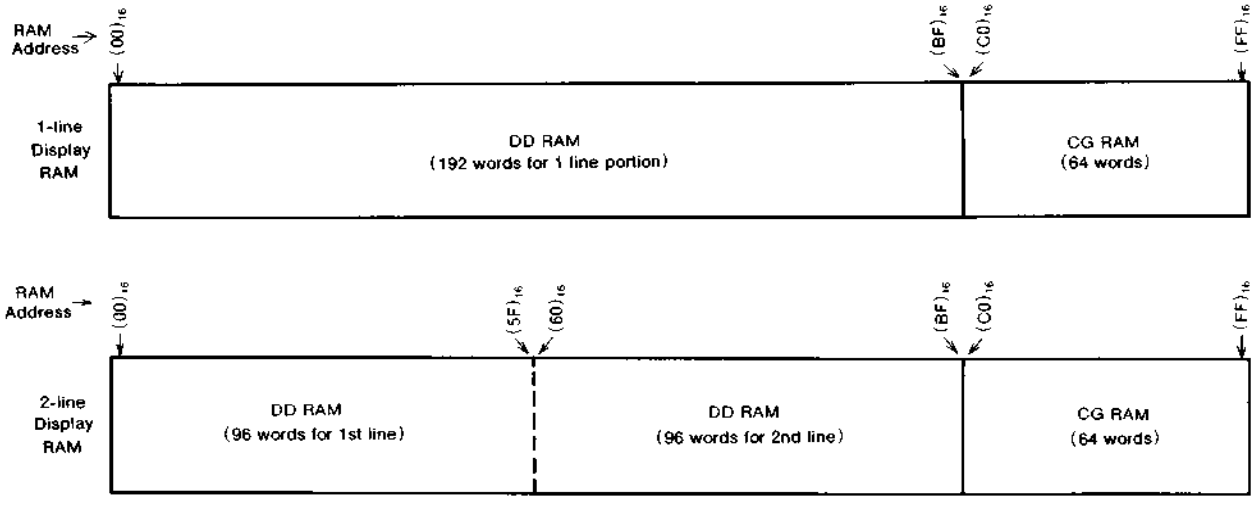
9-1-1 Case of 256 words for DD RAM and 0 word for CG RAM

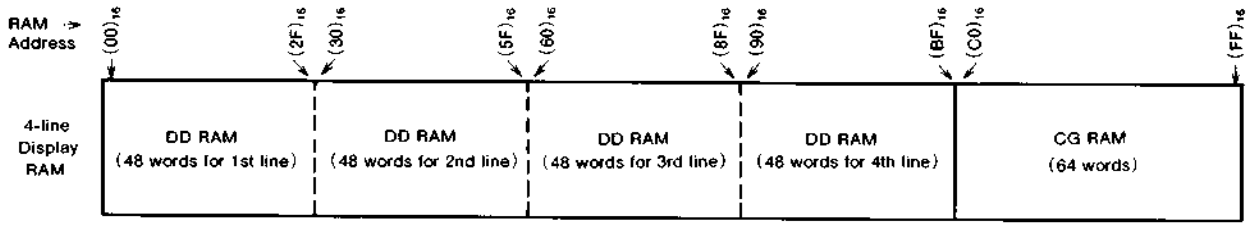


9-1-2 Case of 224 words for DD RAM and 32 words for CG RAM

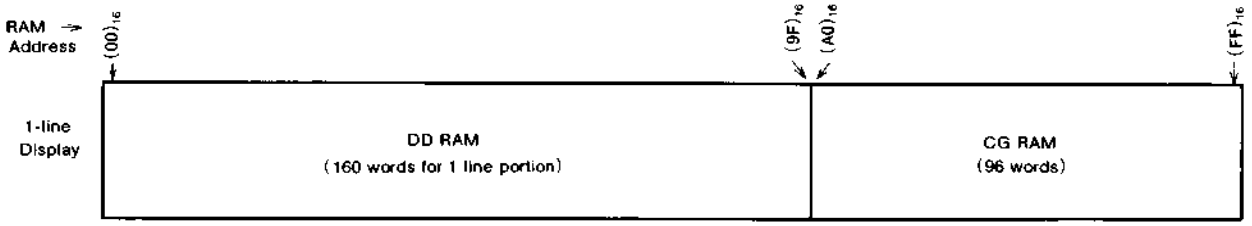


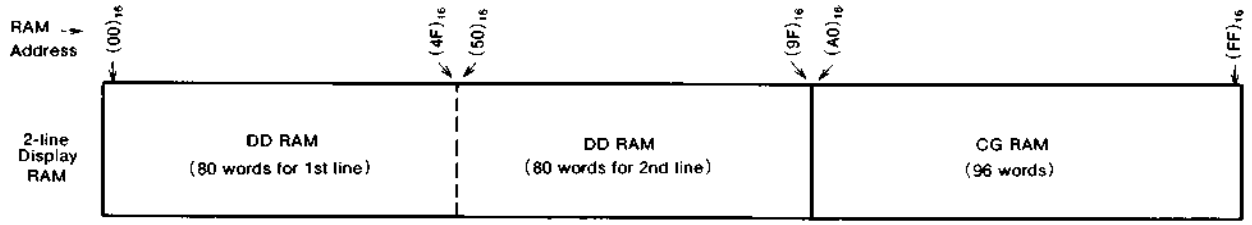
9-1-3 Case of 192 words for DD RAM and 64 words for CG RAM

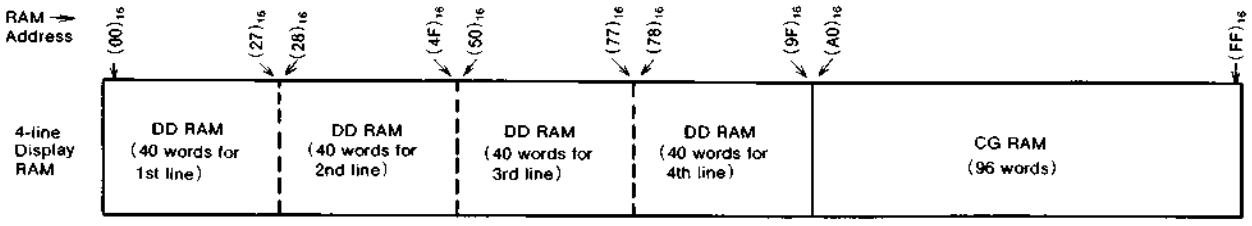




9-1-4 Case of 160 words for DD RAM and 96 words for CG RAM





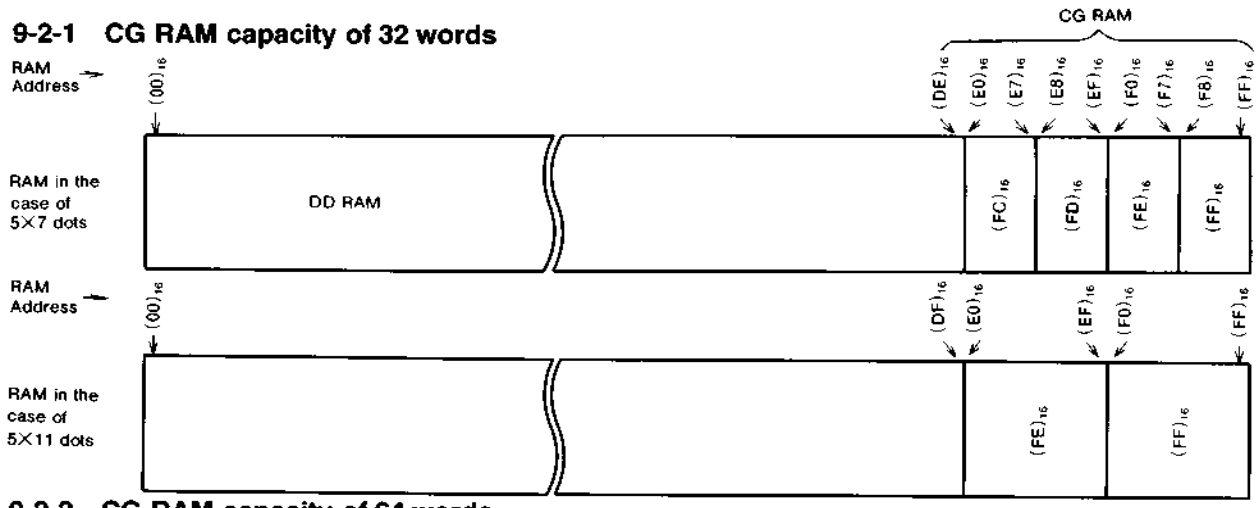


9-2 Character Generator RAM (CG RAM)

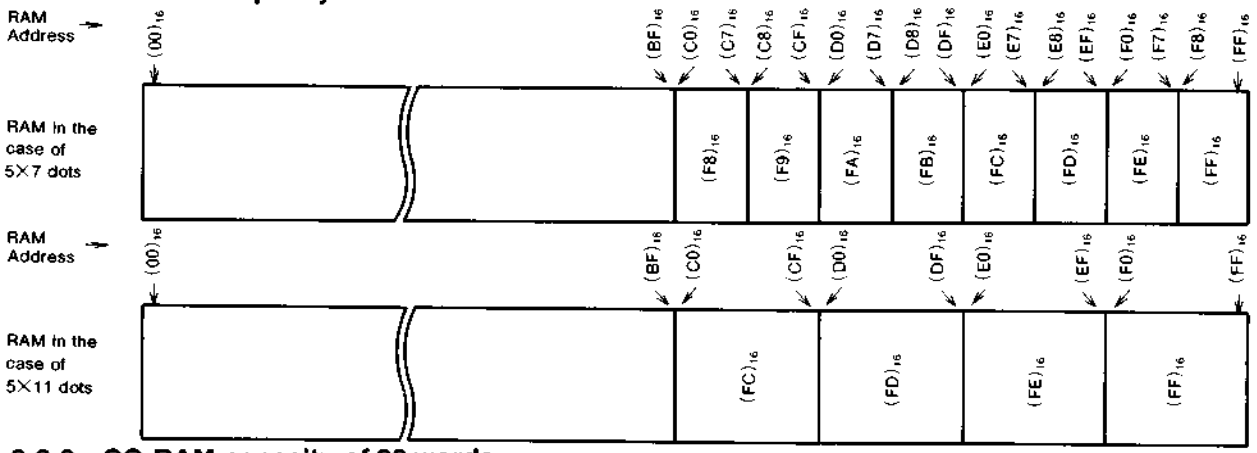
In the CG RAM the user can write an arbitrary font of 5×7 dots or 5×11 dots. A maximum of 12 character fonts in the case of 5×7 dots, and a maximum of 6 fonts in the case of 5×11 dots, can be written in the CG RAM.

The address of the CG RAM which is written a character font and the character code of the character font are made to correspond in a 1 to 1 fashion as shown in the diagram (9-2-1~9-2-4).

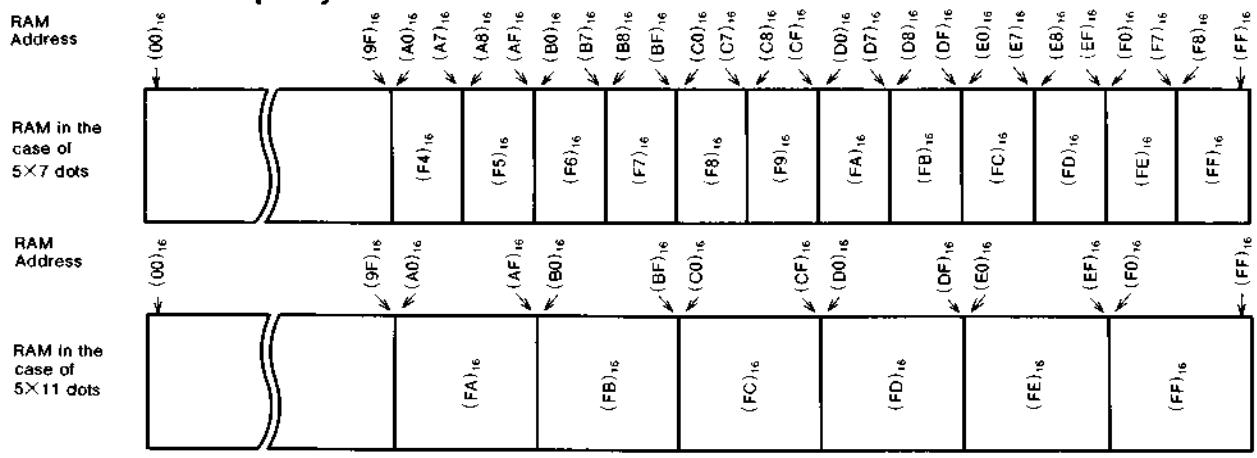
9-2-1 CG RAM capacity of 32 words



9-2-2 CG RAM capacity of 64 words

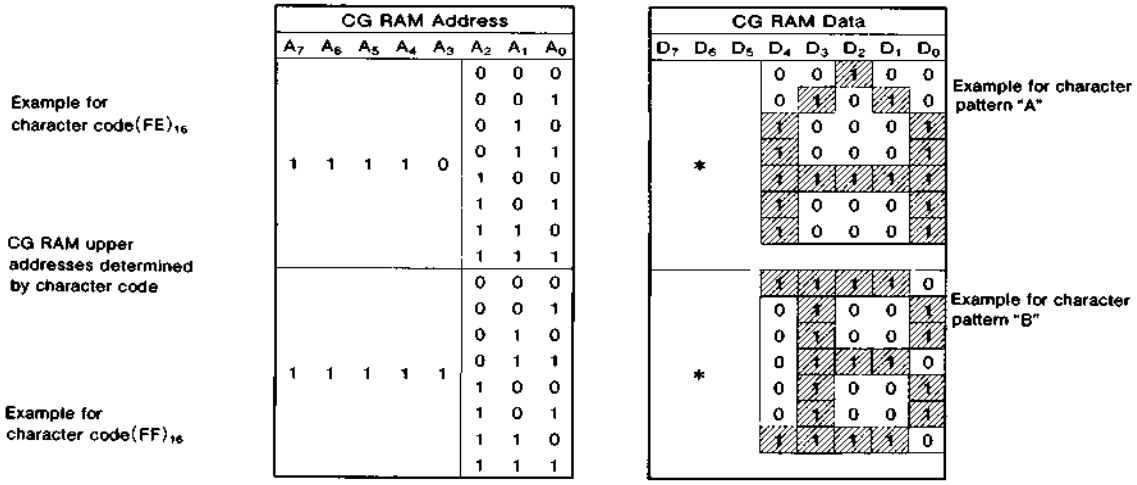


9-2-3 CG RAM capacity of 96 words



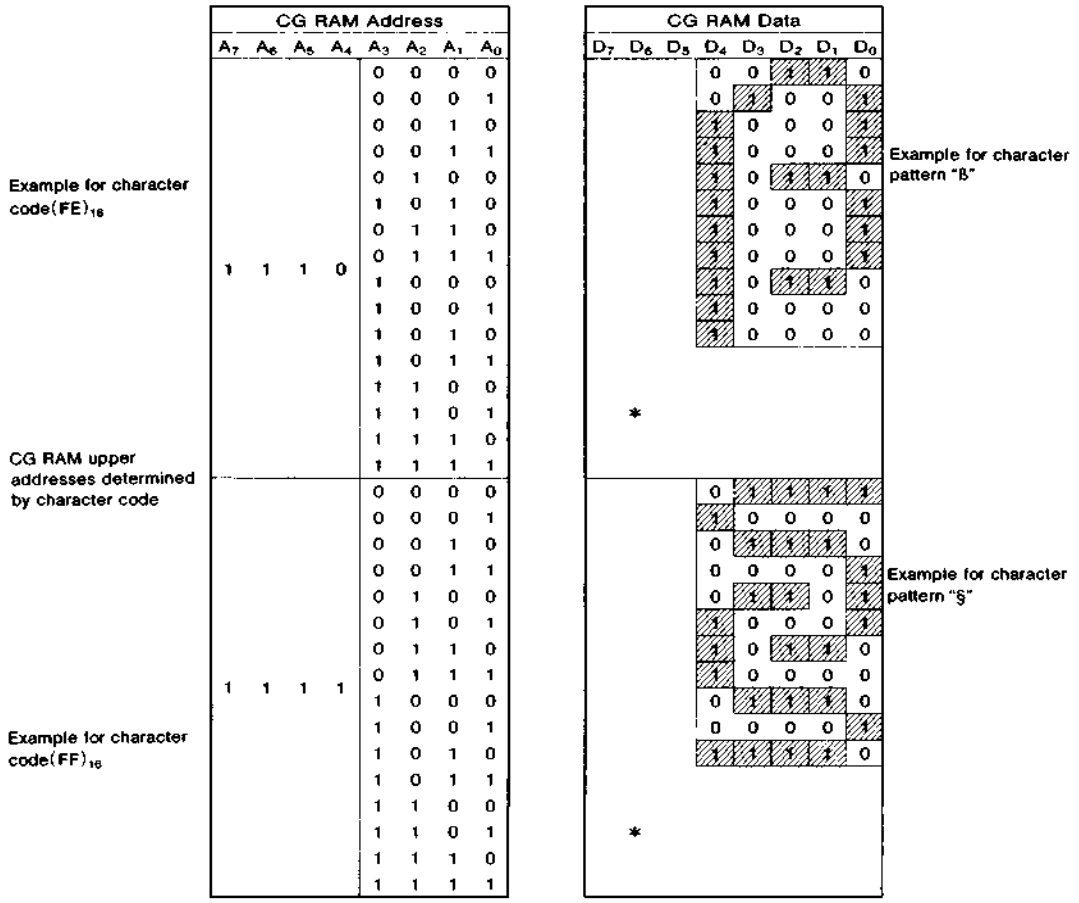
Next, an example of constructing a character font from an address and a data of the CG RAM for each character code will be described.

CHARACTER FONT OF 5×7 DOTS



The portion of the CG RAM marked with an " * ", namely, data D_7 D_6 D_5 and data D_7~D_0 in which the address for A_2 A_1 A_0 is $(111)_2$, will not be used as a pattern for a character font. However, it can be used for general data RAM.

CHARACTER FONT OF 5×11 DOTS



The portion marked with an "*", namely data D_7 D_6 D_5 and data $D_7 \sim D_0$ in which the address A_3 A_2 A_1 A_0 is in the range from $(1011)_2$ to $(1111)_2$, will not be used as a pattern for character font. However, it can be used for general data RAM.

To write and read character pattern data for character font from the CG RAM, the address is set in the cursor address register with the instruction WC, analogous to the case of writing and reading a data from the DD RAM. Writing and reading are executed with the instructions WD and RD using 8 bits per word. Of the 8 bits in a word 5 bits are made to correspond to 5 dots in a line as character pattern data for the character font. The bits of the CG RAM data, $(1)_2$ corresponds to the display selection by the LCD dots while $(0)_2$ corresponds to the nondisplay selection. In the case of a character font of 5×7 dots, the bit is written 7 words for 7 line portions, and in the case of a character font of 5×11 dots, it is necessary to write the bit for 11 words for 11 line portions.

10 CHARACTER GENERATOR ROM (CG ROM)

This is the ROM for generating a fixed character font from the character codes with display data 8 bits. The content of CG ROM (character fonts) is programable by mask ROM. 256 kinds of character fonts of 5×7 dots or 5×11 dots as dot-matrix characters can be stored.

These 256 kinds of font represent the sum of the number of the character fonts generated in the CG RAM and the number of the character fonts generated in the CG ROM. Accordingly, the number of fonts that can be generated in the CG RAM and the CG ROM varies depending upon the division ratio of the DD RAM and the CG RAM regions and also upon whether using 5×7 dots or 5×11 dots. Those combinations are shown in table 10.

The relationship between the range of the character codes corresponding to the CG RAM and the range of the character codes corresponding to the CG ROM will now be shown.

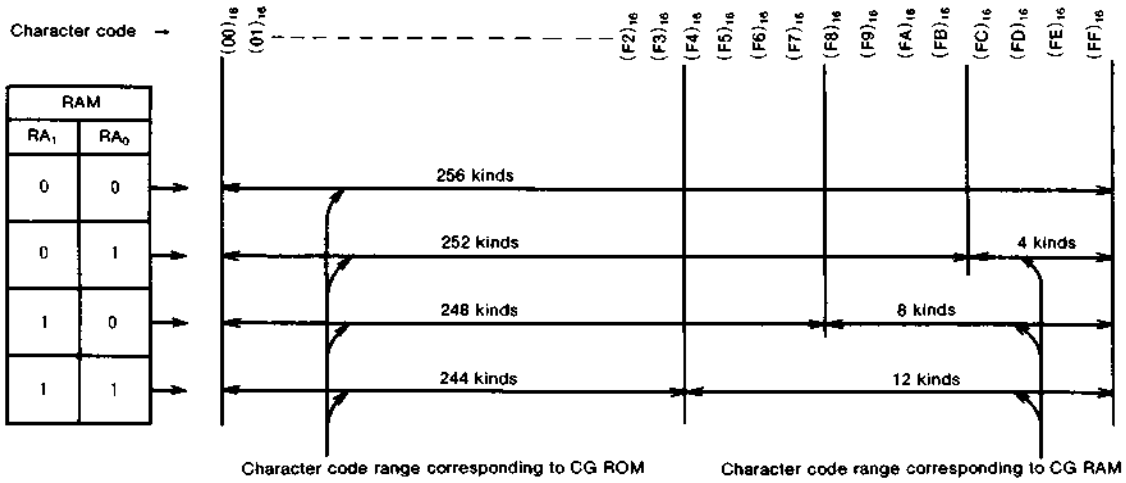
Of the character codes, the space code is a special code which is used for the clear display. All of the dot bits in the character font 5×11 dots for the CG ROM content that correspond to the space code are $(0)_2$, indicating nondisplay. And the space code must be set up between from character code $(00)_{16}$ to $(F3)_{16}$.

When the DD RAM content is cleared by the autoclear or the instruction CH, all of the display data go to the space code.

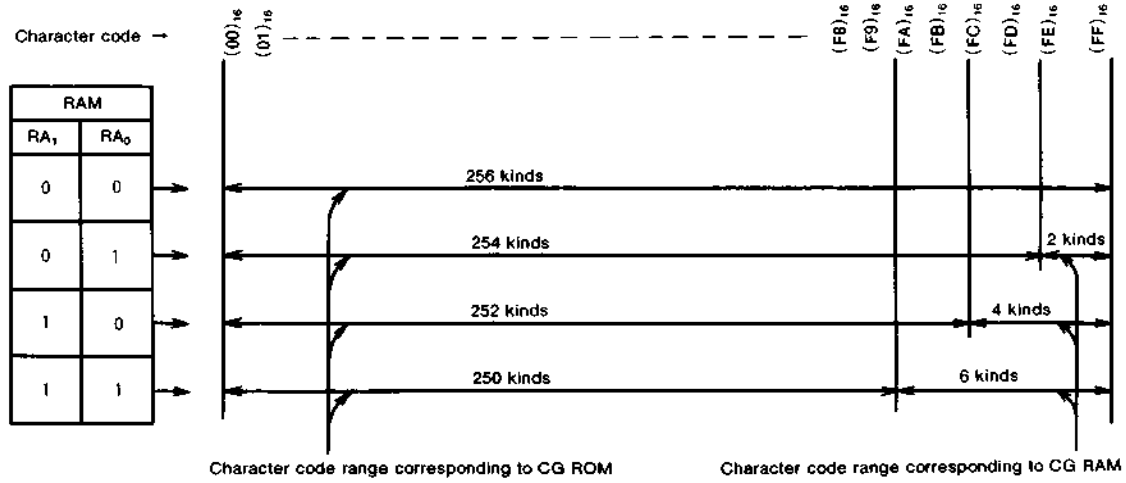
Table 10. Display font number

Dot Matrix Composition	Instruction SF			CG RAM		CG ROM
	Font 8/12	RA_1	RA_0	Memory Capacity(words)	Font Number(kinds)	Font Number(kinds)
5×7 dots	1	0	0	0	0	256
		0	1	32	4	252
		1	0	64	8	248
		1	1	96	12	244
5×11 dots	0	0	0	0	0	256
		0	1	32	2	254
		1	0	64	4	252
		1	1	96	6	250

CASE OF CHARACTER FONT OF 5×7 DOTS



CASE OF CHARACTER FONT OF 5×11 DOTS



11 SERIES/PARALLEL CONVERSION CIRCUIT

This is the circuit for sending a parallel font pattern data from the CG ROM or the CG RAM to the column driver by converting it to a serial data.

12 DISPLAY, CURSOR, AND BLINK CONTROLS

They control the ON/OFF of the LCD, cursor display, blinking display, and so forth. Various display modes given below can be set using the instruction SD.

- ON/OFF of the entire display
- ON/OFF of the cursor
- ON/OFF of the underline display
- Blinking of the cursor display
- Blinking of a character at the cursor position

By the use of the instruction SB, 1 blinking frequency can be selected out of the following 4 kinds.

0.5Hz 1Hz 2Hz 4Hz

(for an oscillation frequency of about 2.5MHz)

The cursor will be displayed on the lowest line of the font matrix as indicated below.

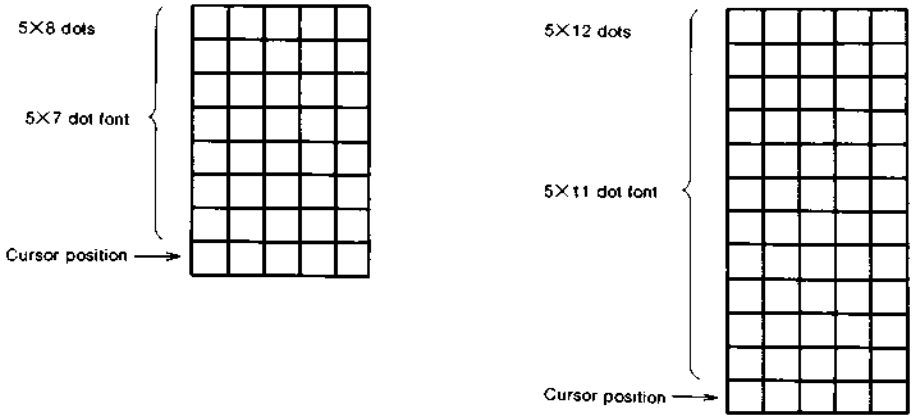
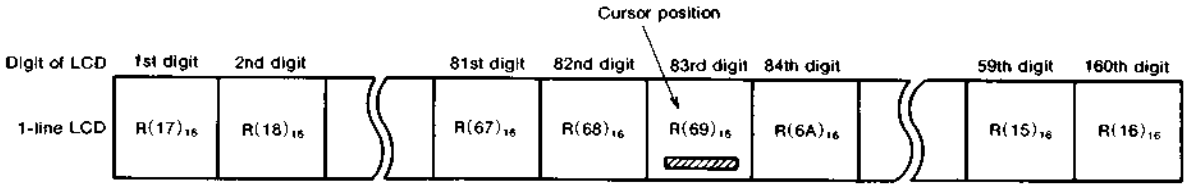


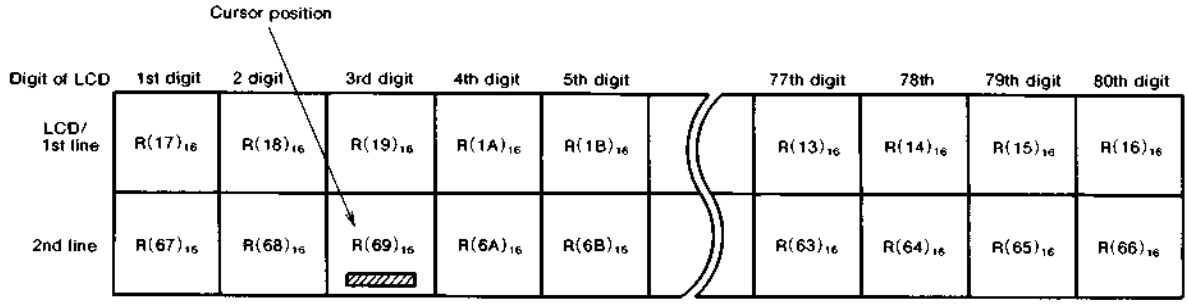
Fig.12. Position of character font and cursor.

The cursor display and the blinking display will be displayed at the digit position of the RAM display data which is designated by the cursor address register.
When the content of the cursor register is $(69)_{16}$ and the content of the display start register is $(17)_{16}$, the display positions of the cursor and the blinking are as shown below.

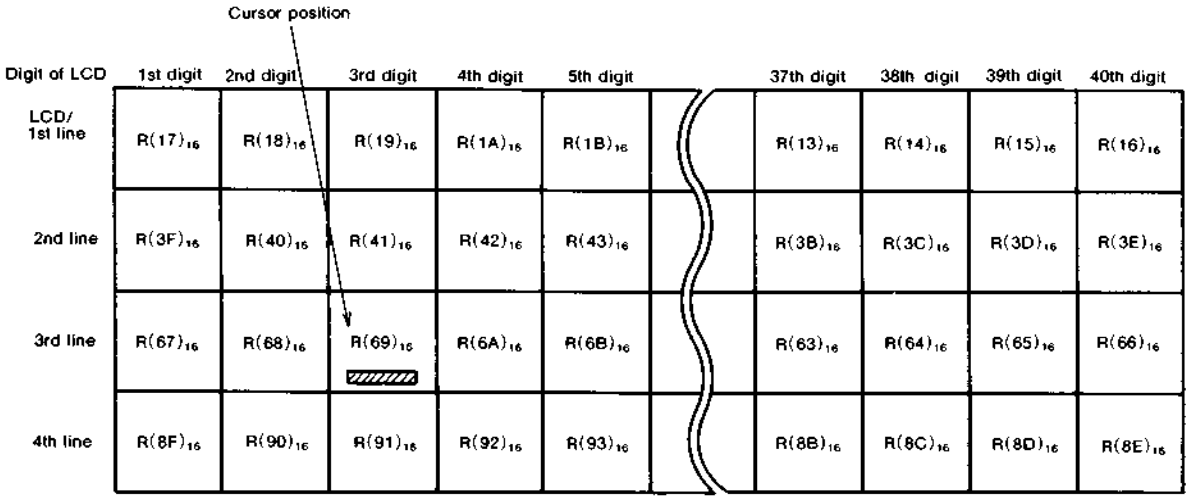
• 1 line of LCD (for 160 words of DD RAM and 96 words of CG RAM)



• 2 lines of LCD (same conditions as above)



• 4 lines of LCD (same conditions as above)



13 COMMON SIGNAL OUTPUT CIRCUIT

There are 32 lines of common signal drive output which directly drive the common side of the LCD.

Therefore, it is possible to directly drive the common signals with the display duties ranging from 1/8 to 1/32. Further, by connecting a common driver for expansion, M50521FP or M50524FP in the outside, it becomes possible to drive common signals up to a duty of 1/48. The output signal CMD is the common signal to be sent to the external common driver.

The unused common drive outputs become nondisplay selection signals. For example, when duty is 1/16, the common outputs COM1~COM16 output common scanning signals, but COM17~COM32 always output nondisplay selection signals.

The instruction SF can set the character font and the duty, and the number of display lines and the effective common signal are given as shown in the Table. 11.

14 COLUMN SIGNAL OUTPUT CIRCUIT

The display data which is converted to a character font pattern is sent to a 40-bit shift register as serial pattern data, and is then latched.

The latched output controls the driver to output 40 lines of column signals that directly drive the liquid crystal display.

With the 40 lines of column signals it is possible to direcrly drive an 8 digit portion LCD for either a 1-line, 2-line, or 4-line display.

The number of displayed digits can be expanded by transferring the character font pattern data to an external column driver (M50521FP or M50524FP) from the column data output signal CLD . Depending upon the number of bits of the column driver (which is connected externally) it is possible to expand the character display from an arbitrary digit number to a maximum digit number.

15 TIMING SIGNAL GENERATING CIRCUIT

The ocsillation circuit generates various kinds of internal timing signals to be used for display processing, instruction processing, and so forth.

In addition, the circuit generates timing signals for controlling the external LCD driver in order to expand the digit number of the LCD.

The processig of an instruction is executed totally independently of the LCD processing so that there will be no change in the processing time of LCD which is determined by the duty employed.

Further, the period for liquid crystal to display all of the display patterns once, (the period of the common signal) depends only on the oscillation frequency. The period of the cursor/character display blinking, also depends only on the oscillation frequency.

Table 11. Effective common signal output

Character Font	Instruction SF			Duty	Number of Display Lines	Effective Common Signal Output
	Font 8/12	DT_1	DT_0			
5×8 dots	1	0	0	1/8	1	COM1~COM8
		0	1	1/16	2	COM1~COM16
		1	0	1/32	4	COM1~COM32
5×12 dots	0	0	0	1/12	1	COM1~COM12
		0	1	1/24	2	COM1~COM24
		1	0	1/48	4	*COM1~COM32

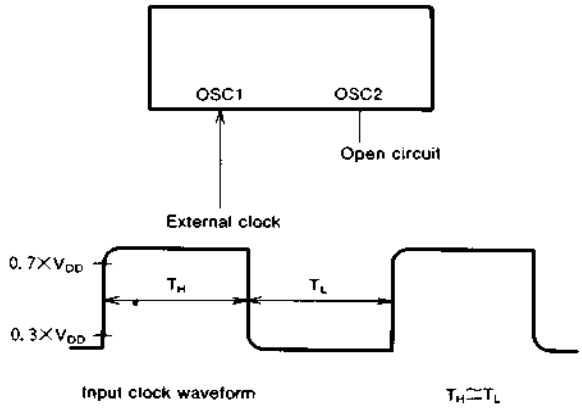
※ By the use of an external common driver for expansion COM33~COM48 can be generated.

16 OSCILLATOR

To generate an internal clock, it is possible to let the built-in oscillator induce self-oscillation by connecting a simple external part. It is also possible to input a clock to the oscillator from the outside.

16-1 Using an external clock

Input the external clock to the oscillator input terminal OSC1, and leave the oscillator output terminal OSC2 disconnected.



$T_H + T_L = 330 \sim 500ns$

16-2 Using built-in oscillator

(16-2-1) The built-in oscillator can be set to oscillate by connecting an external resistor for oscillation between the terminals OSC1 and OSC2.
Try to minimize the wire length for connecting the resistor in order to reduce the external capacitance to be connected to the terminals OSC1 and OSC2.

(16-2-2) It is possible to set the built-in oscillator into oscillation by connecting a ceramic vibrator between the terminals OSC1 and OSC2 as in the figure.

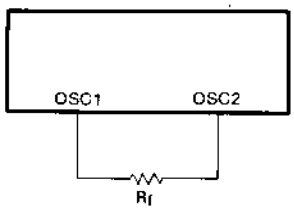
Next, the oscillation frequency of the oscillator and the period of the common signal are related by the following equations:

$T_{COM} = \frac{36864}{f_{OSC}}$ Here, T_{COM} : Period of common signal (s)

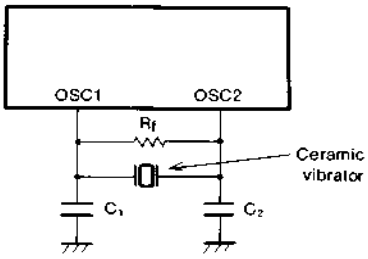
f_{COM} : Inverse of T_{COM} (Hz)

$f_{COM} = \frac{f_{OSC}}{36864}$ f_{OSC} : Oscillation frequency (Hz)

For example, to obtain 70Hz for f_{COM}, f_{OSC} must be about 2.58MHz.



When the oscillation frequency is about 2.5 MHz,
R_f = 3.9KΩ±2%
(Reference value)



Refrence vlaue
(f_{OSC} = 2.5MHz)
R_f = 1MΩ ± 10%
C_1 = 100 ~ 220pF
C_2 = 100 ~ 220pF
Ceramic vibrator: CSA 2.500MK
(Made by Murata Corp.)

17 AUTOCLEAR

After closing the power supply, a built-in autoclear circuit is actuated to linitialize RAM and various kinds of mode flags. While the autoclear is in operation, the busy flag is set to $(1)_2$.

- All of the 8bit display data of the RAM display data region are set to the space code, and all of the underline bits are set to $(0)_2$(nondisplaying)
- The display start address and the cursor address are set to $(00)_{16}$.
- The mode flags to be used for the instructions are initialized as Fig. 13

To operate the autoclear circuit without failure please be sure to let the power supply V_{DD} satisfy the conditions indicated in Fig. 14. When these conditions are not fulfilled, it is necessary to meet the conditions by the execution of instructions.

Function mode (Instruction SF)

I/OC	FONT	DUTY		RAM	
8/4	8/12	DT_1	DT_0	RA_1	RA_0
1	0	0	0	0	0

Entry mode (Instruction SE)

CSR	CSR CONDITION		DSP	DSP CONDITION	
D/I	W	R	D/I	W	R
0	0	0	0	0	0

Display mode (Instruction SD)

DSP	CSR	UND	CSR	CHR
ON/OFF	ON/OFF	ON/OFF	BLINK	BLINK
0	0	0	1	1

Underline mode (Instruction SU)

USR	UND
ON/OFF	S/R
0	1

Blinking mode (Instruction SB)

BLINK FREQ	
B_1	B_0
0	1

Fig.13 Mode of initialization

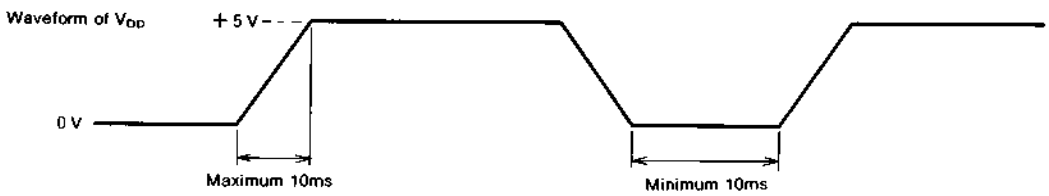
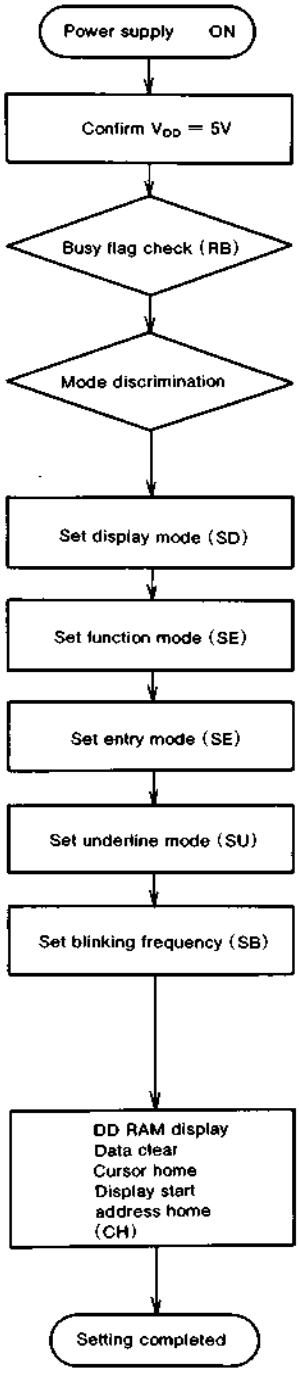


Fig.14 V_{DD} waveform

An example of a software initialization method is shown below.

Example of Set Data(for 8-bit mode)										
I/O C1	I/O C2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	1	Flag check							
0	0	0	0	0	1	0	0	0	1	1
0	0	0	1	1	1	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1	0	1
0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	0	1



Hereafter, carry out busy flag check whenever an instruction is to be executed. If a check is not given, it is necessary to wait until the execution of the preceding instruction is completed.

Refer to the mode discrimination method at the time of turning on the power supply described in "Read instrucions for busy flag and function flags (RB)"

Display OFF, cursor and character blinking ON

Length of the interface data is 8 bits, 256 characters 5 × 12 dot font are displayed in 1 line.

No change in the cursor address as well as in the display start address at the time of access to the RAM.

No change in underline bit

Blinking frequency

$$fB = \frac{f_{OSC}(\text{Oscillation frequency})}{4718592} \times 2$$

RAM data clear
Cursor home
Display start address home

Note : Letters within ( ) are abbreviation symbols for an instruction.

INSTRUCTION CODE

Instruction Code

I/OC 1	I/OC 2	R/W	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	D B Input to LSI / Output from LSI	Instruction Function	Execution Time for f_{OSC}=2.58MHZ	Abbreviation for instruction
1	1	1	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0	Output	Read cursor address of RAM	20μs	RC
		0	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0	Input	Write cursor address of RAM	20μs	WC
	0	1	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0	Output	Read display start address	20μs	RS
		0	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0	Input	Write display start address	20μs	WS
0	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Output	Read RAM data	20μs	RD
		0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Input	Write RAM data	20μs	WD
	0	1	BUSY	4μ2	I/O 8/4	FONT 8/12	BUSY	4μ2	RAM RA_1	RAM RA_0	Output	Read busy flag and other flags	0	RB
		0	1	1	I/O 8/4	FONT 8/12	DUTY DT_1	DUTY DT_0	RAM RA_1	RAM RA_0	Input	Set function mode	20μs	SF
				1	CSR D/I	CSR CONDITION W	CSR CONDITION R	DSP D/I	DSP CONDITION W	DSP CONDITION R	Input	Set entry mode	20μs	SE
					1	DSP ON/OFF	CSR ON/OFF	UND ON/OFF	CSR BLINK	CHR BLINK	Input	Set display mode	20μs	SD
						1	CSR	CSR D/I	DSP	DSP D/I	Input	Shift cursor/display-start address	20μs	MA
							1	1	USR ON/OFF	UND S/R	Input	Set underline mode	20μs	SU
								0	UND S/R	CSR I	Input	Write RAM underline bit	20μs	WU
								1	BLINK FREQ B_1	BLINK FREQ B_0	Input	Set blinking frequency	20μs	SB
					0				1	1	Input	Cursor home and display start address home	20μs	MH
										1	Input	Clear cursor of DD RAM display data home, and display start address home	1.25ms	CH
											Input	No operation	20μs	NOP

DESCRIPTION OF INSTRUCTIONS

1 THE READ CURSOR ADDRESS INSTRUCTION (RC)

READ DD/CG RAM CURSOR ADDRESS

This instruction reads the cursor address which designates the RAM address. It reads the 8-bit ($AD_7 \sim AD_0$) cursor address register to the data bus ($DB_7 \sim DB_0$).

The most significant bit (MSB) of the address data is AD_7 and the least significant bit (LSB) is AD_0.

The cursor address can be used for address designation of writing and reading for both DD RAM and CG RAM.

This instruction enable the value of the current cursor address to be determined.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	1	1	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0
Input to the LSI			Output from the LSI							

2 THE WRITE CURSOR ADDRESS INSTRUCTION (WC)

WRITE DD/CG RAM CURSOR ADDRESS

This instruction writes a cursor address which designates the RAM address. It writes the 8-bit data ($AD_7 \sim AD_0$) on the data bus ($DB_7 \sim DB_0$) to the cursor address register.

The most significant bit (MSB) of the address data is AD_7 and the least significant bit (LSB) is AD_0.

The cursor address can be used in address designation for writing and reading of both DD RAM and CG RAM.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	1	0	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0
Input to the LSI										

3 THE READ DISPLAY START ADDRESS INSTRUCTION (RS)

READ DISPLAY START ADDRESS

This instruction reads the display start addres.

It reads the 8-bit ($AD_7 \sim AD_0$) display start address register to the data bus ($DB_7 \sim DB_0$).

The most significant bit (MSB) of the address data is AD_7 and the least significant bit (LSB) is AD_0.

The display start address conforms to the RAM address that corresponds to the leftmost digit of the LCD.

This instruction enable the current value of the display start address to be determined.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	1	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0
Input to the LSI			Output from the LSI							

4 THE WRITE DISPLAY START ADDRESS INSTRUCTION (WS)

WRITE DISPLAY START ADDRESS

This instruction writes the display start address.

It writes the 8-bit data ($AD_7 \sim AD_0$) on the data bus ($DB_7 \sim DB_0$) to the display start address register.

The most significant bit (MSB) of the address data is AD_7 and the least significant bit (LSB) is AD_0.

The display start address corresponds to the RAM address that corresponds to the leftmost digit of the LCD. In the 2-line and 4-line display, the display start address agrees with the RAM address that corresponds to the leftmost digit fo the first line.

The region of the display start address for various DD RAM regions and numbers of display lines are shown Table.12. Choose the display start address within the range indicated.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	0	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0
Input to the LSI										

Table 12. Range of display start address

Instruction SF		1-line Display	2-line Display	4-line Display
	DT_1	0	0	1
RA_1	DT_0 / RA_0	0	1	0
0	0	0~255	0~127	0~63
0	1	0~223	0~111	0~55
1	0	0~191	0~ 95	0~47
1	1	0~159	0~ 79	0~39

5 THE READ RAM DATA INSTRUCTION

READ DD/CG RAM DATA

This instruction reads RAM data.

It reads the 8-bit data (D_7~D_0) of the DD RAM or CG RAM designated by the cursor address to the data bus (DB_7~DB_0).

The most significant bit (MSB) of the data is D_7 and the least significant bit (LSB) is D_0.

After the RAM data is read, the cursor address or the display start address is incremented (+1) or decremented (−1) according to the entry mode conditions.

(See the entry mode instruction SE.)

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Input to the LSI			Output from the LSI							

6 THE WRITE RAM DATA INSTRUCTION (WD)

WRITE DD/CG RAM DATA

This instruction writes data to the RAM.

It writes the 8-bit data (D_7~D_0) of the data bus (DB_7~DB_0) to the DD RAM address or the CG RAM address which is designated by the cursor address.

The most significant bit (MSB) of the data is D_7 and the least significant bit (LSB) is D_0.

When the system is set to USR=1, the instruction SU sets the underline bit of the cursor address RAM data to $(1)_2$ when UND S/R=1, and resets to $(0)_2$ when UND S/R=0. (See the underline mode set instruction SU.)

After writing data to the RAM, the cursor address or the display start address is incremented (+1) or decremented (−1) according to the entry mode conditions. (See the entry mode set instruction SE.)

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Input to the LSI										

7 THE READ BUSY FLAG AND FUNCTION FLAGS INSTRUCTION (RB)

READ BUSY FLAG & FUNCTION FLAGS

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	1	BUSY	4μ2	I/O 8/4	FONT 8/12	BUSY	4μ2	RAM RA_1	RAM RA_0

Input to the LSI / Output from the LSI

The busy flag and the 4 function mode flags are read to the data bus(DB_7~DB_0) by this instruction. In DB_7 and DB_3 the status of the busy flags (which show whether an instruction other than the instruction RB is in execution) is read.

If BUSY=1, the LSI is executing an instruction.

If BUSY=0, instruction execution is completed.

The busy flags are the flags which show whether the M50530-XXXFP can accept an external instruction. Therefore, when it is desired to issue an external instruction other than the RB to M50530-XXXFP, be sure to read the busy status using instruction RB. If BUSY=1, issue the instruction RB repeatedly until BUSY=0. Issue the next instruction after confirmation that BUSY=0.

In DB_5, DB_4, DB_1, and DB_0, the flag status of the 4 function modes that were set by the function mode set instruction SF and read out.

I/O 8/4 Interface data length flag

FONT 8/12 Font flag

RA_1, RA_0 RAM region flags

In DB_6 and DB_2 (4μ2) the flag statuses indicating the current instruction state of the M50530-XXXFP are output to the interfaces with the 8-bit and 4-bit microcomputers.

When 85/μc is in the "L" state, the result of execution of the instruction RB is as shown in Table. 13.

It is to be noted that when 85/μc is in "H" state, DB_6 and DB_2 always go to "L" state.

Show in Fig. 15, an example of status discrimination by means of the flags is presented.

8 THE SET FUNCTION MODE INSTRUCTION (SF)

SET FUNCTION MODE.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	1	1	I/O 8/4	FONT 8/12	DUTY DT_1	DUTY DT_0	RAM RA_1	RAM RA_0

Input to the LSI

This instruction sets up the interface width, font, duty, and RAM region.

These prerequisites to the internal data processing are set by the instruction code as follows.

The I/O 8/4 determines the width of the data to be transferred through the external interface.

- I/O 8/4 = 1 : The 8 lines of the input/output data bus (DB_7~DB_0) are used for the transfer of 8-bit data. Interfacing with an 8-bit μc is possible.
- I/O 8/4 = 0 : 8-bit data is transferred in 2 portions (the upper 4 bits and the lower 4 bits), by using the high nibble (DB_7~DB_4) of the 8 input/output data bus (DB_7~DB_0).
  Interfacing with a 4-bit μc is possible.

The FONT 8/12 determines the dot matrix composition for one character font.

- FONT 8/12=1 : The font for 1 digit is composed of 5×8 dots. Of these, 5×7 dots are for the character font, and the 5×1 dots in the bottom row are for the cursor.
- FONT 8/12=0 : The font for 1 digit is composed of 5×12 dots. Of these 5×11 dots are for the character font, and the 5×1 dots in the bottom row for the cursor.

The DUTY (DT_1 and DT_0) sets the duty and the line number of the display. The RAM (RA_1 and RA_0) sets the DD region and the CG region.

This is shown in Table. 14.

Table 13. Result of excuted instruction RB.

		Data BUS DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
		BUSY	4μ2	I/O 8/4	FONT 8/12	BUSY	4μ2	RA_1	RA_0	
8-bit mode		BUSY	L	H	8/12	BUSY	"L"	RA_1	RA_0	Result of execution in 8-bit operation mode
4-bit mode	First half data	BUSY	"L"	"L"	8/12					Result of execution in first 4-bit operation mode
	Second half data	BUSY	"H"	RA_1	RA_0					Result of execution in second 4-bit operation mode

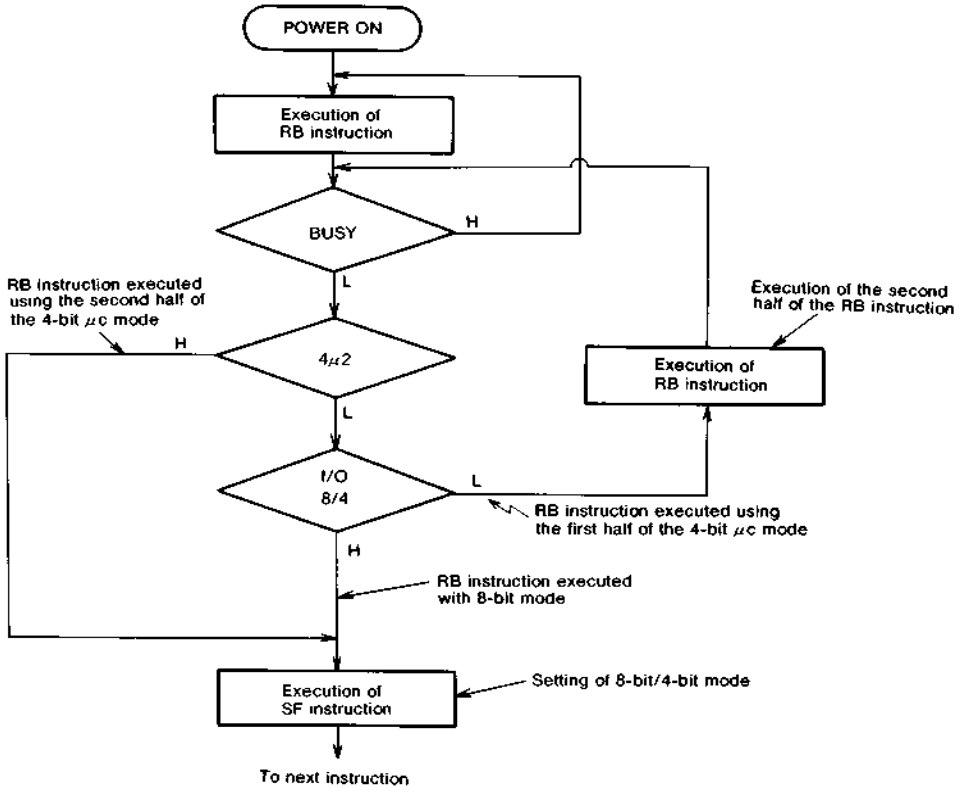


Fig.15 Example of status discrimination

Mode discrimination method at the time of turning on the power supply (when the power on clear is inoperative)

Table 14. Region of RAM

Instruction SF			RAM (9 bits for 1 Word)					
			DD RAM					
			1-line Display	2-line Display	4-line Display	CG RAM		
	FONT	1	Duty 1/8	Duty 1/16	Duty 1/32			
	8/12	0	Duty 1/12	Duty 1/24	Duty 1/48		CG character number	
	DT_1		0	0	1		FONT 8/12	
RA_1	DT_0 / RA_0		0	1	0		1	0
0	0		1 line×256 words	2 line×128 words	4 line× 64 words	0word	0character	0character
0	1		1 line×224 words	2 line×112 words	4 line× 56 words	32words	4character	2character
1	0		1 line×192 words	2 line× 96 words	4 line× 48 words	64words	8character	4character
1	1		1 line×160 words	2 line× 80 words	4 line× 40 words	96words	12character	6character

Please refer to Item DD/CG RAM Regarding the RAM addresses.

9 THE SET DISPLAY MODE INSTRUCTION (SE)

SET ENTRY MODE

This instruction determines whether the cursor address or the display start address is incremented (+ 1) or decremented (− 1) after writing a data in the RAM with the instruction WD, or after reading a data from the RAM with the instruction RD.

The conditions for the cursor address and the display start address can be set independently of each other. The setting conditions are shown in Table 15, 16.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	CSR D/I	CSR CONDITION W	CSR CONDITION R	DSP D/I	DSP CONDITION W	DSP CONDITION R

Input to the LSI

Table 15. Cursor Address setting Conditions

CSR D/I	CSR CONDITION W	CSR CONDITION R	Cursor Address
×	0	0	No change in the cursor address occurs due to the instroction WD or RD.
1	0	1	The cursor address is decremented after reading the data with the instruction RD
0	0	1	The cursor address is incremented after reading the data with the instruction RD.
1	1	0	The cursor address is decremented after writing data using the instruction WD.
0	1	0	The cursor address is incremented after writing data using the instruction WD.
1	1	1	The cursor address is decremented after execution of the instruction WD or RD.
0	1	1	The cursor address is incremented after execution of the instruction WD or RD.

Table 16. Display Start Address setting Conditions

DSP D/I	DSP CONDITION W	DSP CONDITION R	Display Start Address
×	0	0	No change in the display start address occurs due to the instruction WD or RD.
1	0	1	The display start address is decremented after reading the data with the instruction RD.
0	0	1	The display start address is incremented after reading the data with the instruction RD.
1	1	0	The display start address is decremented after writing data with the instruction WD.
0	1	0	The display start address is incremented after writing data with the instruction WD.
1	1	1	The display start address is decremented after execution of the instruction WD or RD
0	1	1	The display start address is incremented after execution of the instruction WD or RD.

10 THE SET DISPLAY MODE INSTRUCTION (SD)

SET DISPLAY MODE

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	1	DSP ON/OFF	CSR ON/OFF	UND ON/OFF	CSR BLINK	CHR BLINK

Input to the LSI

This instruction sets the display modes.
The following display modes can be set by this instruction code.

- DSP ON/OFF=1 : This turns on all displays.
  DSP ON/OFF=0 : This turns off all displays.
- CSR ON/OFF=1 : This turns on the cursor display.
  CSR ON/OFF=0 : This turns off the cursor display.
- UND ON/OFF=1 : This turns on the underline display.
  UND ON/OFF=0 : This turns off the underline display.
- CSR BLINK=1 : This causes the cursor display to blink.
  CSR BLINK = 0 : This displays the cursor display without blinking.
- CHR BLINK=1 : This causes the character display of the cursor position to blink.
  CHR BLINK=0 : This displays the character display without blinking.

The blink displays are presented as shown Fig. 16 depending upon the position of the cursor.

11 THE SHIFT CURSOR/DISPLAY-START ADDRESS INSTRUCTION (MA)

MOVE CURSOR/DISPLAY ADDRESS

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	1	CSR	CSR D/I	DSP	DSP D/I

Input to the LSI

This instruction increments (+1) or decrements (−1) the cursor address or the display start address.
The cursor address and the display start address can be incremented or decremented independently of each other.
The results of the execution of the instruction code are as shown Table 17, 18.

CSR ON/OFF	1	1	1
CSR BLINK	1	10	1
CMR BLINK	0	1	1
Examples are for a 5×8 dot matrix	Displayed alternately	Displayed alternately	Displayed alternately

Fig.16 Example of blinking

Table 17. Shift of cursor address

CSR	CSR D/I	Cursor Address
0	×	No change occurs in the cursor address.
1	1	This decrements the cursor address. The cursor appears to be shifted to the left.
1	0	This increments the cursor address. The cursor appears to be shifted to the right.

Table 18. Shift of display start address

DSP	DSP D/I	Display Start Address
0	×	No change occurs in the display start address.
1	0	The display start address is decremented. The display as a whole appears to be shifted to the right.
1	0	The display start address is incremented. The display as a whole appears to be shifted to the left.

12 THE SET UNDERLINE MODE INSTRUCTION (SU)

SET UNDERLINE MODE

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	1	1	USR ON/OFF	UND S/R

Input to the LSI

This instruction determines whether or not to set or reset the underline bit at the time of writing an 8-bit data in the RAM by means of the instruction WD.

The instruction code can set Table 19 conditions:

When display data for which the underline bit is set is displayed in the underline display mode, a (5×1) dot underline will be displayed at the bottom row position of the dot matrix (position where the 5 × 1 dot cursor line is displayed), in addition to the character display.

Since every word in the RAM carries an underline bit, one can set the underline display for every character displayed.

Table 19. Set underline mode.

USR ON/OFF	UND S/R	Underline Bit Set/Reset Mode
1	1	One can set the underline bit by means of the instruction WD following the execution of this instruction SU.
1	0	One can reset the underline bit by means of the instruction WD following the execution of this instruction SU.
0	×	The set/reset mode is canceled so that the underline bit will neither be set nor reset by the instruction WD.

13 THE WRITE UNDERLINE BIT INSTRUCTION (WU)

WRITE UNDERLINE BIT

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	1	0	UND S/R	CSR I

Input to the LSI

This instruction sets or resets the underline bit in the 9-bit data of the cursor address of the RAM. It can also increment the cursor address after setting or resetting. This instruction performs Table 20 operations.

When display data for which the underline bit is set is displayed in the underline display mode, a 5×1 dot underline at the position of the bottom row of the dot matrix (position where the cursor line with 5×1 dot is displayed) will be displayed, in addition to the display of characters.

Since every word of the RAM carries an underline bit, the underline display can be set for every word in the display.

Table 20. Set underline and cursor address

UND S/R	CSR I	Underline Bit/Cursor Address
1	1	After setting the underline bit, the cursor address is incremented.
1	0	This sets the underline bit. No change occurs in the cursor address.
0	1	After resetting the underline bit, the cursor address is incremented.
0	0	This resets the underline bit. No change occurs in the cursor address.

14 THE SET BLINK FREQUIENCY INSTRUCTION (SB)

SET BLINK FREQUENCY

This instruction sets the blinking frequency for the cursor line or a character situated at the position of the cursor. The blinking frequencies are assigned by the instruction code as Table 21.

Table 21. Blinking frequency

B_1	B_0	Blinking Frequency
0	0	$f_B=f_{OSC}/4718592$
0	1	$f_B=(f_{OSC}/4718592)\times 2$
1	0	$f_B=(f_{OSC}/4718592)\times 4$
1	1	$f_B=(f_{OSC}/4718592)\times 8$

Here, f_{OSC} is the oscillation frequency of the oscillator.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	0	1	BLINK FREQ	
									B_1	B_0

Input to the LSI

15 THE DISPLAY/CURSOR ADDRESS HOME INSTRUCTION (MH)

MOVE DISPLAY/CURSOR ADDRESS HOME

This instruction writes $(00)_{16}$ in the display start address register and the cursor address register. By this, both the display address and the cursor address are set to the home address.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	0	0	1	1

Input to the LSI

16 THE CLEAR DISPLAY/ADDRESS HOME INSTRUCTION (CH)

CLEAR DISPLAY, MOVE DISPLAY/CUROR ADDRESS HOME

This instruction converts all of the 8-bit display data of the RAM display data region to the space code, and all of the underline bits to $(0)_2$ (nondisplaying.)

In addition, it writes $(00)_{16}$ to the display start address register and the cursor address register. By this, both the display start address and the cursor address are set to the home address.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	0	0	0	1

Input to the LSI

17 THE NO OPERATION INSTRUCTION (NOP)

NO OPERATION

This is the instruction for doing nothing. No change occurs from this instruction.

Instruction code

I/OC 1	I/OC 2	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	0	0	0	0

Input to the LSI

INTERFACES WITH μc AND μp

M50530-XXXFP can interface directly with 4-bit μc, 8-bit μc and 8085 μp.

1 The interface with 8-bit μc

The 8-bit μc and M50530-XXXFP are connected as Fig. 17: The output ports of the 8-bit μc are connected to the EX, I/OC1, I/OC2, and R/W terminals of M50530-XXXFP. The input/output port of the 8-bit μc, is connected to the data bus terminal of M50530-XXXFP.

By giving an input/output instruction to the 8-bit μc, via the ports, to the I/OC1, I/OC2, R/W, and $DB_7 \sim DB_0$ terminals, and by applying a start signal to the EX terminal, M50530-XXXFP will execute the instruction.

If one designates instructions other than RB (read busy flag and function flags) by IR (NOT RB), then M50530-XXXFP assigns $(1)_2$ to the busy flag to indicate that it is executing an instruction, when it is executing autoclear at the time of closing the power supply or it is executing an instruction IR (NOT RB). When the busy flag is set $(1)_2$, even if a subsequent instruction IR (NOT RB) is given, M50530-XXXFP will not execute it. Accordingly, in giving an instruction to M50530-XXXFP, it is necessary to examine, using the read busy flag instruction RB, whether the busy flag is $(1)_2$ or $(0)_2$. If it is $(0)_2$, an instruction IR (NOT RB) given next to M50530-XXXFP will be executed.

Fig. 18 is an example of instructions exchange between the 8-bit μc and the M50530-XXXFP timing sequence.

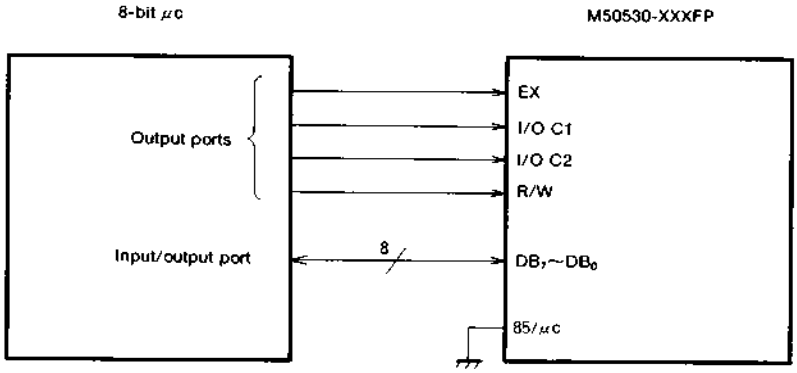


Fig.17 Interface with 8-bit μc.

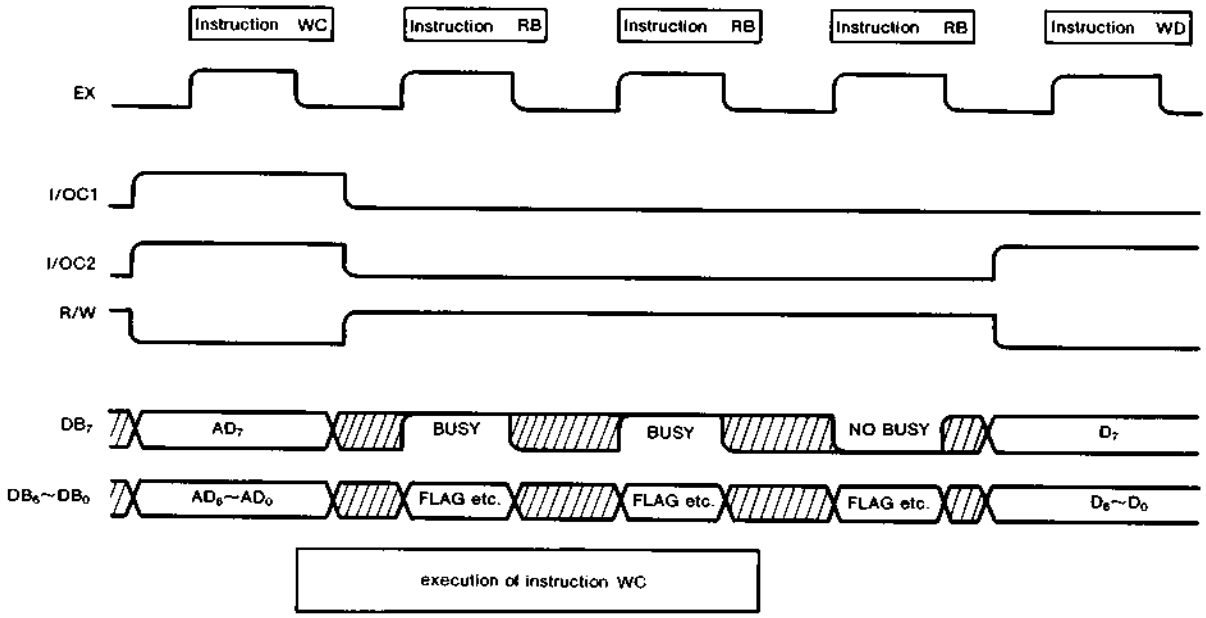


Fig.18 Interface timing with 8-bit μc

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2 The interface with 4-bit μc

The 4-bit μc and M50530-XXXFP are connected as shown Fig. 19.

The output ports of the 4-bit μc are connected to the EX, I/OC1, I/OC2, and R/W terminals of M50530-XXXFP, and the input/output port of the 4-bit μc is connected to the upper 4-bit terminals of M50530-XXXFP data bus ($DB_7 \sim DB_4$). The lower 4-bit terminals ($DB_3 \sim DB_0$) of the data bus are left disconnected, and will not be used in this case.

To simplify the explanation, the data bus instruction code $DB_7 \sim DB_0$ for the 8-bit is be renamed in the 4-bit μc mode. The upper 4-bit instruction code is defined as $UB_7 \sim UB_4$ and the lower 4-bit instruction code will be defined as $LB_3 \sim LB_0$.

Data Bus Instruction Code

8-bit mode	4-bit mode
DB_7	UB_7
DB_6	UB_6
DB_5	UB_5
DB_4	UB_4
DB_3	LB_3
DB_2	LB_2
DB_1	LB_1
DB_0	LB_0

In the case of the 8-bit μc, the EX signal is applied one time to execute an instruction. However, in the case of the 4-bit μc mode, the data bus is used twice to execute one instruction, as such it is absolutely necessary to start execution by applying the EX signal twice. Therefore, identical instruction codes are given to the I/OC1, I/OC2, and R/W terminals for both the first and second times. $UB_7 \sim UB_4$ are given to the data bus terminals $DB_7 \sim DB_4$ the first time and $LB_3 \sim LB_0$ the second time. If the instructions other than the read busy flag and function flags instruction RB are called IR (NOT RB), during execution of autoclear at the time of closing of the power supply and during execution of an instruction IR (NOT RB), M50530-XXXFP shows $(1)_2$ for the busy flag, indicating that it is in execution of an instruction. When the busy flag is set $(1)_2$, even when the next instruction IR (NOT RB) is given to M50530-XXXFP, the instruction will not be executed.

Therefore, busy flag status, $(1)_2$ or $(0)_2$, must be examined, by means of the read busy flag instruction RB before initiating an instruction. If the flag is $(0)_2$, the next instruction IR (NOT RB) given to M50530-XXXFP will be executed.

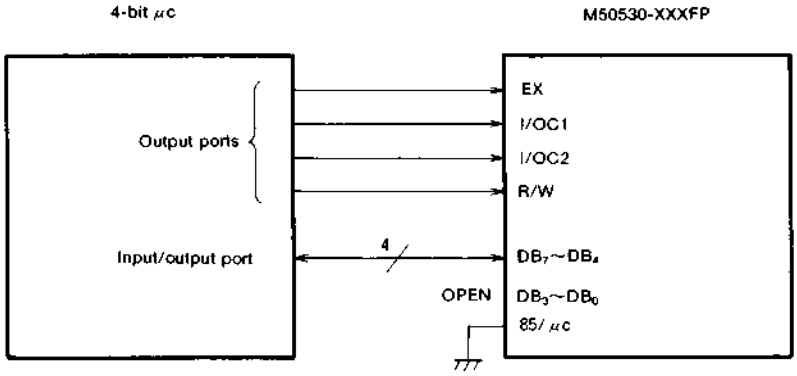


Fig.19 Interface with 4-bit μc.

In the case of the 4-bit μc, it is necessary to apply EX signal twice times for the execution of an instruction.
When the power supply is turned on, it is in the 8-bit μc mode. If 4-bit μc mode is desired, then instruction SF is given after confirming the completion of the autoclear operation. This is done with the use of the read busy flag and function flags instruction RB subsequent to the closing of the power supply (at this time still in the 8-bit mode). The instruction SF at this time is 4-bit μc mode instruction, and it is necessary to hold for two EX signals. Fig. 20 is a timing sequence diagram example of an instruction exchange between the 4-bit μc and the M50530-XXXFP.

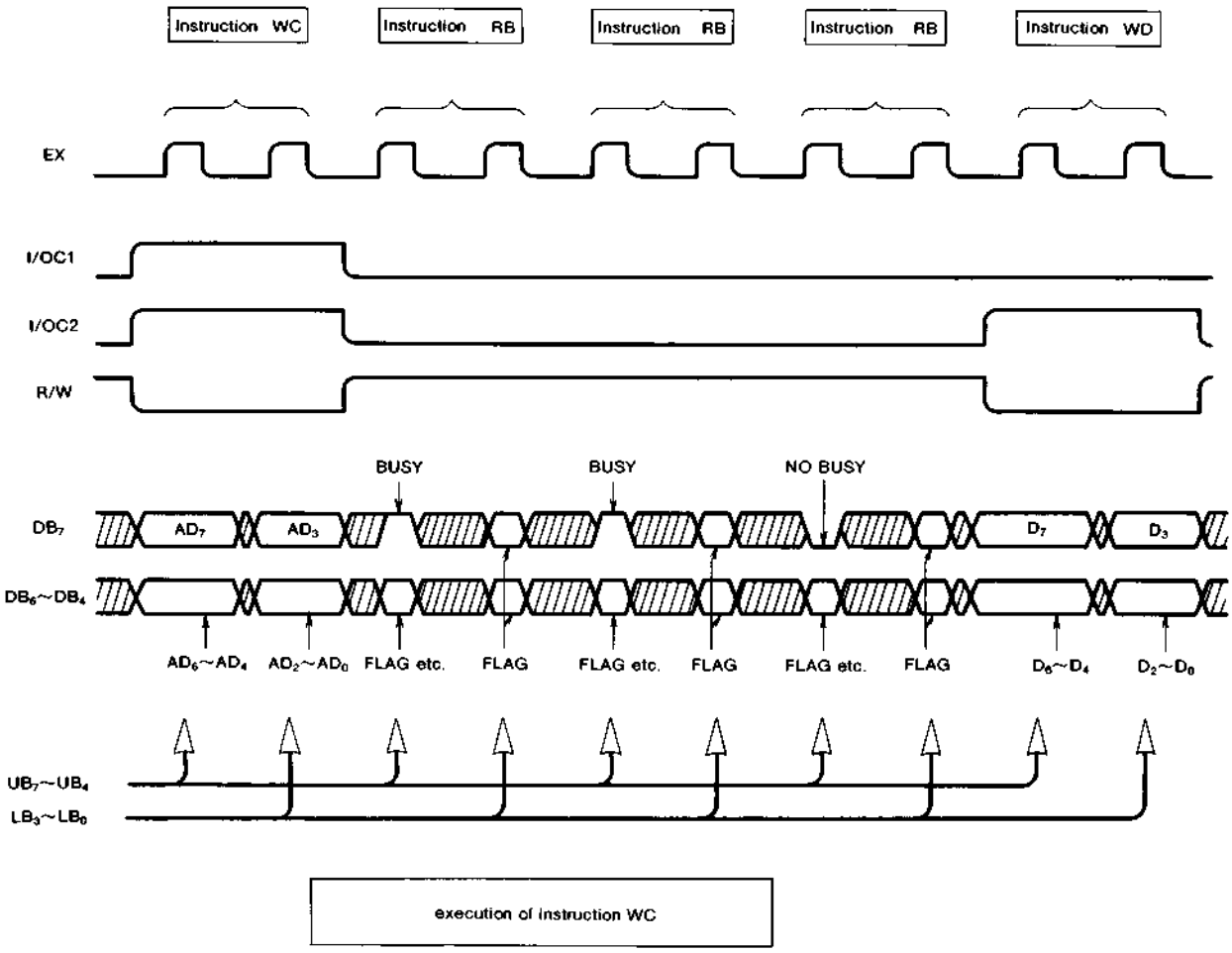


Fig.20 Interface timing with 4-bit μc.

3 The interface with 8085 μp (μp mode)

The 8-bit μp 8085 and M50530-XXXFP are connected as shown in Fig. 21.

In this mode the signal terminals ALE, $\overline{RD}$, $\overline{WR}$, and $\overline{IOM}$ unique to the 8085μp are connected to the EX, R/W, I/OC1, and I/OC2 terminals of the M50530-XXXFP. The address data bus $AD_7 \sim AD_0$ of the 8085μp is connected to the data bus $DB_7 \sim DB_0$ of M50530-XXXFP.

The instruction codes I/OC1, I/OC2, and R/W from the μc mode are sent in this mode on the address data bus $AD_7 \sim AD_0$.

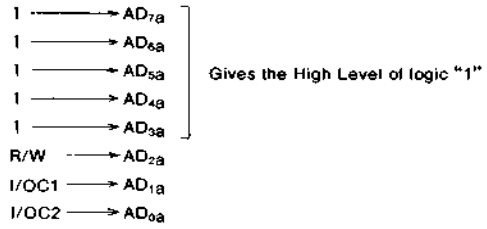
The terminals for the signals R/W, I/OC1, and I/OC2 of the M50530-XXXFP become independent of the instruction codes, and come to be used exclusively for $\overline{RD}$, $\overline{WD}$, and $\overline{IOM}$ of 8085.

To give an instruction to M50530-XXXFP from the 8085, the 8085 input and output instructions IN and OUT are used. When the $\overline{IOM}$ singal is "H", the 8085 sends two kinds of data on the 8-bit address data bus $AD_7 \sim AD_0$. Of these, if the data sent first is designated $AD_{7a} \sim AD_{0a}$ and the next data sent is designated $AD_{7b} \sim AD_{0b}$, then

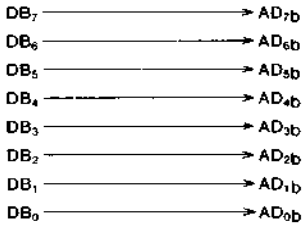
$AD_{7a} \sim AD_{0a}$ is I/O port address and

$AD_{7b} \sim AD_{0b}$ is read or write data

By using the address data bus in the above for the 8085 input and output instructions IN and OUT, M50530-XXXFP is controlled as shown below.



Next, of the instruction codes, $DB_7 \sim DB_0$ are placed on $AD_{7b} \sim AD_{0b}$ as shown below.



In the above, the address (chip select) when M50530-XXXFP is seen as an I/O port is given by

$(AD_{7a}, AD_{6a}, AD_{5a}, AD_{4a}, AD_{3a}, AD_{2a}, AD_{1a}, AD_{0a}) = (1111xxx)_2$

where the symbol x stands for 1 or 0.

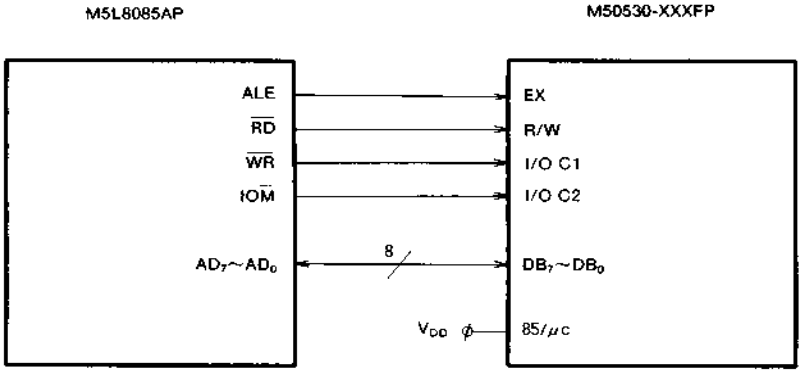
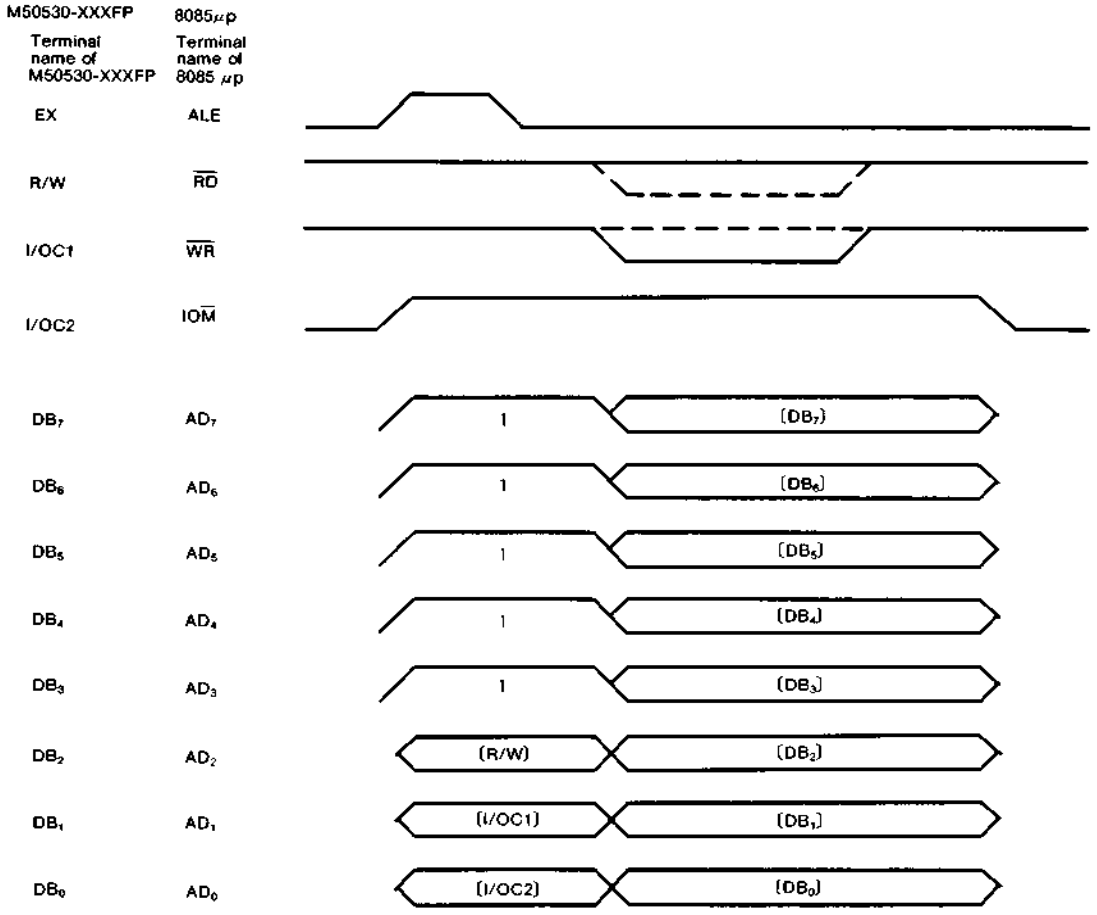


Fig.21 Interface with 8085μp.

A timing sequence diagram example of the instruction exchange between the 8085 μp and the M50530-XXXFP is shown in Fig. 22.
When many instructions are executed, the IO$\overline{M}$ signal of the μp mode (8085μp) corresponds to the EX signal of the μc mode (8-bit μc mode).

In all other cases, the instruction sequence is similar for the μp mode and the μc mode.
However, the data width of DB in the μp mode has 8 bits, and it is not possible to set the I/O interface to the 4-bit mode by means of the instruction SF.

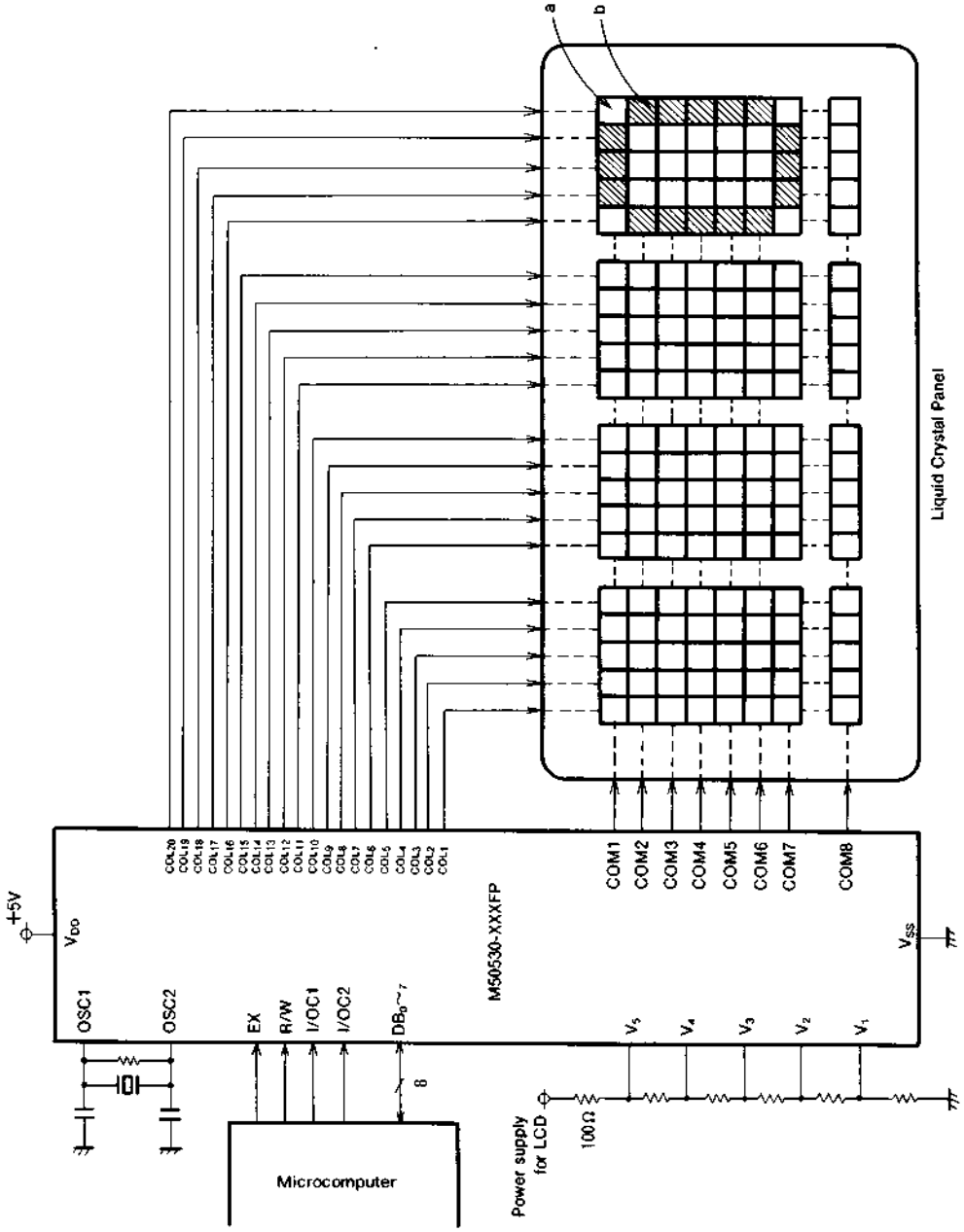


In the above, [ ] shows an instruction code.

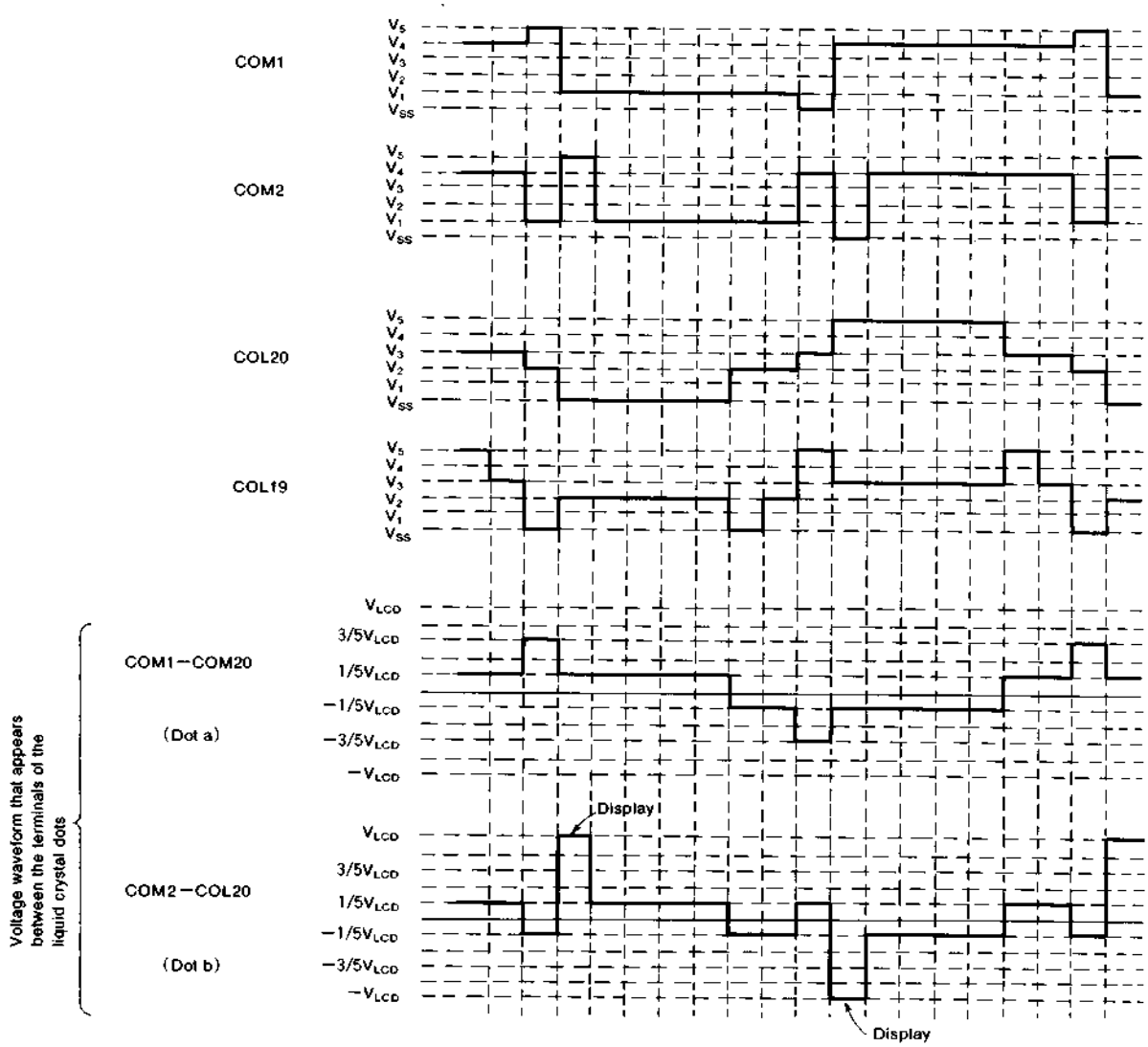
Fig.22 Interface timing with 8085μp

AN EXAMPLE OF APPLICATION CIRCUIT AND WAVEFORMS FOR LIQUID CRYSTAL DRIVING

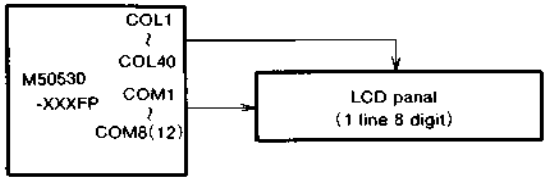
1 A circuit example (Display of 4 characters with 5×8 dots)



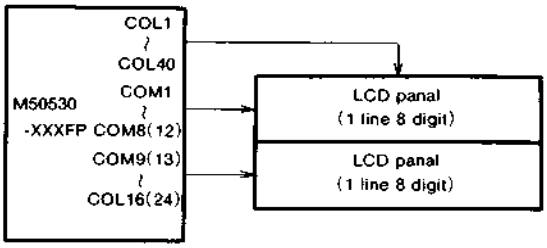
2 Waveforms for liquid crystal driving



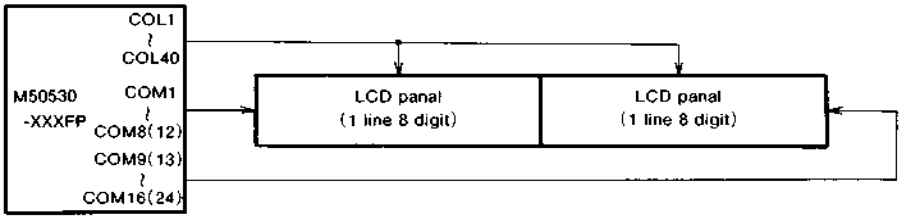
M50530-XXXFP one chip system example



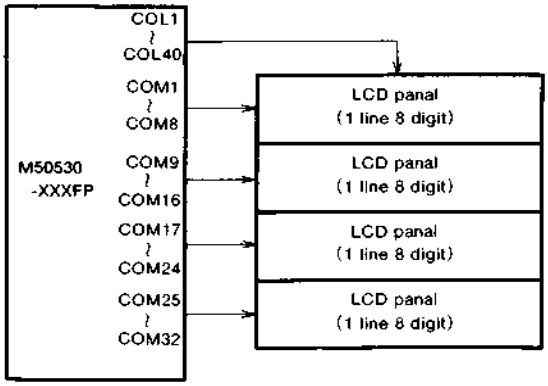
1 line 8 digit (5×8 or 5×12 dot)



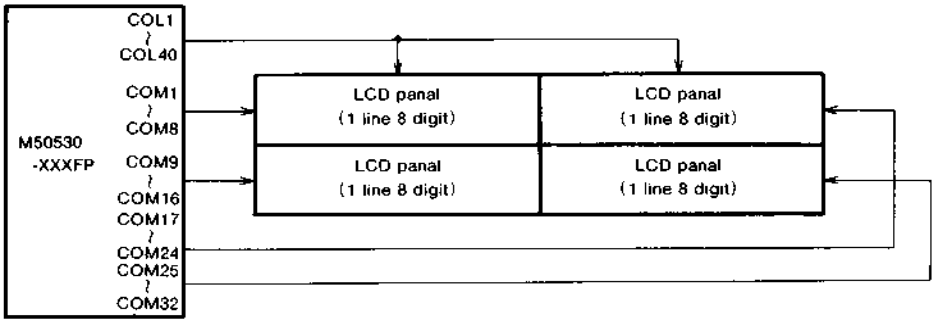
2 line 8 digit (5×8, or 5×12 dot)



1 line 16 digit (5×8, or 5×12 dot)

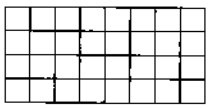
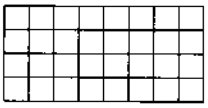
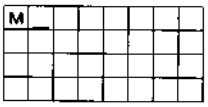
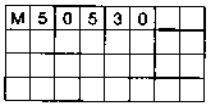
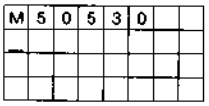
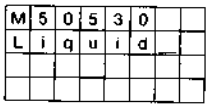


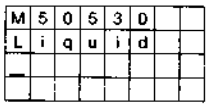
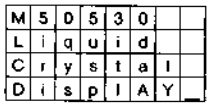
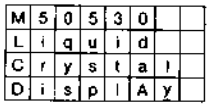
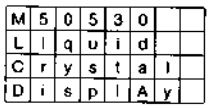
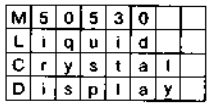
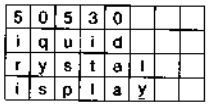
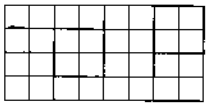
4 line 8 digit (5×8 dot)



2 line 16 digit (5×8 dot)

8-bit action, 8 characters × 4 lines display example

No.	Instruction: Abbreviation	I/O C1	I/O C2	R/W	D B 7	6	5	4	3	2	1	0	Display	Action
1	—	Power ON												Initialized by internal reset curcuit. Nothing displayed.
2	SF	Set function mode			0	0	0	1	1	1	1	0		8-bit action, 4 lines displayed. Font is 5×8 dot
3	SE	Set entry mode			0	0	0	0	1	0	1	0		Mode is set to increase cursor address after writting data by instruction WD.
4	SD	Set display mode			0	0	0	0	0	1	1	0		Cursor is displayed.
5	WD	Write data to RAM			0	1	0	0	1	0	0	1		"M" is displayed, and cursor shifts right.
6 7 8 9 10	WD	Write data to RAM			0	1	0	×	×	×	×	×		"50530" is displayed.
11	WC	Write cursor address			1	1	0	0	1	0	0	0		Cursor moves to 2nd line 1st digit.
12 13 14 15 16 17	WD	Write data to RAM			0	1	0	×	×	×	×	×		"Liquid" is displayed.

No.	Abbreviation	Instruction: I/O C1	I/O C2	R/W	D B 7	6	5	4	3	2	1	0	Display	Action
18	WC	Write cursor address												Cursor move to 3rd line 1st digit
		1	1	0	1	0	0	0	0	0	0			
19 : : 33	WD WC WD													"Crystal" is displayed. Cursor moves to 4th line, 1st digit and "DispIAY" is displayed.
34	MA	Shift cursor and display start address												Cursor address is decreased. Namely Cursor shifts left. Display start address don't change.
		0	0	0	0	0	0	1	1	1	0	0		
35	MA	Shift cursor and display start address												Cursor address is decreased. Namely Cursor shifts left. Display start address don't change.
		0	0	0	0	0	0	1	1	1	0	0		
36	WD	Write data to RAM												"a" is displayed.
		0	1	0	0	1	1	0	0	0	0	1		
37	MA	Shift cursor and display start address												Only display start address is decreased. Display shifts left.
		0	0	0	0	0	0	1	0	0	1	0		
38	CH	Clear DD RAM data and address home of display start address												Display is cleared, and cursor moves to 1st line 1st digit.
		0	0	0	0	0	0	0	0	0	0	1		

Note) Please enter instructions, after checking busy flag with instruction RB.
If busy flag is set, it is necessary to wait for the execution of the previous instruction before entering new instruction.

AN EXTENSION OF THE SYSTEM

The LCD system of the M50530-XXXFP can be expanded by connecting to it an external liquid crystal driver IC M50521FP or M50524FP.

1 AN EXTENSION OF THE COLUMN DRIVER

The M50521FP uses the M50524FP as the column driver. For this case, the SCL, CLD, CS, DST, and FRM terminals of the M50530-XXXFP are connected to the SCL, DI, CSI, DST, and FRM terminals of the driver IC, respectively. A maximum display of 256 digits (1 line) is possible.

2 AN EXTENSION OF THE COMMON DRIVER

The M50521FP also uses the M50524FP as the common driver. For this case, the CMD, DST, and FRM terminals of the M50530-XXXFP are connected to the CSI, DST, and FRM terminals of the driver IC, respectively. A maximum display of 4 lines (for duty of 1/48) of 5×12 dot characters is possible.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{DD}	Supply voltage	Logic circuit		−0.3~+7.0	V
V1~V5*		LCD driving circuit		−0.3~+15	V
V_I	Input voltage			$V_{SS}-0.3 \leqq V_I \leqq V_{DD}+0.3$	V
T_{opr}	Operating ambient temperature			−20~+70	℃
T_{stg}	Storage temperature			−40~+125	℃
P_d	Maximum power dissipation			300	mW

※In the above, it is assumed that V5>V4≧V3≧V2≧V1.

RECOMMENDED OPERATING CONDITIONS (T_a=−20 to +70℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage for logic circuit	4.5	5.0	5.5	V
V5*	Supply voltage for LCD driving circuit	3		14	V
V_{IL}	"L" input voltage	V_{SS}	V_{SS}	$0.3\times V_{DD}$	V
V_{IH}	"H" input voltage	$0.7\times V_{DD}$	V_{DD}	V_{DD}	V
f_{OSC}	Clock oscillation frequency	2	2.5	3	MHz

※Connect to V5 a resistor not less than 47Ω(±10%)in series with the power supply.

ELECTRICAL CHARACTERISTICS (unless otherwise noted, for V_{DD}=5V at T_a=25℃)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
I_{DD}	Supply current for logic	f_{OSC}=2.5MHz			10	mA
I_{V5}	Supply current for LCD	No-load LCD output V5=14V			100	μA
V_{OL}	"L" output voltage (1)	I_{OL}=2mA			0.4	V
V_{OH}	"H" output voltage (1)	I_{OH}=−2mA	3.5			V
I_I	Input leak current (2)	V_I=0~V_{CC}	−10		10	μA
V_{OZ}	OFF-state output current (3)	V_O=0~V_{CC}	−10		10	μA
R_{ON}	LCD output ON resistance (4)	V5=14V			500	Ω
		V5=5V			2	kΩ

(1) Applicable to the output terminals: DST, SCL, FRM, CS, CMD, and CLD.
(2) Applicable to the inputs of 85/μc: I/OC1, I/OC2, R/W, EX, and OSC1.
(3) Applicable to the output terminals. DB_7 to DB_0.
(4) Applicable to each LCD output of COL1 to COL40 and COM1 to COM32.

TIMING CHARACTERISTICS UNDER THE 8-BIT μc CONTROL

(unless otherwise noted, for V_{DD}=5V at T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EX)}$	EX signal pulse width		200			ns
t_{su}	Control data setup time		200			ns
t_h	Control data hold time		100			ns
$t_{d(EX-D)}$	Data output delay time	C_L=15pF			300	ns
$t_{v(EX-D)}$	Data effective time	C_L=15pF	20			ns
$t_{su(D-EX)}$	Data setup time		200			ns
$t_{h(EX-D)}$	Data hold time		100			ns

TIMING CHARACTERISTICS UNDER THE 4-BIT μc CONTROL

(unless otherwise noted, for V_{DD}=5V at T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EX)}$	EX signal pulse width		200			ns
$t_{C(EX)}$	EX signal interval		800			ns
t_{su}	Control data setup time		200			ns
t_h	Control data hold time		100			ns
$t_{d(EX-D)}$	Data output delay time	C_L=15pF			300	ns
$t_{v(EX-D)}$	Data effective time	C_L=15pF	20			ns
$t_{su(D-EX)}$	Data setup time		200			ns
$t_{h(EX-D)}$	Data hold time		100			ns

TIMING CHARACTERISTICS UNDER THE 8085 μp CONTROL

(unless otherwise noted, for V_{DD}=5V at T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EX)}$	EX signal pulse width		200			ns
t_{su}	Control data setup time		200			ns
t_h	Control data hold time		100			ns
$t_{d(D)}$	Data delay time	C_L=15pF			300	ns
$t_{v(D)}$	Data effective time	C_L=15pF	20			ns
$t_{su(D)}$	Data setup time		200			ns
$t_{h(D)}$	Data hold time		100			ns

TIMING CHARACTERISTICS FOR EXTENDED SIGNALS

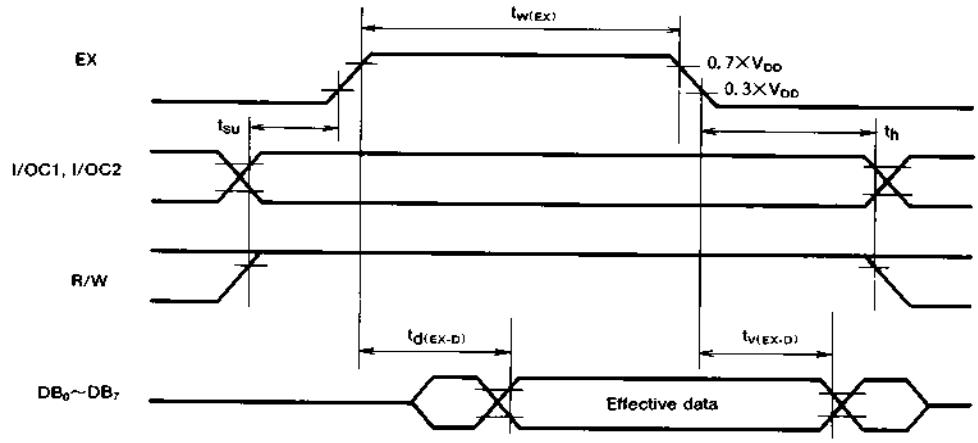
(unless otherwise noted, for V_{DD}=5V and f_{OSC}=3MHz at T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{WH(SCL)}$	Shift clock "H" pulse width		300			ns
$t_{WL(SCL)}$	Shift clock "L" pulse width		300			ns
$t_{W(CS)}$	Chip select pulse width		300			ns
$t_{h(SCL-CS)}$	Chip select hold time		300			ns
$t_{h(CS-SCL)}$	Shift clock hold time		300			ns
$t_{su(D)}$	Column data setup time		200			ns
$t_{h(D)}$	Column data hold time		300			ns
$t_{W(DST)}$	Data set pulse time		450			ns
$t_{h(SCL-DST)}$	Data set hold time		600			ns
$t_{W(CMD)}$	Common data pulse width		1950			ns
$t_{su(CMD-DST)}$	Data setup time		200			ns
$t_{d(DST-FRM)}$	Frame delay time				300	ns

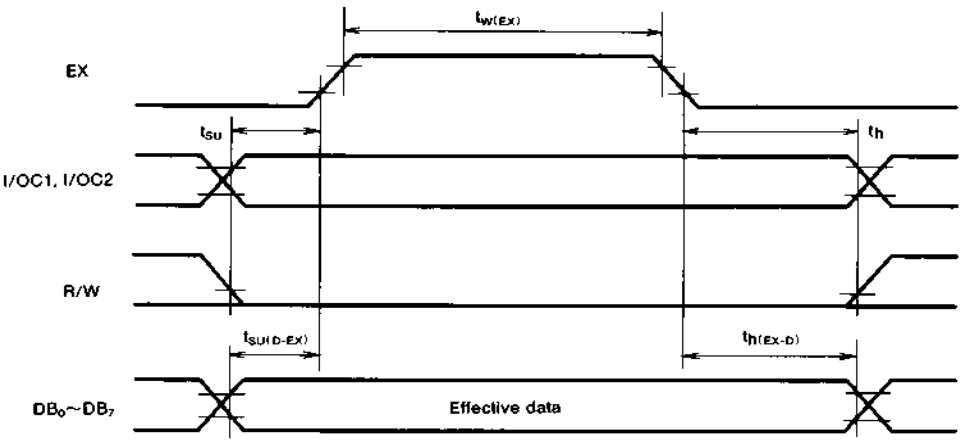
Note : All values refer to the case of load capacity of C_L=15pF.

Timing Wave forms under 8-bit μc Control

1) Read

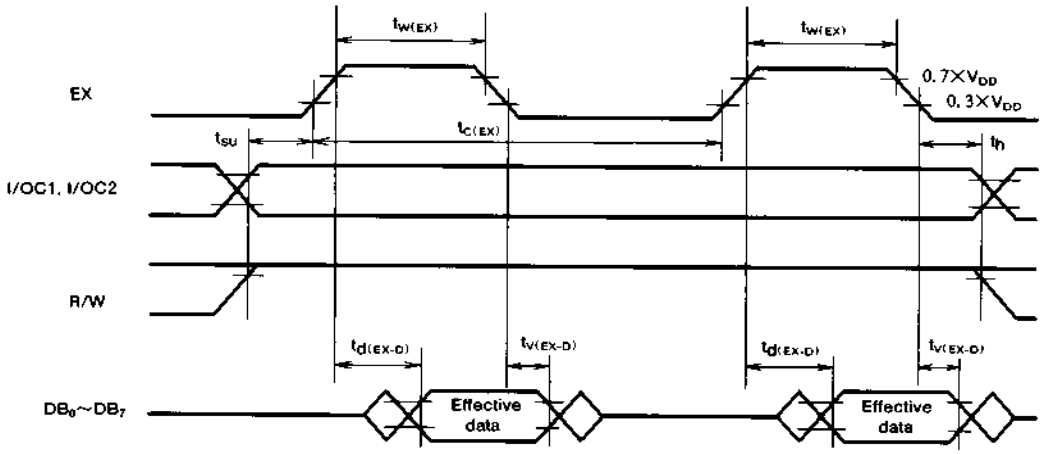


2) Write

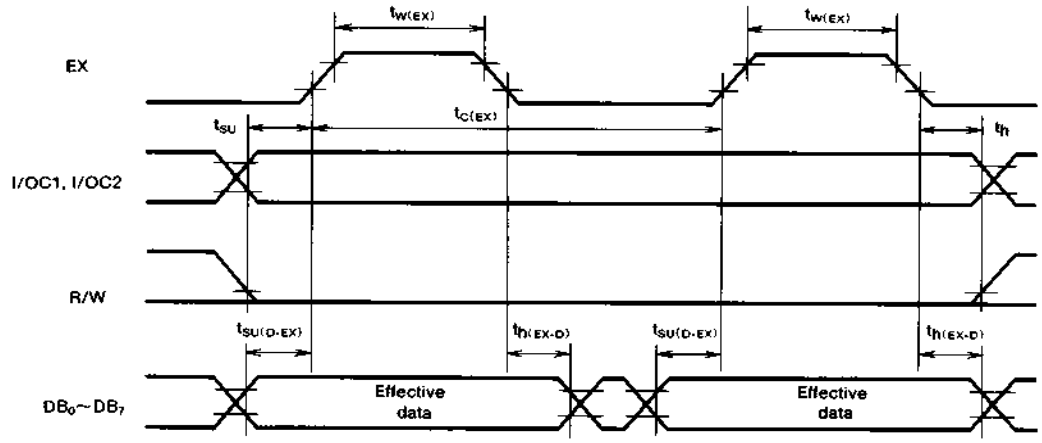


Timing Wave forms under 4-bit μc Control

1) Read

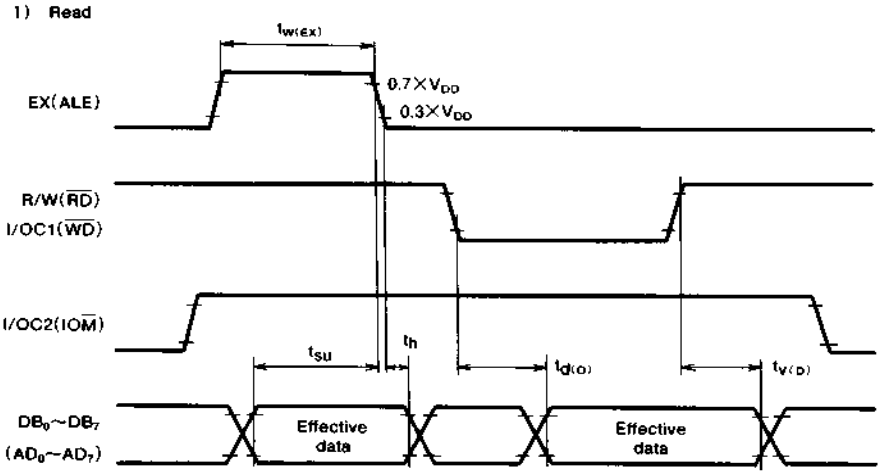


2) Write

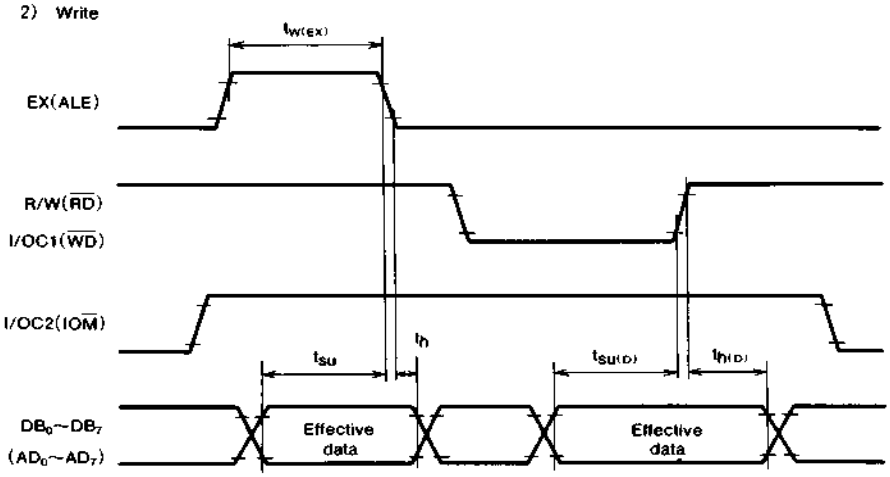


Timing Wave forms under 8085μp Control

1) Read

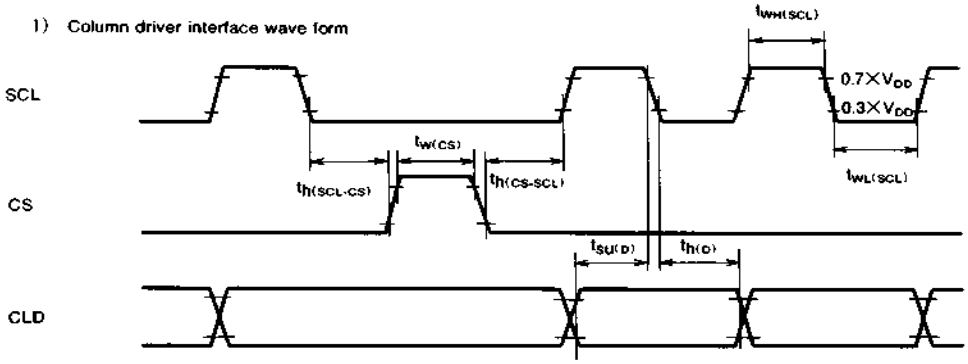


2) Write

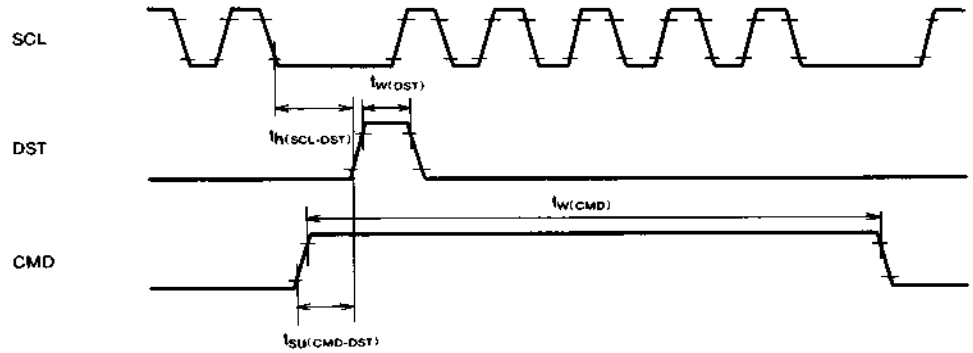


Timing Wave forms for Extended Signals

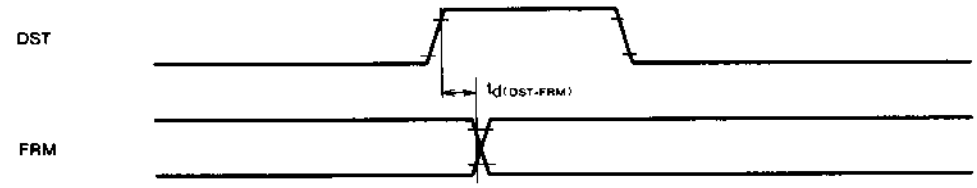
1) Column driver interface wave form



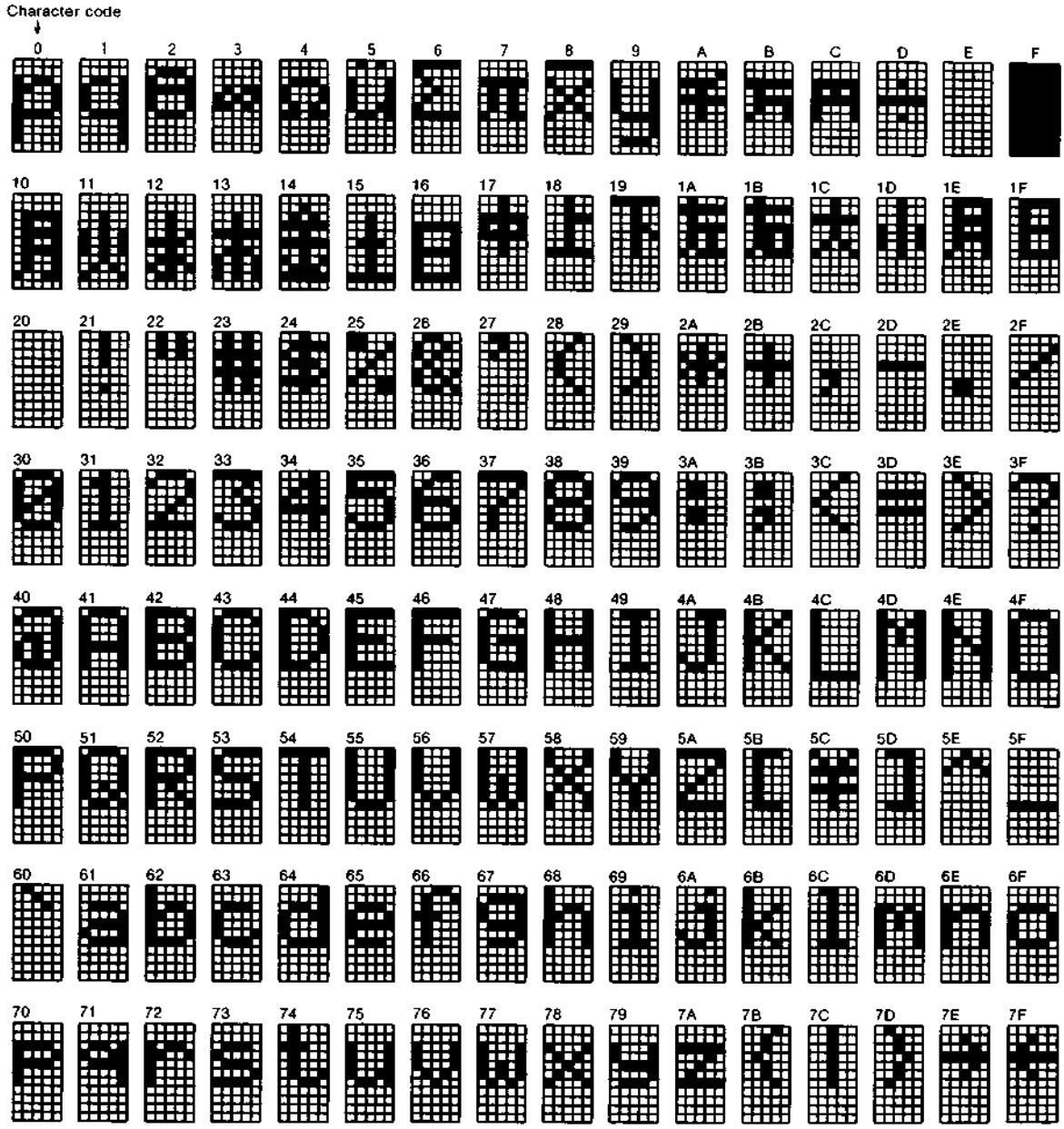
2) Common driver interface wave form



3) FRM



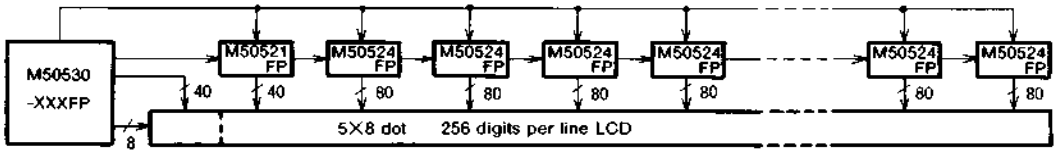
Character codes and character patterns (1/2)
(example of M50530-001FP)

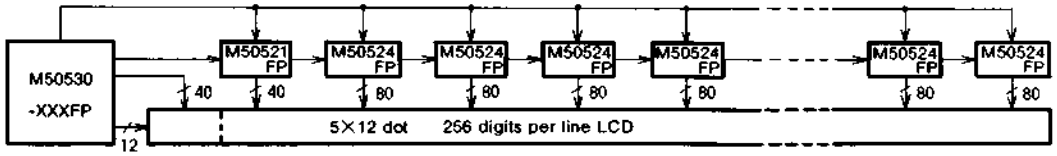


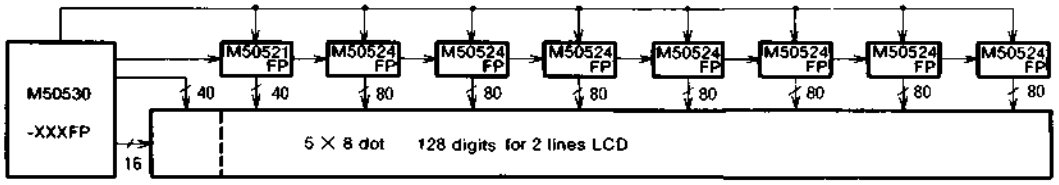
SPACE CODE : $(20)_{16}$

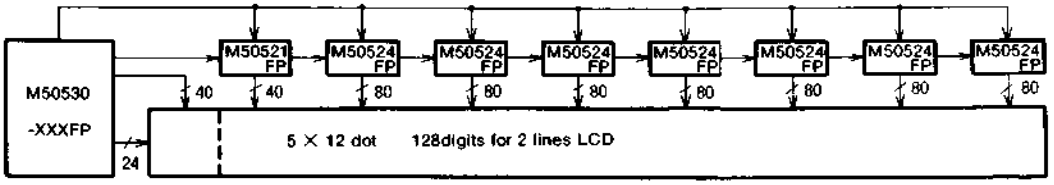
Character codes and character patterns (2/2)

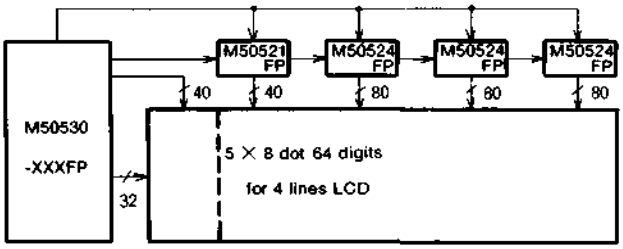
Examples of system extension (data RAM of 256 words)

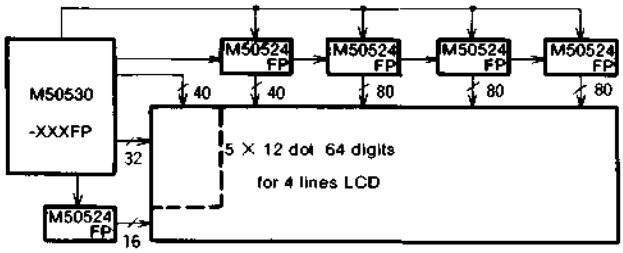




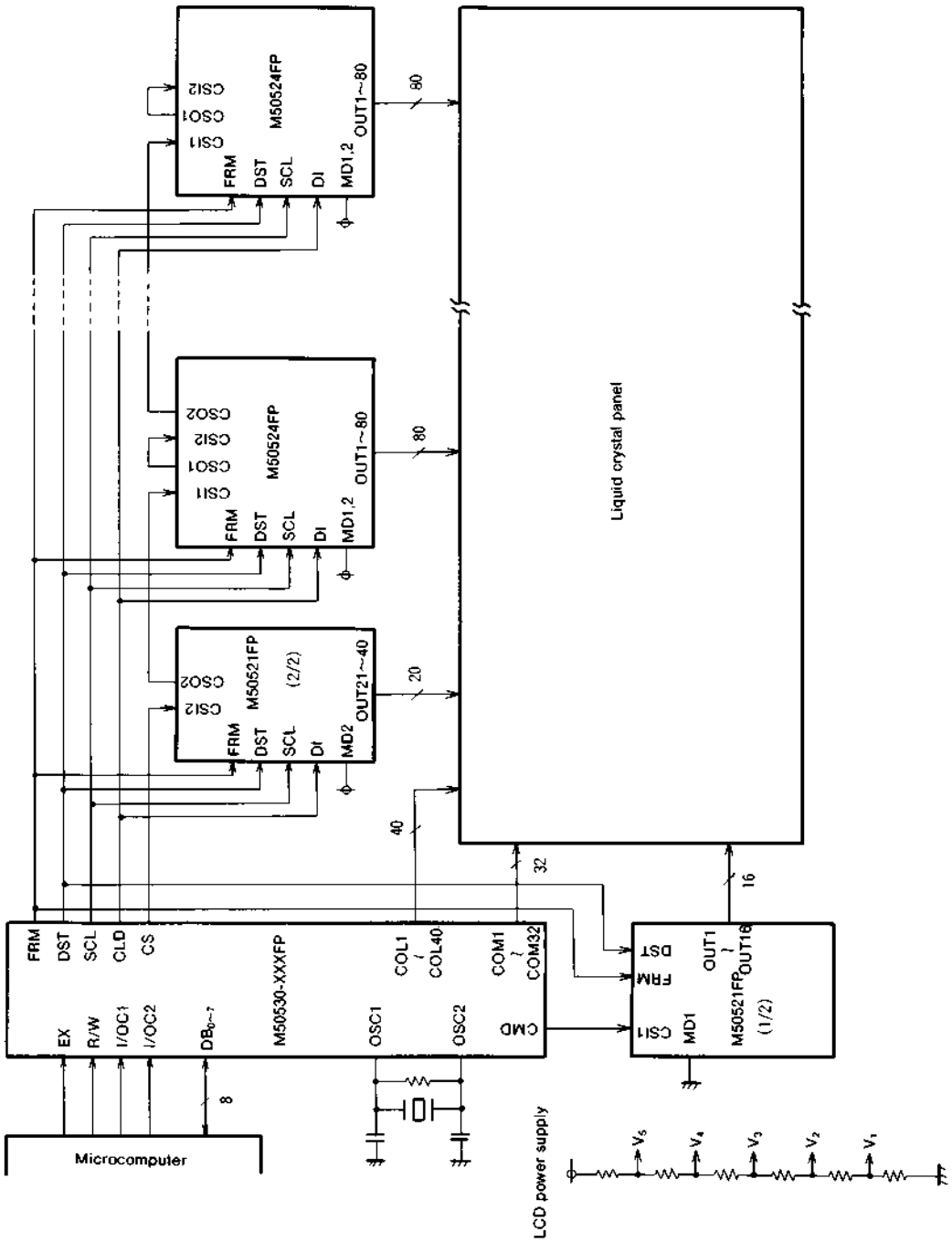








AN example of system connection



DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

JAPAN
Semiconductor Marketing Division
Mitsubishi Electric Corporation
2-3, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100, Japan
Telex: 24532 MELCO J
Telephone: (03) 218-3473
(03) 218-3499
Facsimile: (03) 214-5570

Overseas Marketing Manager
Kita-Itami Works
4-1, Mizuhara, Itami-shi,
Hyogo-ken 664, Japan
Telex: 526408 KMELCO J
Telephone: (0727) 82-5131
Facsimile: (0727) 72-2329

HONG KONG
MITSUBISHI ELECTRIC (H.K.) LTD.
25 Floor, Leighton Centre,
77, Leighton Road, Causeway Bay,
Hong Kong
Telex: 60800 MELCO HX
Telephone: (5) 773901-3
Facsimile: (5) 895-3104

SINGAPORE
MELCO SALES SINGAPORE PTE. LTD.
230 Upper Bukit Timah Road # 03-01/15
Hock Soon Industrial Complex
Singapore 2158
Telex: RS 20845 MELCO
Telephone: 4695255
Facsimile: 4695347

TAIWAN
MELCO-TAIWAN CO., Ltd.
1st fl., Chung-Ling Bldg.,
363, Sec. 2, Fu-Hsing S Road,
Taipei R.O.C.
Telephone: (02) 735-3030
Facsimile: (02) 735-6771
Telex: 25433 CHURYO "MELCO-TAIWAN"

U.S.A.
NORTHWEST
Mitsubishi Electronics America, Inc.
1050 East Arques Avenue
Sunnyvale, CA 94086
Telephone: (408) 730-5900
Facsimile: (408) 730-4972

SAN DIEGO
Mitsubishi Electronics America, Inc.
11545 West Bernardo Court
Suite 100
San Diego, CA 92128
Telephone: (619) 592-1445
Facsimile: (619) 592-0242

DENVER
Mitsubishi Electronics America, Inc.
4600 South Ulster Street
Metropoint Building, 7th Floor
Denver, CO 80237
Telephone: (303) 740-6775
Facsimile: (303) 694-0613

SOUTHWEST
Mitsubishi Electronics America, Inc.
991 Knox Street
Torrance, CA 90502
Telephone: (213) 515-3993
Facsimile: (213) 217-5781

SOUTH CENTRAL
Mitsubishi Electronics America, Inc.
1501 Luna Road, Suite 124
Carrollton, TX 75006
Telephone: (214) 484-1919
Facsimile: (214) 243-0207

NORTHERN
Mitsubishi Electronics America, Inc.
15612 Highway 7 #243
Minnetonka, MN 55345
Telephone: (612) 938-7779
Facsimile: (612) 938-5125

NORTH CENTRAL
Mitsubishi Electronics America, Inc.
800 N. Bierman Circle
Mt. Prospect, IL 60056
Telephone: (312) 298-9223
Facsimile: (312) 298-0567

NORTHEAST
Mitsubishi Electronics America, Inc.
200 Unicorn Park Drive
Woburn, MA 01801
Telephone: (617) 932-5700
Facsimile: (617) 938-1075

MID-ATLANTIC
Mitsubishi Electronics America, Inc.
800 Cottontail Lane
Somerset, NJ 08873
Telephone: (201) 469-8833
Facsimile: (201) 469-1909

SOUTH ATLANTIC
Mitsubishi Electronics America, Inc.
2500 Gateway Center Blvd., Suite 300
Morrisville, NC 27560
Telephone: (404) 368-4850
Facsimile: (404) 662-5208

SOUTHEAST
Mitsubishi Electronics America, Inc.
Town Executive Center
6100 Glades Road #210
Boca Raton, FL 33433
Telephone: (407) 487-7747
Facsimile: (407) 487-2046

CANADA
Mitsubishi Electronics America, Inc.
6185 Ordan Drive, Unit #110
Mississauga, Ontario, Canada L5T 2E1
Telephone: (416) 670-8711
Facsimile: (416) 670-8715

Mitsubishi Electronics America, Inc.
300 March Road, Suite 302
Kanata, Ontario, Canada K2K 2E2
Telephone: (416) 670-8711
Facsimile: (416) 670-8715

WEST GERMANY
Mitsubishi Electric Europe GmbH
Headquarters:
Gothear Str 8
4030 Ratingen 1, West Germany
Telex: 8585070 MED D
Telephone: (02102) 4860
Facsimile: (02102) 486-115

Munich Office:
Arabellastraße 31
8000 München 81, West Germany
Telex: 5214820
Telephone: (089) 919006-09
Facsimile: (089) 9101399

FRANCE
Mitsubishi Electric Europe GmbH
55, Avenue de Colmar
92563 Rueil Malmaison Cedex
Telex: 632326
Telephone: 47087871
Facsimile: 47513622

ITALY
Mitsubishi Electric Europe GmbH
Centro Direzionale Colleoni
Palazzo Cassiopea 1
20041 Agrate Brianza I-Milano
Telephone: (039) 636011
Facsimile: (039) 6360120

SWEDEN
Mitsubishi Electric Europe GmbH
Lastbilsvägen 6B
5-19149 Sollentuna, Sweden
Telex: 10877 (meab S)
Telephone: (08) 960468
Facsimile: (08) 966877

U.K.
Mitsubishi Electric (U.K.) Ltd.
Travellers Lane
Hatfield
Herts AL10 8XB, England, U.K.
Telephone: (0044) 7072 76100
Facsimile: (0044) 7072 78692

AUSTRALIA
Mitsubishi Electric Australia Pty. Ltd.
73-75, Epping Road, North Ryde,
P.O. Box 1567, Macquarie Centre,
N.S.W., 2113, Australia
Telex: MESYD AA 26614
Telephone: (02) (888) 5777
Facsimile: (02) (887) 3635

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