FEEDBACK COMPENSATION DESIGN FOR SWITCHED MODE POWER SUPPLIES WITH A RIGHT-HALF-PLANE (RHP) ZERO

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Abstract

A boost and flyback converters operating in Continuous Conduction Mode (CCM) are notorious for their difficult control loop stabilisation and sluggish response. This paper describes feedback compensation design of these converters. Design of the two selected compensation circuits is illustrated with a CCM boost converter, with experimental results given to verify effectiveness of each compensation circuit.

1 Introduction

Switched Mode Power Supplies (SMPS) have become a standard power source for modern electronic equipment due to their compactness and high efficiency. The SMPS maintain an output voltage to be within a prescribed limit throughout their operating conditions, by means of feedback control. Invariably, the SMPS feedback control is designed with the objectives that the output voltage must be stable and well regulated, and responds sensibly fast to disturbances such as a sudden change in load current. These targets can be achieved by appropriate design of a compensation circuit in the feedback loop.

SMPS feedback compensation circuit design method is described in [1]. Performed in the frequency domain and aided by Bode plots, the design essentially involves positioning of poles and zeros of the selected compensation circuit to compensate the undesirable characteristics of a power stage. The desired result is an open loop transfer function that has high gain and reasonably high bandwidth, and that does not violate Nyquist's stability criterion. Due to its graphical nature and simplicity, this design method has been widely adopted in practical compensation circuit design [2,3]. For a buck converter and its derivative (e.g. forward converter, half-bridge converter, etc.), the feedback compensation circuit can be designed to give the converter a wide system bandwidth and thus a fast output voltage response, while an adequate phase margin for stability is maintained. The bandwidth of up to a quarter of a switching frequency is typical for this class of converters. However, for converters whose transfer functions include a Right-Half-Plane (RHP) zero [4], such as a boost and flyback converters operating in Continuous Conduction Mode (CCM), an additional 90° phase lag introduced by the RHP zero makes the feedback loop more difficult to stabilise than their buck counterparts. The bandwidth of these converters is usually limited to be below the frequency at which the RHP zero occurs to ensure stable operation of the converters. In the realm of control engineering, a system with a RHP zero is referred to as a non-minimum phase system [5], which is known for its delayed and sluggish response. Feedback compensation design in [3,6-8] deals with the design of buck-type converters. In this paper, feedback compensation of SMPS with a non-minimum phase characteristic is presented.

2 Feedback compensation circuit design

A control block diagram of SMPS is shown in figure 1.

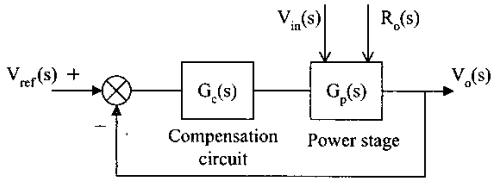


Fig. 1 A control block diagram of SMPS

$G_p(s)$ and $G_c(s)$ represent transfer functions of a power stage (power circuit and PWM modulator combined) and a feedback compensation circuit respectively. Variations of an input voltage, $V_{in}(s)$, and output resistance, $R_o(s)$, are the two major disturbances that cause an output voltage to be deviated from the desired value, $V_{ref}(s)$. The SMPS feedback loop must therefore be compensated to regulate the output voltage to be within the limits allowed by the specification, when subjected to these disturbances. For the diagram in figure 1, the transfer function $G_p(s)$ is predetermined from the chosen converter topology, mode of operation (Continuous Conduction Mode, CCM, or Discontinuous Conduction Mode, DCM), and control method (voltage mode control or current mode control). Hence, feedback compensation design involves selection of a suitable compensation circuit configuration and positioning of its poles and zeros to yield an open loop transfer function, $G_p(s)G_c(s)$, the following desired frequency characteristics:

- High gain at low frequency region to provide tight output voltage regulation
- A phase margin of at least 45° to ensure an adequate stability margin

- A crossover frequency (or bandwidth), f_c, of between one tenth and one fourth of a switching frequency for a system to respond sufficiently fast to disturbances

Feedback compensation to meet the above requirements can be performed, without much difficulty, for a buck converter and its derivative. However, for the converters with a non-minimum phase characteristic, there exists a trade-off between the system bandwidth and stability in compensation circuit design. Consider the transfer function of a CCM boost or flyback converters, which has a general form of

$$G_p(s) = K_p \frac{\left(1+\frac{s}{\omega_z}\right)\left(1-\frac{s}{\omega_{zRHP}}\right)}{1+\left(\frac{s}{\omega_p Q}\right)+\left(\frac{s}{\omega_p}\right)^2} \quad (1)$$

where ω_p, ω_z, and ω_{zRHP} are angular frequencies of an output filter pole, ESR zero, and RHP zero respectively, and Q is a quality factor. Asymptote Bode plots of equation (1) are depicted in figure 2, for the case where f_{zRHP} is greater than f_z. Slopes of –1 and –2 denote –20dB/decade and –40dB/decade respectively.

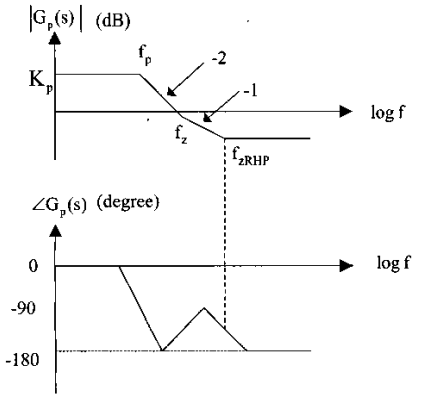


Fig. 2 Asymptote Bode plots of equation (1)

It can be seen that a 90° phase lag contributed by the RHP zero at f_{zRHP} makes the phase of $G_p(s)$ direct toward -180°. Thus, in compensating $G_p(s)$ to attain a sufficient amount of a phase margin requires that the crossover frequency, f_c, be selected below f_{zRHP}. The situation will be even worse if the RHP zero precedes the ESR zero, i.e. $f_{zRHP} < f_z$. In this case, the phase lag of $G_p(s)$ at f_{zRHP} will approach –270° and f_c will have to be selected below the frequency of the output filter pole, f_p.

3 Compensation circuits

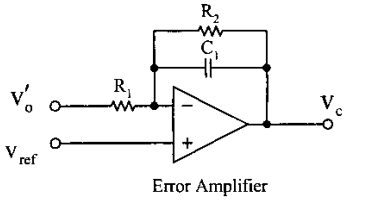
The compensation circuit configuration is selected based on compensation strategies used. The most simple strategy is to place a pole at low frequencies (required for improved output voltage regulation) and roll off the open loop gain with f_c well below f_p of the power stage, where a sufficient phase margin is obtained. Despite its simplicity, this compensation technique is disadvantageous in that the system bandwidth is very limited and thus the output voltage response sluggish. Another compensation approach is to place poles and zeros to compensate the undesirable characteristics of the power stage. This allows the system bandwidth to be extended to the frequency close to f_{zRHP} and considerable improvement in output voltage response to be achieved, at the expense of more design effort required as compared with the first approach. Though other compensation circuits may be used, in this paper a single-pole and two-pole two-zero compensation circuits described below are selected to realise the former and latter strategies respectively.

3.1 Single-pole compensation circuit

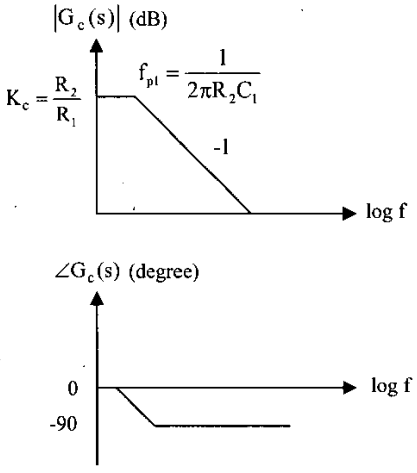
A single-pole compensation circuit (figure 3(a)) is expressed by the transfer function

$$G_c(s) = K_c \frac{1}{\left(1+\frac{s}{\omega_{p1}}\right)} \quad (2)$$

where $K_c=R_2/R_1$ and $\omega_{p1} = 1/R_2C_1$. Asymptote Bode plots of equation (2) are depicted in figure 3(b). The circuit contains a pole at f_{p1}, which is usually placed at low frequencies, a requirement for good output voltage regulation. When used to compensate a converter with a RHP zero, the crossover frequency, f_c, will be selected to be at least 50% below f_p in figure 2 to avoid f_{p1} being too close to f_p that leads to deterioration of the phase margin. Feedback compensation using the single-pole circuit is illustrated in section 4.1.



(a)



(b)

Fig. 3 (a) A single-pole compensation circuit (b) its asymptote Bode plots

3.2 Two-pole two-zero compensation circuit

A two-pole two-zero compensation circuit (figure 4(a)) is expressed by the transfer function

$$G_c(s) = K_c \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \quad (3)$$

where $K_c=R_3/(R_1+R_2)$, $\omega_{z1} = 1/(R_4C_2)$, $\omega_{z2} = 1/(R_2C_1)$, $\omega_{p1} = 1/(C_2(R_3+R_4))$, and $\omega_{p2} = (R_1+R_2)/(R_1R_2C_1)$. Asymptote Bode plots of equation (3) are depicted in figure 4(b). When used to compensate a converter with a RHP zero, the first pole at f_{p1} is placed at low frequencies, a requirement for good output voltage regulation. The two zeros at f_{z1} and f_{z2} are placed at frequencies near f_p in figure 2 to nullify the effects of the output filter's double poles. The second pole at f_{p2} is placed at frequencies near f_z in figure 2 to nullify the effects of the ESR zero. The crossover frequency, f_c, will be selected to not exceed f_{zRHP} in figure 2 to avoid potential instability due to an accumulated phase lag of -180° caused by the pole at f_{p1} and the RHP zero at f_{zRHP}. Feedback compensation using the two-pole two-zero circuit is illustrated in section 4.2.

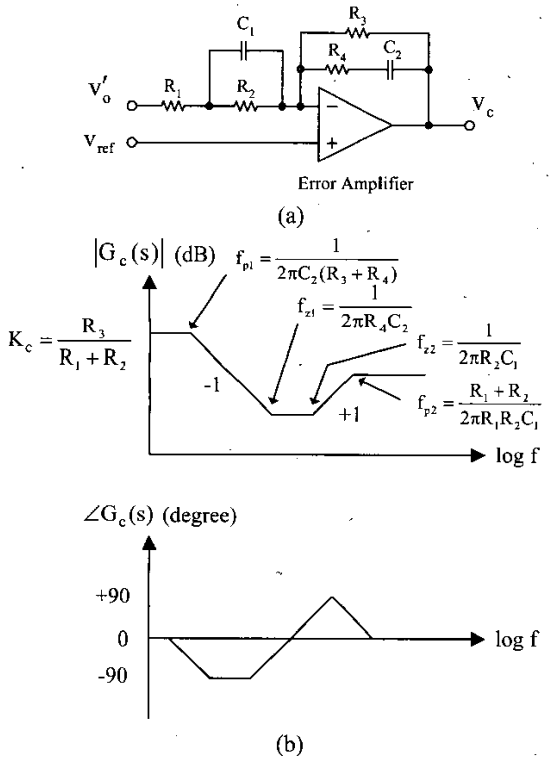


Fig. 4 (a) A two-pole two-zero compensation circuit (b) its asymptote Bode plots

4 Design Examples

Compensation circuit design is illustrated with a CCM boost converter in figure 5.

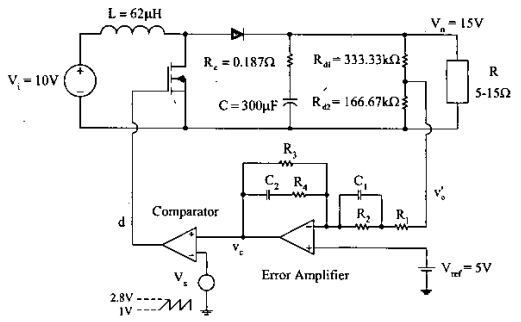


Fig. 5 A CCM boost converter

The converter's specifications are as follows: V_i = 10V, V_o = 15V, I_o = 1A to 3A, switching frequency (f_s) = 100kHz. The compensation circuit design is carried out for a maximum load current (R = 5Ω). It will be later shown that the result is also valid when the load current is minimum (R = 15Ω). Various unknowns of the boost converter's transfer function in equation (1) are determined as follows:

$$K_p = \frac{V_o^2}{V_s V_i}\left(\frac{R_{d2}}{R_{d1}+R_{d2}}\right) = \frac{(15)^2}{(1.8)(10)}\left(\frac{166.67\times10^3}{500\times10^3}\right) = 4.17\ (12.40\text{dB})$$

$$f_p = \frac{V_i}{2\pi V_o\sqrt{LC}} = \frac{10}{2\pi(15)\sqrt{(62\times10^{-6})(300\times10^{-6})}} = 778\text{Hz}$$

$$f_z = \frac{1}{2\pi R_c C} = \frac{1}{2\pi(0.187)(300\times10^{-6})} = 2{,}837\text{Hz}$$

$$f_{zRHP} = \frac{V_i^2 R}{2\pi V_o^2 L} = \frac{(10)^2(5)}{2\pi(15)^2(62\times10^{-6})} = 5{,}704\text{Hz}$$

$$Q = \frac{(V_i/V_o)^2 R}{\omega_p\left((V_i R R_c C/V_o)+L\right)} = \frac{(10/15)^2(5)}{2\pi(778)\left(\left((10)(5)(0.187)(300\times10^{-6})/(15)\right)+(62\times10^{-6})\right)} = 1.83$$

An asymptote magnitude plot of the boost power stage is depicted in figures 6(a) and 8(a). The estimated gains at f_p, f_z, and f_{zRHP} are 12.4dB, -10.1dB, and –16.1dB respectively.

4.1 Design of single-pole compensation circuit

Asymptote magnitude plots, illustrating the single-pole compensation circuit design, are shown in figure 6. As stated in section 3.1, the design of this circuit requires the crossover frequency, f_c, be selected at least 50% below f_p of the power stage. Here, f_c is chosen at $0.2f_p$ or 150Hz. At f_c, $G_p(s)$ is found to have a gain of 12.4dB; therefore the required gain of $G_c(s)$ at this frequency is –12.4dB. The pole of $G_c(s)$ at f_{p1} must be placed at a frequency lower than f_c for the overall system to have high gain at low frequencies. It is positioned at 0.04Hz and results in the low frequency gain of 60dB for G_c (s) and 72.4dB for $G_p(s)G_c(s)$. Having established the gain frequency characteristic of $G_c(s)$ (figure 6(b)), the compensation circuit component values are calculated and rounded off to the nearest standard values, obtaining R_1 =

5.6kΩ, R_2 = 5MΩ, and C_1 = 1μF. This design result yields Bode plots of $G_p(s)G_c(s)$ shown in figure 7. It can be seen that the designed compensation circuit yields the stable system for both minimum and maximum load currents, with a phase margin of about 86°. In the figure, the low frequency gain and crossover frequency are approximately 70dB and 121Hz respectively. It should be noted that this value of f_c is lower than the one used in the design (f_c=150Hz). This discrepancy is largely due to the asymptote approximation assumed in the design process and the "round-off" error in which the calculated compensation component values were rounded off to match the nearest standard values.

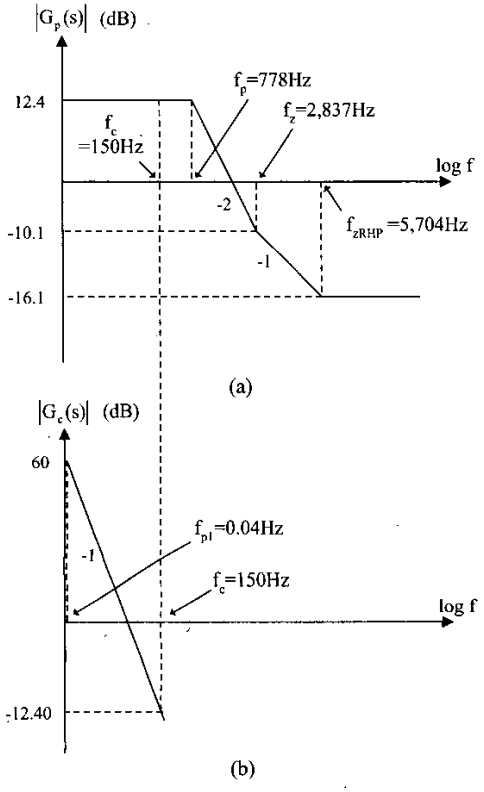


Fig. 6 Design of the single-pole circuit

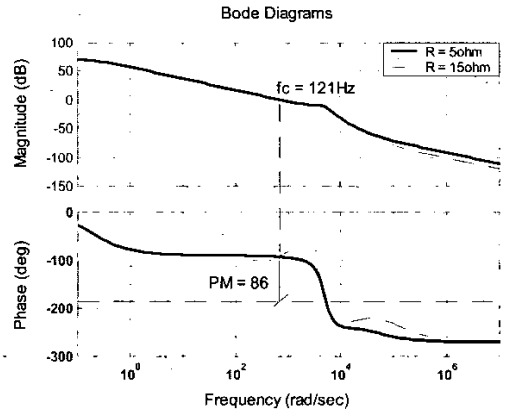


Fig. 7 Bode plots of $G_p(s)G_c(s)$ given by the designed single-pole compensation circuit

4.2 Design of two-pole two-zero compensation circuit

Asymptote magnitude plots, illustrating the two-pole two-zero compensation circuit design, is given in figure 8. As stated in section 3.2, the design of this circuit requires the crossover frequency, f_c, be selected below f_{zRHP} of the power stage. Here, f_c is chosen at 5,000Hz (whilst f_{zRHP} = 5,704Hz). At f_c, $G_p(s)$ is found to have a gain of −15dB; therefore the required gain of $G_c(s)$ at this frequency is 15dB. The two zeros of $G_c(s)$ are placed at $f_{z1} = f_{z2}$ = 700Hz (near f_p of the power stage), the second pole at f_{p2} = 3,000Hz (near f_z of the power stage), and the first pole at f_{p1} = 0.92Hz to give the low frequency gain of 60dB for $G_c(s)$ and 72.4dB for $G_p(s)G_c(s)$. The gain of $G_c(s)$ at f_{z1} (= f_{z2}), and f_{p2} are determined to be 2.4dB and 15dB respectively. Having established the gain frequency characteristic of $G_c(s)$ (figure 8(b)), the compensation circuit component values are calculated and rounded off to the nearest standard values, obtaining R_1 = 560Ω, R_2 = 1.8kΩ, R_3 = 3.3MΩ, R_4 = 1.8kΩ, and $C_1 = C_2$ = 0.12μF. This design result yields Bode plots of $G_p(s)G_c(s)$ shown in figure 9. It can be seen that the designed compensation circuit yields the stable system for both minimum and maximum load currents, with a phase margin of about 45°. In the figure, the low frequency gain and crossover frequency are approximately 74dB and 3.5kHz respectively. It should be noted that this value of f_c is smaller than the one used in the design (f_c=5kHz). The reasons for this discrepancy are similar to those explained in section 4.1.

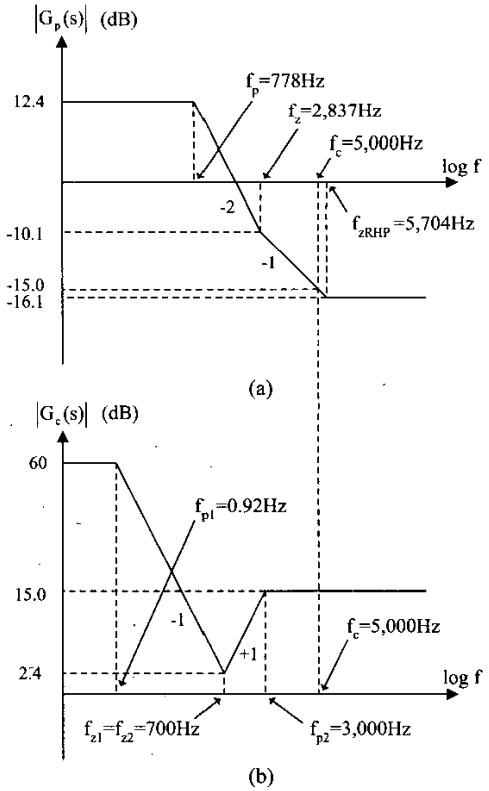


Fig. 8 Design of the two-pole two-zero circuit

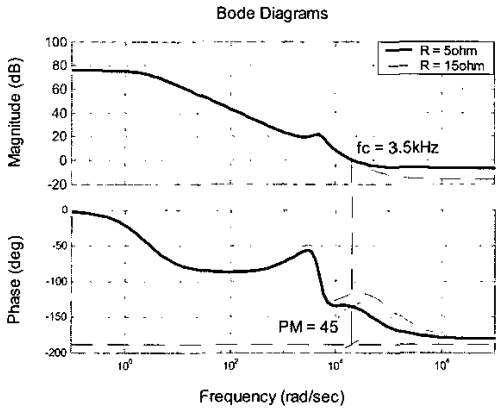


Fig. 9 Bode plots of $G_p(s)G_c(s)$ given by the designed single-pole compensation circuit

5 Experimental results

A prototype CCM boost converter shown in figure 10 is built to test performance of the designed compensation circuits.

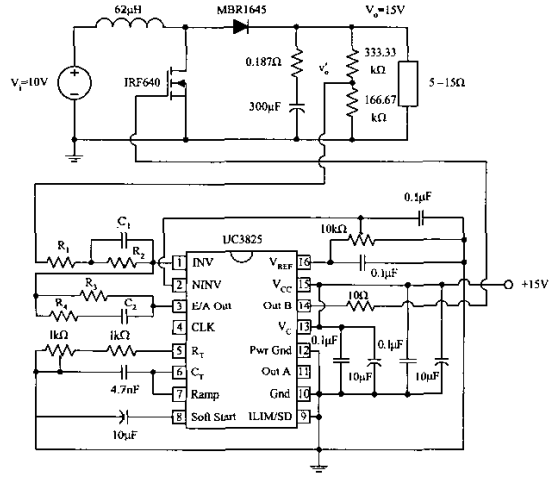


Fig. 10 A prototype CCM boost converter

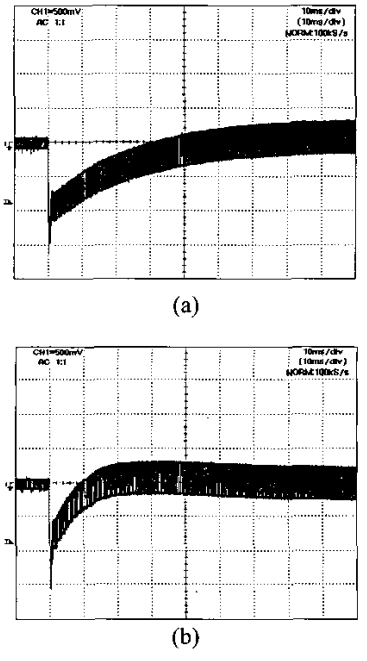
The SMPS control IC UC3825 [9] is employed as a control circuit. The compensation circuits designed in sections 4.1 and 4.2 are connected around an error amplifier available at pins 1, 2, and 3 of the IC. In the figure, the two-pole two-zero compensation circuit is shown; for the single-pole compensation circuit R_2, R_4, and C_1 are zeroed.

The output voltage of the prototype boost converter given by each type of compensation circuits is measured and shown in table 1. It can be seen that the output voltage is well regulated at minimum and maximum load currents. Good output voltage regulation is due to that the design of both compensation circuits yields the system high gain at low frequencies, about 70dB for the single-pole circuit (figure 7) and about 74dB for the two-pole two-zero circuit (figure 9). The output voltage is noticed to have slightly increased at full load. This could have been caused by the larger output voltage ripple at full load.

The output voltage response given by each type of compensation circuit, when load current is stepped from 1A to 3A, is shown in figure 11. The maximum voltage drop and settling time are approximately 1.5V and 40ms for the single-pole compensation circuit (figure 11(a)), and approximately 1.5V and 15ms for the two-pole two-zero compensation circuit (figure 11(b)). The converter employing the latter compensation circuit has a faster response because of its larger system bandwidth (f_c) as indicated in figure 9.

Compensation circuit	V_i (V)	I_o (A)	V_o (V)
Single-pole	10	1	15.00
		3	15.02
Two-pole two-zero	10	1	15.00
		3	15.09

Table 1 Measured output voltage of the prototype boost converter



(a)

(b)

Fig. 11 Output voltage response of the prototype boost converter due to a 2A step load, with (a) the designed single-pole circuit (b) the designed two-pole two-zero circuit.

6 Conclusions

In this paper, feedback compensation design of SMPS with a RHP zero has been described and design examples illustrated with a CCM boost converter, using a single-pole and two-pole two-zero compensation circuits. While both circuits are capable of providing the converter good output voltage regulation, feedback compensation with the two-pole two-

zero compensation circuit can achieve the greater system bandwidth close to the RHP zero frequency and thus the faster output voltage response. These are confirmed by the experimental results in table 1 and figure 11. Though not shown in the paper, the design procedure is also valid for a CCM flyback converter. However, in off-line applications where a DC input voltage to a converter may contain a large voltage ripple, additional design effort is needed to suppress propagation of this input voltage ripple onto the output.

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