DATA MODUL
DISPLAY AND SYSTEM SOLUTIONS

Specification for

MGLS12864 p.06-12
MGLS12864 p.13-23
MGLS12864-LED03 p.24-36
MGLS12864T p.37-46

Reversion: 0.0

Nov.2000

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PRELIMINARY SPECIFICATION

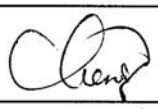
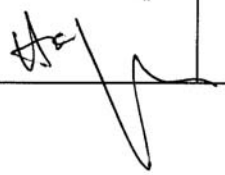
FOR

LCD MODULE TYPE

ITEM NO.: MGLS12864-46

MGLS12864-HT-HV-F (SAMSUNG IC)

(DOC. REVISION 0.0)

DEPARTMENT	NAME	SIGNATURE	EFFECTIVE DATE
PREPARED BY	PHILIP CHENG		2000.11.13
APPROVED BY	K.P.HO		2000.11.13

DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
0.0	2000.11.13		PHILIP CHENG	K.P.HO

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Preliminary Specification
of
LCD Module Type
Item No.: MGLS12864-46
MGLS12864-HT-HV-F (SAMSUNG IC)

1. General Description

- 128 x 64 dots FSTN HT Positive Black & White Reflective Dot Matrix LCD Graphic Module.
- Driving scheme: 1/64 multiplexed drive, 1/9 bias.
- Viewing direction: 6 o'clock.
- 'SAMSUNG' KS0107B flat pack 64 channel LCD common driver or equivalent.
- 'SAMSUNG' KS0108B flat pack 64 channel LCD segment driver or equivalent.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	78.0(W) x 70.0(H) x 10.0 Max.(D)	mm
Viewing area	62.0(W) x 44.0(H)	mm
Active area	56.27(W) x 38.35(H)	mm
Display format	128(Horizontal) x 64(Vertical)	dots
Dot size	0.39(W) x 0.55(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.44(W) x 0.60(H)	mm
Weight	TBD	grams

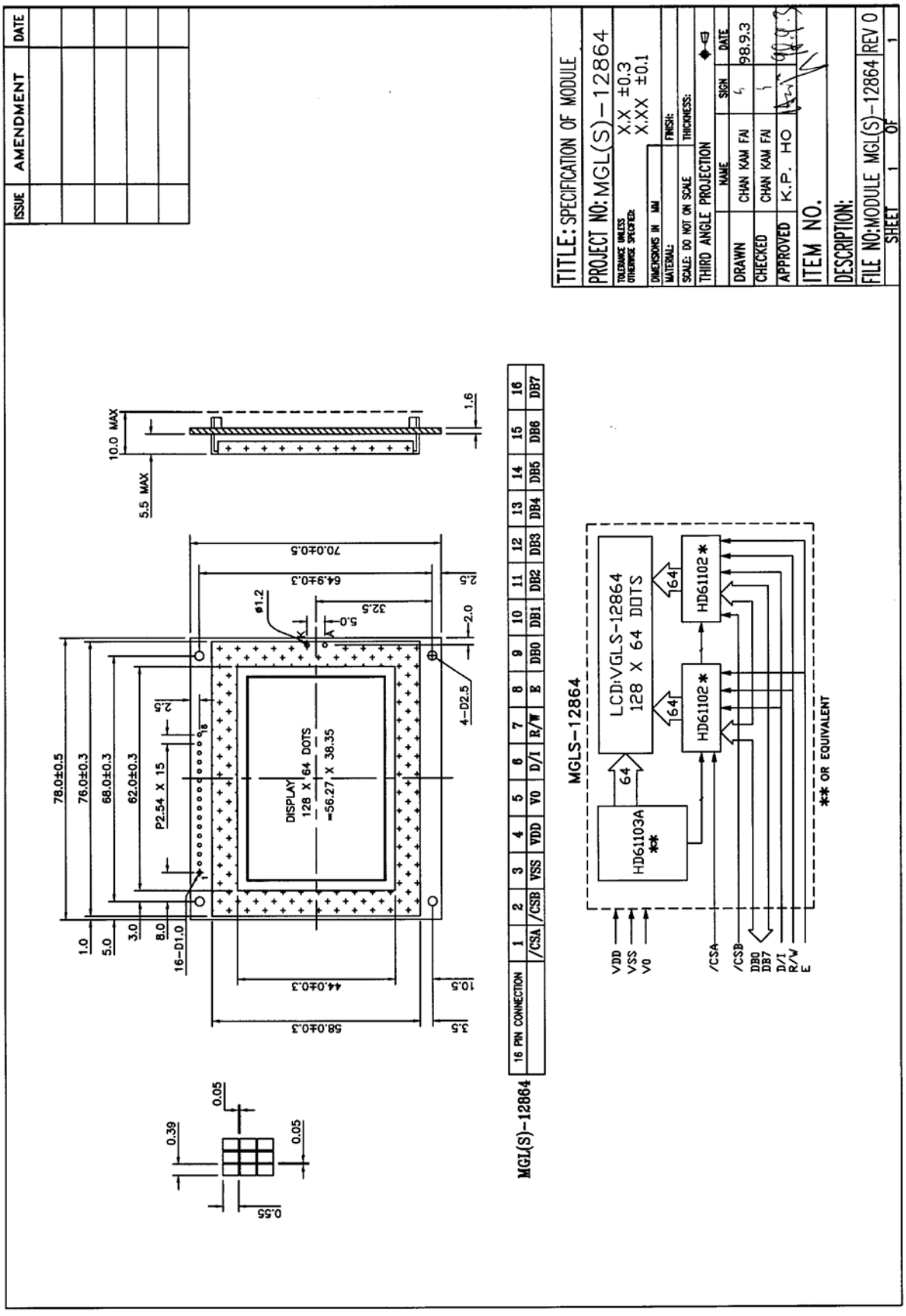


Figure 1: Outline Drawing Of The Module MGLS12864-HT-HV-F (SAMSUNG IC).

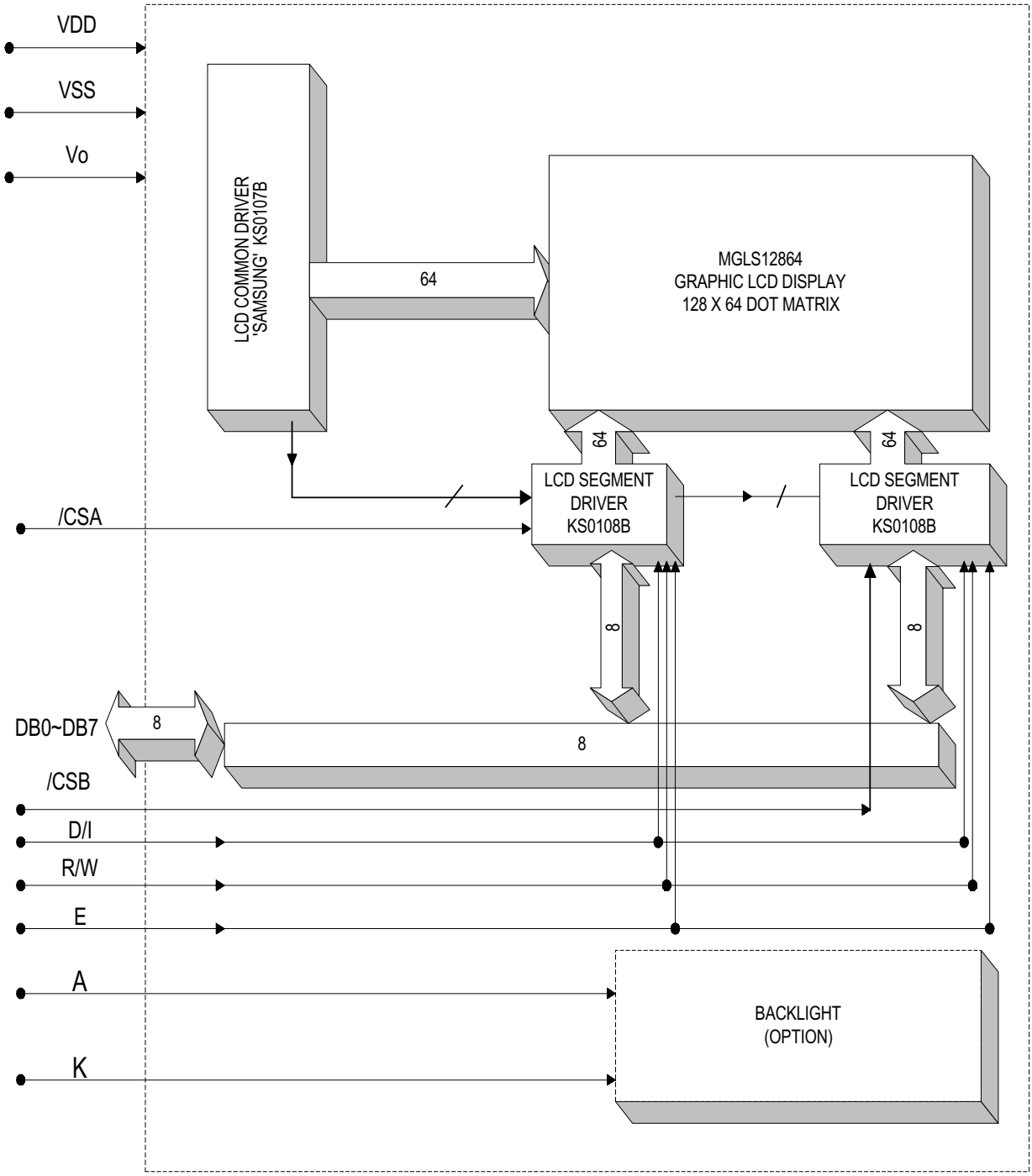


Figure 2: Block diagram

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings (Ta = 25 ºC)

Table 2

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	V_{DD} - V_{SS}	-0.3	+7.0	V
Power Supply voltage (LCD drive)	V_{DD} - V_O	-0.3	+17.0	V
Input voltage	Vin	-0.3	V_{DD} +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to Vss = 0V.

3.2 Environmental Condition

Table 3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	Note 1		Note 1		no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Note 2		Note 2		3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Note 3		Note 3		3 directions

Note 1: 95% max. RH for Ta ≤ 40°C

< 95% RH for Ta > 40°C

Note 2: Frequency: 10 ~ 55 Hz

Amplitude: 0.75 mm

Duration: 20 cycles in each direction.

Note 3: Pulse duration: 11 ms

Peak acceleration: 981 m/s^2 = 100g

Number of shocks: 3 shocks in 3 mutually perpendicular axes.

4. Electrical Specifications

4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	/CSA	Chip selection for the first column driver
2	/CSB	Chip selection for the second column driver
3	Vss	Ground (0V)
4	V_{DD}	Power supply for logic & LCD (+5V)
5	Vo	Power supply for LCD drive
6	D/I	Data/Instruction. "High" for display data and "Low" for display control data.
7	R/W	Read/Write. "High" for MPU to read data appearing at DB0 to DB7 and "Low" for DB0 to DB7 be accepting at fall of E.
8	E	Chip Enable. At read(R/W = High): Data appears at DB0 to DB7 while E is at high level. At write(R/W = Low): Data of DB0 to DB7 is latched at the fall of E.
9	DB0	Data input/output (LSB)
10	DB1	Data input/output
11	DB2	Data input/output
12	DB3	Data input/output
13	DB4	Data input/output
14	DB5	Data input/output
15	DB6	Data input/output
16	DB7	Data input/output (MSB)
-	A	Anode of LED backlight
-	K	Cathode of LED backlight

4.2 Typical Electrical Characteristics at Ta = +25 ºC, V_{DD} = +5V±5%, V_{SS} = 0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic & LCD)	V_{DD} -Vss		4.75	5.0	5.25	V
Supply voltage (LCD)	V_{DD} -V_0	V_{DD} = 5V, Note 2.	-	TBD	-	V
Input signal voltage (Note 1)	V_{IH}	"H" level	2.0	-	V_{DD}	V
	V_{IL}	"L" level	0	-	0.8	V
Supply current (Logic & LCD)	I_{DD}	V_{DD} = 5V	-	TBD	-	mA
Supply current (LCD)	I_0	Note 2	-	TBD	-	mA

Note (1):
Applies to /CSA, /CSB, E, R/W, D/I, DB0~DB7.

Note (2):
There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

4.3 Timing Specifications

At Ta = -20 °C To +70 °C , V_{DD} = +5V±5%, V_{SS} = 0V.

Refer to Fig. 3 & 4, the bus timing diagram.

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
E cycle time	t_C	1000	-	-	ns
E High Level Width	P_{WH}	450	-	-	ns
E Low Level Width	P_{WL}	450	-	-	ns
E Rise Time	t_R	-	-	25	ns
E Fall Time	t_F	-	-	25	ns
Address Setup Time	t_{ASU}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Setup Time	t_{DSU}	200	-	-	ns
Data Delay Time	t_D	-	-	320	ns
Data Hold Time (Write)	t_{DHW}	10	-	-	ns
Data Hold Time (Read)	t_{DHR}	20	-	-	ns

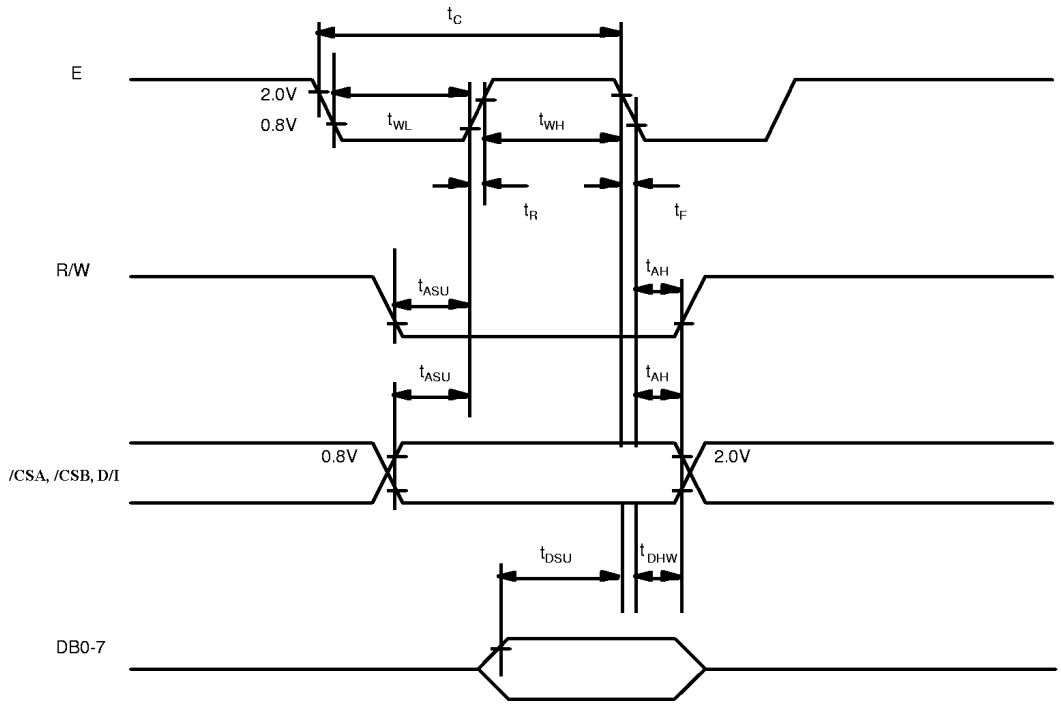


Figure 3 : MPU Write Timing.

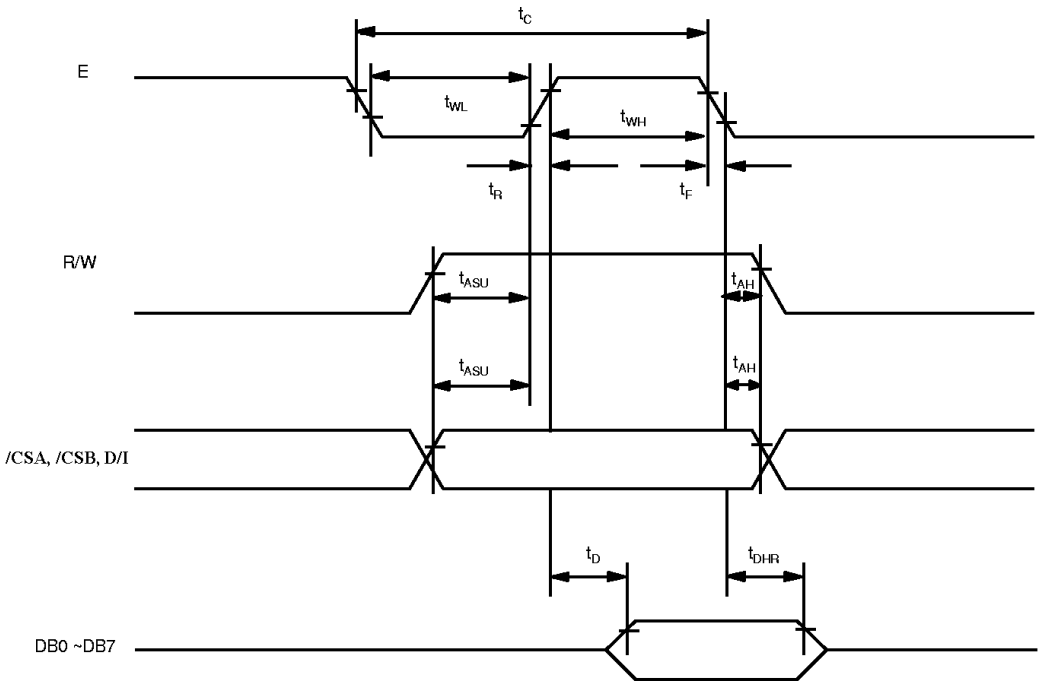


Figure 4 : MPU Read Timing.

4.4 Timing Diagram of V_{DD} against Vo.

Power on sequence shall meet the requirement of Figure 5, the timing diagram of VDD against Vo.

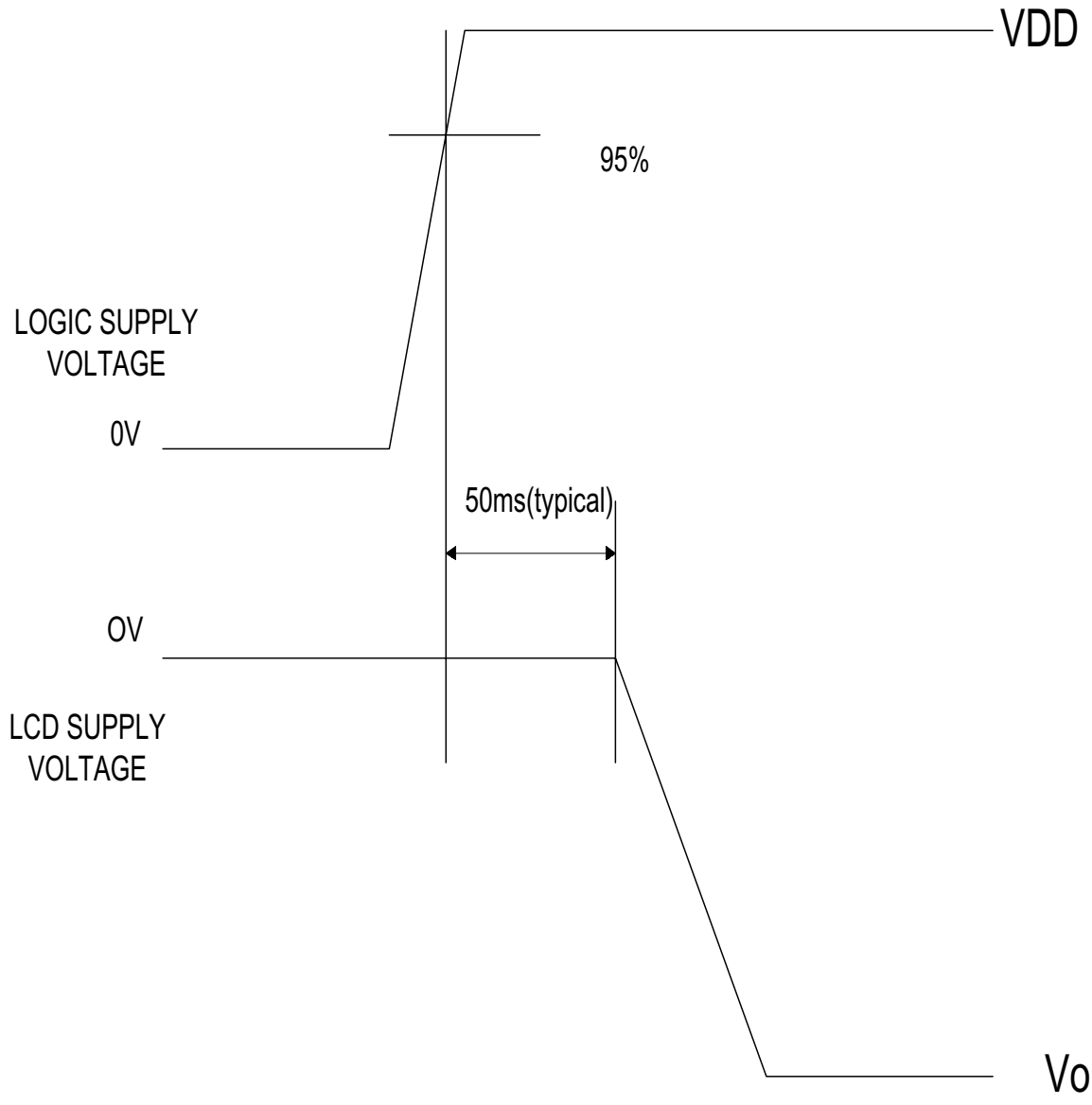


Figure 5: Timing diagram of VDD against Vo.

PRELIMINARY SPECIFICATION

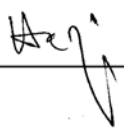
FOR

LCD MODULE TYPE

ITEM NO.: MGLS12864-37

MGLS12864-RH (LCD: C_VGS_12864_16)

(DOC. REVISION 0.0)

DEPARTMENT	NAME	SIGNATURE	EFFECTIVE DATE
PREPARED BY	PHILIP CHENG		2000.11.13
APPROVED BY	K.P.HO		2000.11.13

DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
0.0 0.0	2000.11.13		PHILIP CHENG	K.P.HO

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   4.3 TIMING SPECIFICATIONS.....…….....

   4.4 TIMING DIAGRAM OF V_{DD} VS. THE V_O……..

Preliminary Specification
for
LCD Module Type
Item No.: MGLS12864-37
MGLS12864-RH (LCD: C_VGS_12864_16)

1. General Description

- 128 x 64 dot matrix STN HT positive yellow-green reflective dot matrix LCD graphic module.
- Driving scheme: 1/64 multiplexed drive, 1/9 bias.
- Viewing direction : 6 o'clock.
- 'HITACHI' HD61202UFS flat pack or equivalent LCD column driver.
- 'HITACHI' HD61203UFS flat pack or equivalent LCD row driver.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	78.0(W) x 70.0(H) x 10.0max(D)	mm
Viewing area	62.0(W) x 44.0(H)	mm
Active area	56.27(W) x 38.35(H)	mm
Display format	128(Horizontal) x 64(Vertical)	dots
Dot size	0.39(W) x 0.55(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.44(W) x 0.60(H)	mm
Weight	TBD	gram

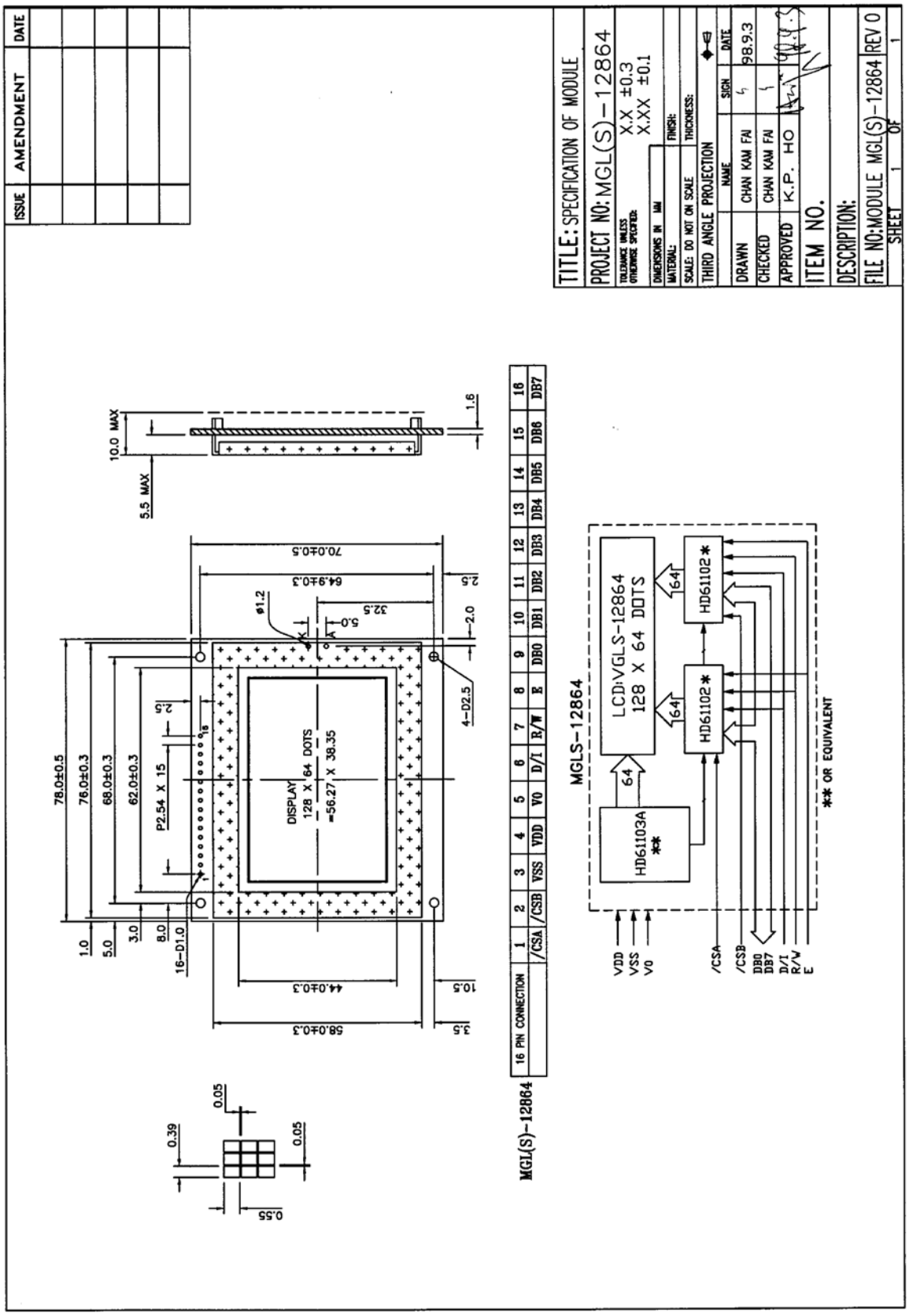

Figure 1: Specification of MGLS12864-RH (LCD: C_VGS_12864_16) MODULE.

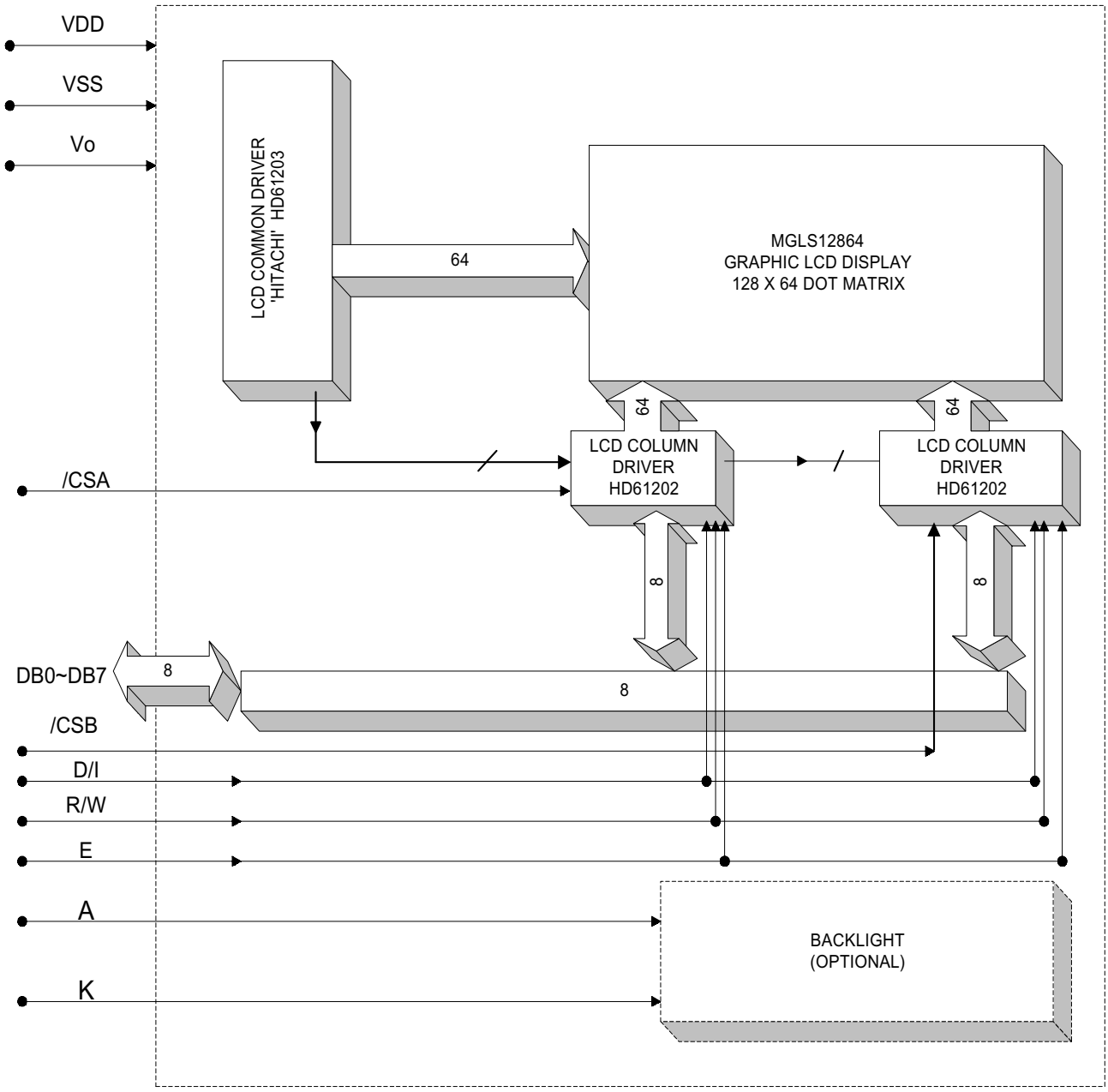

Figure 2: Block diagram

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings (Ta = 25 °C)

Table2

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (Logic)	V_{DD} - Vss	-0.3	+7.0	V
Supply voltage (LCD drive)	V_{DD} - Vo	-0.3	+17.0	V
Input voltage	Vin	-0.3	V_{DD}+0.3	V

Note: The modules may be destroyed if they are used beyond the absolute maximum ratings.
All voltage values are referenced to Vss = 0V.

3.2 Environmental Conditions

Table3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	Note 1		Note 1		no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Note 2		Note 2		3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Note 3		Note 3		3 directions

Note 1: 95% max. RH for Ta ≤ 40°C
< 95% RH for Ta > 40°C

Note 2: Frequency: 10 ~ 55 Hz
Amplitude: 0.75 mm
Duration: 20 cycles in each direction.

Note 3: Pulse duration: 11 ms
Peak acceleration: 981 m/s^2 = 100g
Number of shocks: 3 shocks in 3 mutually perpendicular axes.

4. Electrical Specifications

4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	/CSA	Chip selection for the first column driver
2	/CSB	Chip selection for the second column driver
3	Vss	Ground
4	V_{DD}	Power supply for logic & LCD (+5V)
5	Vo	Power supply for LCD drive
6	D/I	Data/Instruction. "High" for display data and "Low" for display control data.
7	R/W	Read/Write. "High" for MPU to read data appearing at DB0 to DB7 and "Low" for DB0 to DB7 be accepting at fall of E.
8	E	Chip Enable. At read(R/W = High): Data appears at DB0 to DB7 while E is at high level. At write(R/W = Low): Data of DB0 to DB7 is latched at the fall of E.
9	DB0	Data input/output (LSB)
10	DB1	Data input/output
11	DB2	Data input/output
12	DB3	Data input/output
13	DB4	Data input/output
14	DB5	Data input/output
15	DB6	Data input/output
16	DB7	Data input/output (MSB)
-	A	Anode of LED backlight (optional)
.-	K	Cathode of LED backlight (optional).

4.2 Electrical characteristics at Ta = 25 °C, V_{DD} = 5V±5%, Vss=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic & LCD)	V_{DD} -Vss		4.75	5.00	5.25	V
Supply voltage (LCD)	V_{DD} -V_0	V_{DD} = 5V, Note 1.	-	TBD	-	V
Input signal voltage	V_{IH}	"H" level, Note 2.	2.0	-	V_{DD}	V
	V_{IL}	"L" level, Note 2.	0	-	0.8	V
Supply current (Logic & LCD)	I_{DD}	V_{DD} = 5V, Note 1.	-	TBD	-	mA
Supply current (LCD)	I_0	Note 1	-	TBD	-	mA

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.
Note (2): Applies to /CSA, /CSB, E, R/W, D/I, and DB0 ~ DB7.

4.3 Timing Specifications

At Ta = -20 °C to +70 °C , V_{DD} = 5V±5%, Vss = 0V.

Refer to Fig. 3 & 4 , the bus timing diagram .

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
E cycle time	t_{cyc}	1000	-	-	ns
E High Level Width	twh_E	450	-	-	ns
E Low Level Width	twI_E	450	-	-	ns
E Rise Time	tr	-	-	25	ns
E Fall Time	tf	-	-	25	ns
Address Setup Time	t_{as}	140	-	-	ns
Address Hold Time	t_{ah}	10	-	-	ns
Data Setup Time	tdsw	200	-	-	ns
Data Delay Time	tddr	-	-	320	ns
Data Hold Time (Write)	tdhw	10	-	-	ns
Data Hold Time (Read)	tdhr	20	-	-	ns

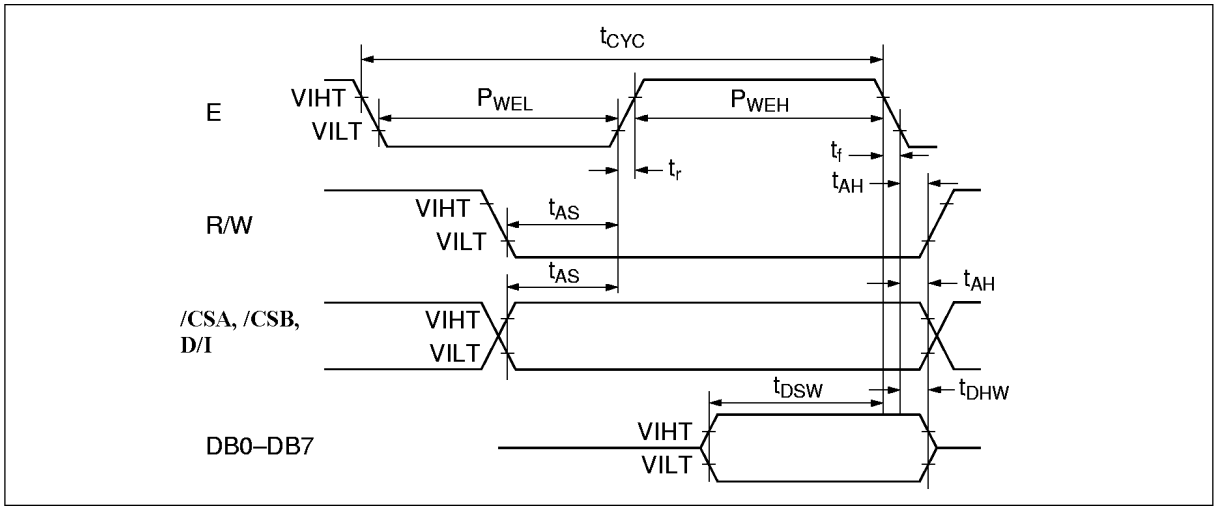

Figure 3: MPU Write Timing.

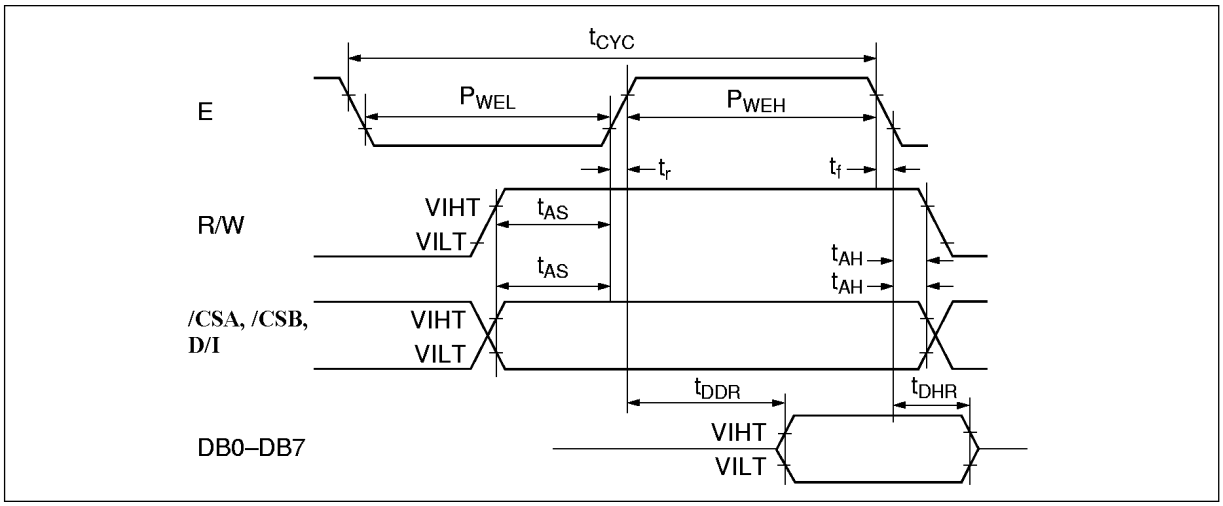

Figure 4: MPU Read Timing.

4.4 Timing Diagram of V_{DD} against Vo.

Power on sequence shall meet the requirement of Figure 5, the timing diagram of VDD against Vo.

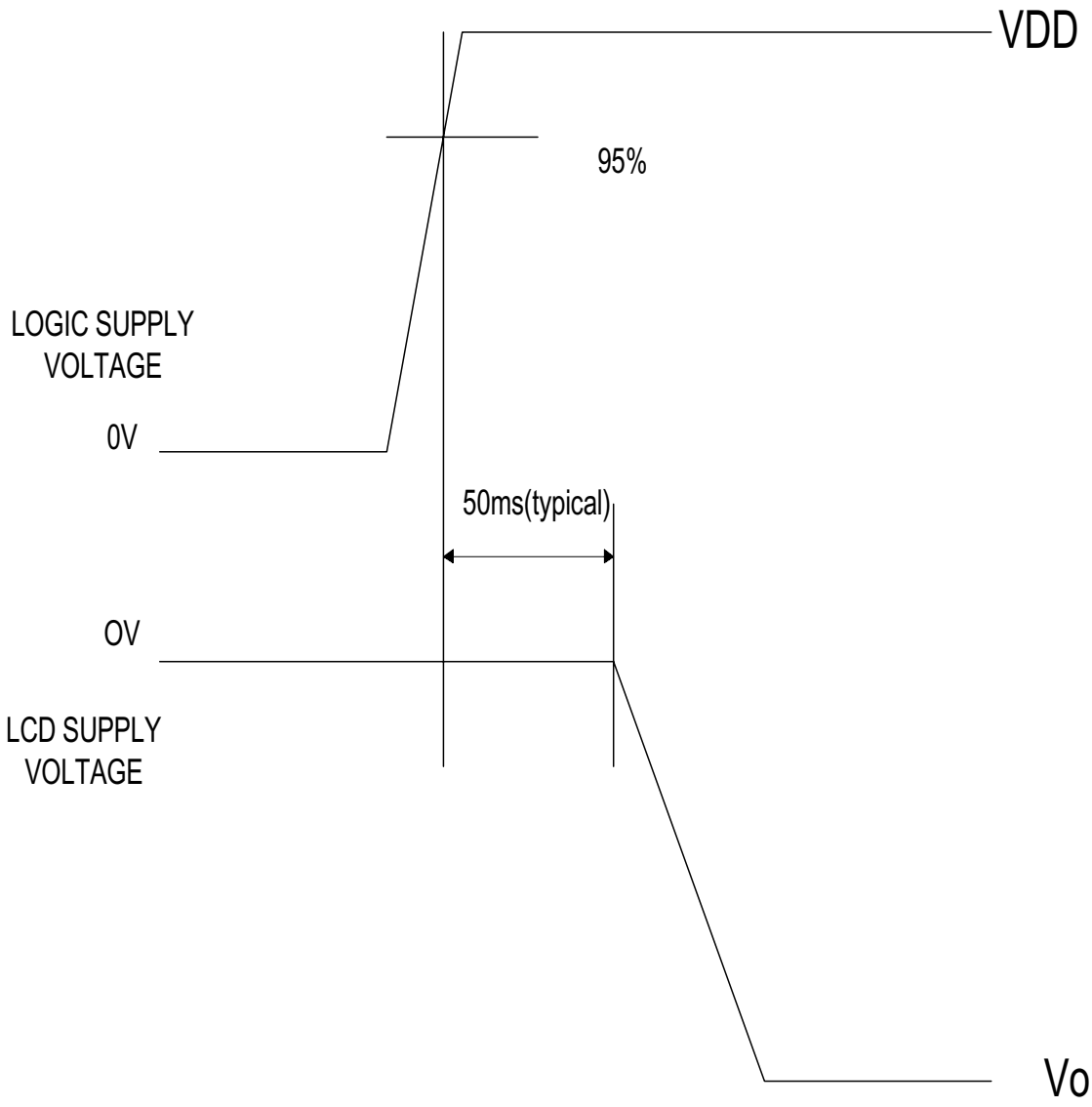

Figure 5: Timing diagram of VDD against Vo.

PRELIMINARY SPECIFICATION

FOR

LCD MODULE TYPE

ITEM NO.: MGLS12864D-01

MGLS12864D-LED03-LV2

(DOC. REVISION 0.0)

DEPARTMENT	NAME	SIGNATURE	EFFECTIVE DATE
PREPARED BY	PHILIP CHENG		2000.11.14
APPROVED BY	K.P.HO		2000.11.14

DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM	TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
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4. ELECTRICAL SPECIFICATIONS .....

   4.1 INTERFACE SIGNALS .....

   4.2 ELECTRICAL CHARACTERISTICS AT Ta=25°C, V_{DD}=5V±5% & Vss = 0V.....

   4.3 TIMING SPECIFICATIONS.....…….....

   4.4 TIMING DIAGRAM OF V_{DD} VS. THE V_O……..

Preliminary Specification
for
LCD Module Type
Item No.: MGLS12864D-01
MGLS12864D-LED03-LV2

1. General Description

- 128 x 64 dot matrix STN LV2 positive green-yellow transflective dot matrix LCD graphic module.
- Driving scheme: 1/64 multiplexed drive, 1/9 bias.
- Viewing direction : 6 o'clock.
- 'HITACHI' HD61202U (Die form) or equivalent LCD column driver.
- 'HITACHI' HD61203U (Die form) or equivalent LCD row driver.
- Yellow-green LED03 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1A and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	78.0(W) x 70.0(H) x 13.0max(D)	mm
Viewing area	62.0(W) x 44.0(H)	mm
Active area	56.27(W) x 38.35(H)	mm
Display format	128(Horizontal) x 64(Vertical)	dots
Dot size	0.39(W) x 0.55(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.44(W) x 0.60(H)	mm
Weight	TBD	grams

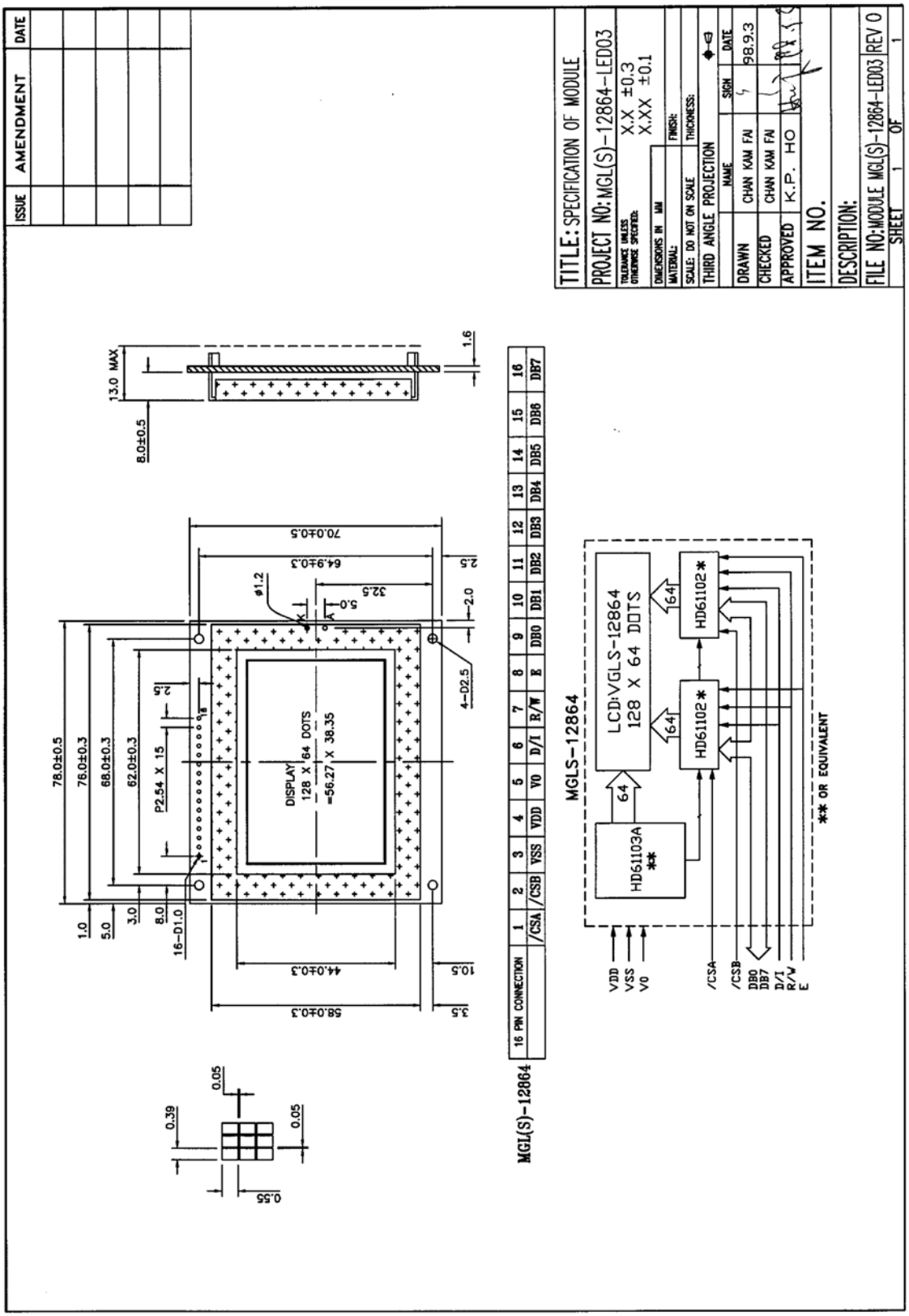

FIG 1(A): Specification of MGLS12864D-LED03-LV2 MODULE.

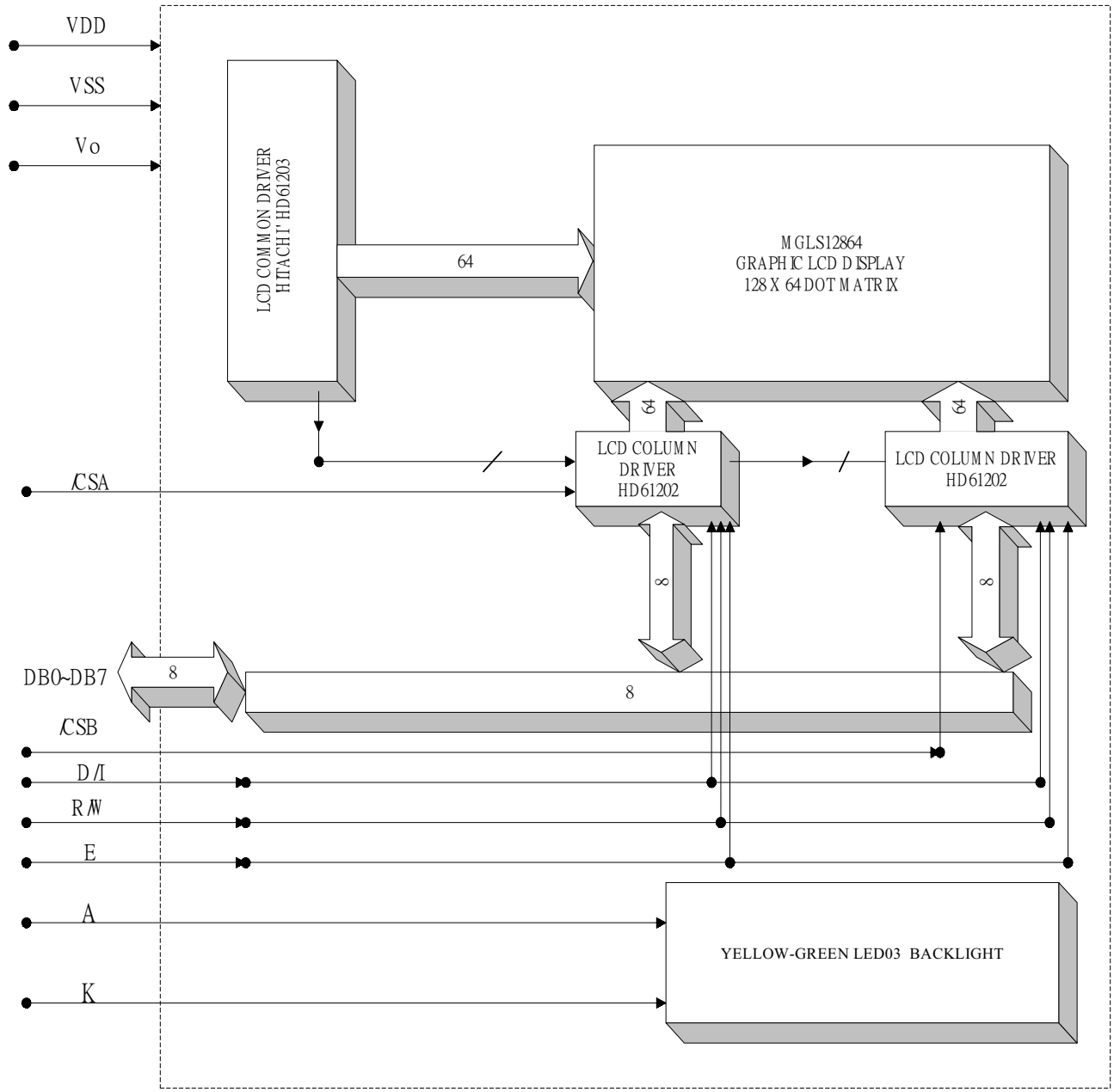

FIG. 1(B): Block diagram of MGLS12864D-LED03-LV2 MODULE.

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings (Ta = 25 °C)

Table2

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (Logic)	V_{DD} - Vss	0	6.0	V
Supply voltage (LCD drive)	V_{DD} - Vo	0	17.0	V
Input voltage	Vin	0	V_{DD}	V

Note: The modules may be destroyed if they are used beyond the absolute maximum ratings.
All voltage values are referenced to Vss = 0V.

3.2 Environmental Conditions

Table3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	Note 1		Note 1		no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Note 2		Note 2		3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Note 3		Note 3		3 directions

Note 1: 95% max. RH for Ta ≤ 40°C
< 95% RH for Ta > 40°C

Note 2: Frequency: 10 ~ 55 Hz
Amplitude: 0.75 mm
Duration: 20 cycles in each direction.

Note 3: Pulse duration: 11 ms
Peak acceleration: 981 m/s^2 = 100g
Number of shocks: 3 shocks in 3 mutually perpendicular axes.

4. Electrical Specifications

4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	/CSA	Chip selection for the first column driver
2	/CSB	Chip selection for the second column driver
3	Vss	Ground
4	V_{DD}	Power supply for logic & LCD (+5V)
5	Vo	Power supply for LCD drive
6	D/I	Data/Instruction. "High" for display data and "Low" for display control data.
7	R/W	Read/Write. "High" for CPU to read data appearing at DB0 to DB7 and "Low" for DB0 to DB7 be accepting at fall of E.
8	E	Chip Enable. At read(R/W = High): Data appears at DB0 to DB7 while E is at high level. At write(R/W = Low): Data of DB0 to DB7 is latched at the fall of E.
9	DB0	Data input/output (LSB)
10	DB1	Data input/output
11	DB2	Data input/output
12	DB3	Data input/output
13	DB4	Data input/output
14	DB5	Data input/output
15	DB6	Data input/output
16	DB7	Data input/output (MSB)
-	A	Anode of LED backlight.
.-	K	Cathode of LED backlight.

4.2 Electrical characteristics at Ta = 25 °C, V_{DD} = 5V±5%, Vss=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic & LCD)	V_{DD} -Vss		4.75	5.00	5.25	V
Supply voltage (LCD)	V_{DD} -V_0	V_{DD} = 5V, Note 1.	-	TBD	-	V
Input signal voltage	V_{IH}	"H" level, Note 2.	2.0	-	V_{DD}	V
	V_{IL}	"L" level, Note 2.	0	-	0.8	V
Supply current (Logic & LCD)	I_{DD}	V_{DD} = 5V, Note 1.	-	TBD	-	mA
Supply current (LCD)	I_0	Note 1	-	TBD	-	mA
Supply voltage (LED03 backlight)	V_{LED03}	Forward current =10x10=100mA Number of LED chips=2x10=20.	3.8	4.1	4.5	V

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Note (2): Applies to /CSA, /CSB, E, R/W, D/I, and DB0 ~ DB7.

4.3 Timing Specifications

At Ta = 0 °C to 50 °C , V_{DD} = 5V±5%, Vss = 0V.

Refer to Fig. 2 & 3 , the bus timing diagram .

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
E cycle time	t_{cyc}	1000	-	-	ns
E High Level Width	twh_E	450	-	-	ns
E Low Level Width	twI_E	450	-	-	ns
E Rise Time	tr	-	-	25	ns
E Fall Time	tf	-	-	25	ns
Address Setup Time	t_{as}	140	-	-	ns
Address Hold Time	t_{ah}	10	-	-	ns
Data Setup Time	tdsw	200	-	-	ns
Data Delay Time	tddr	-	-	320	ns
Data Hold Time (Write)	tdhw	10	-	-	ns
Data Hold Time (Read)	tdhr	20	-	-	ns

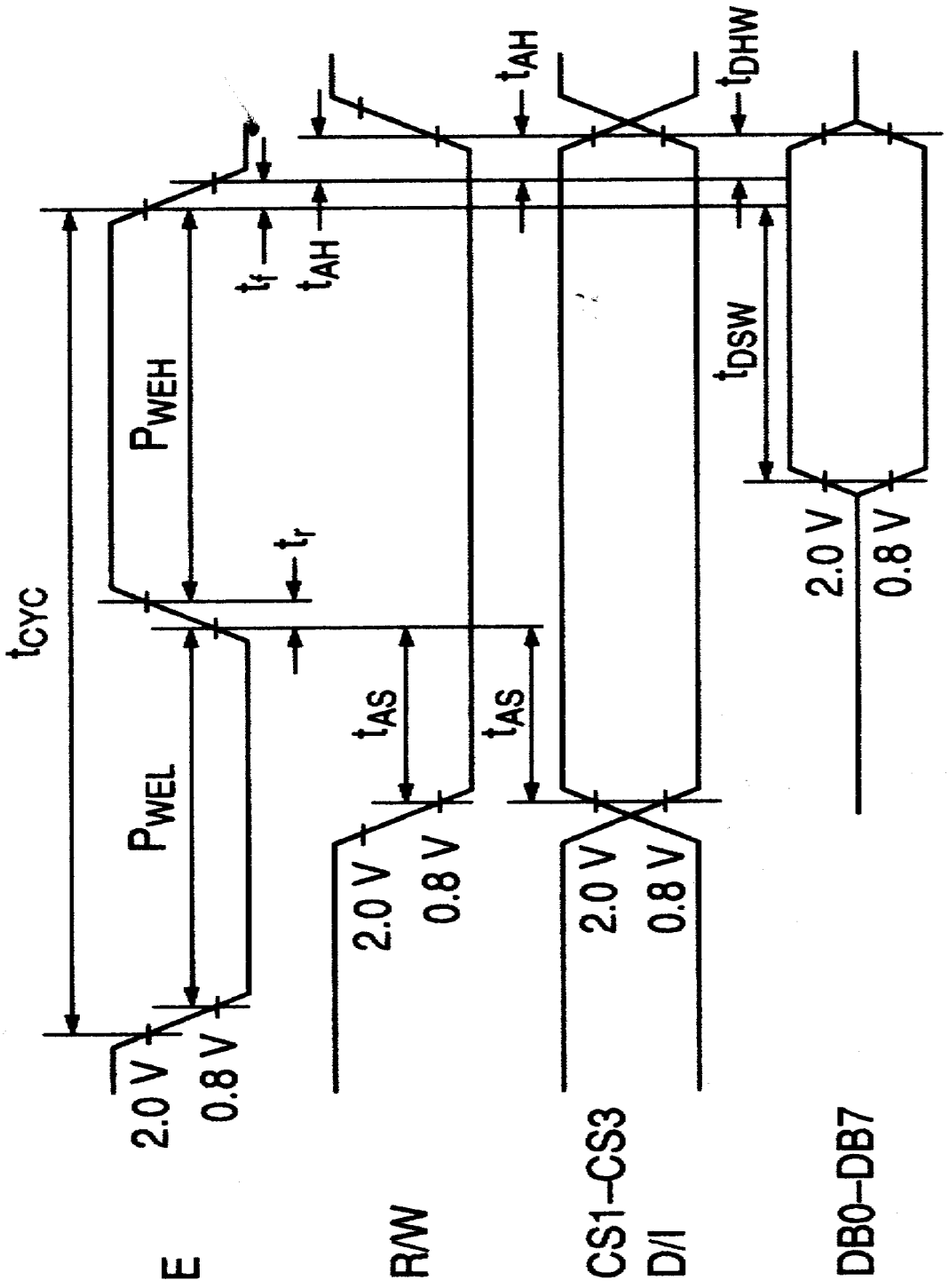

Fig. 2 CPU Write Timing.

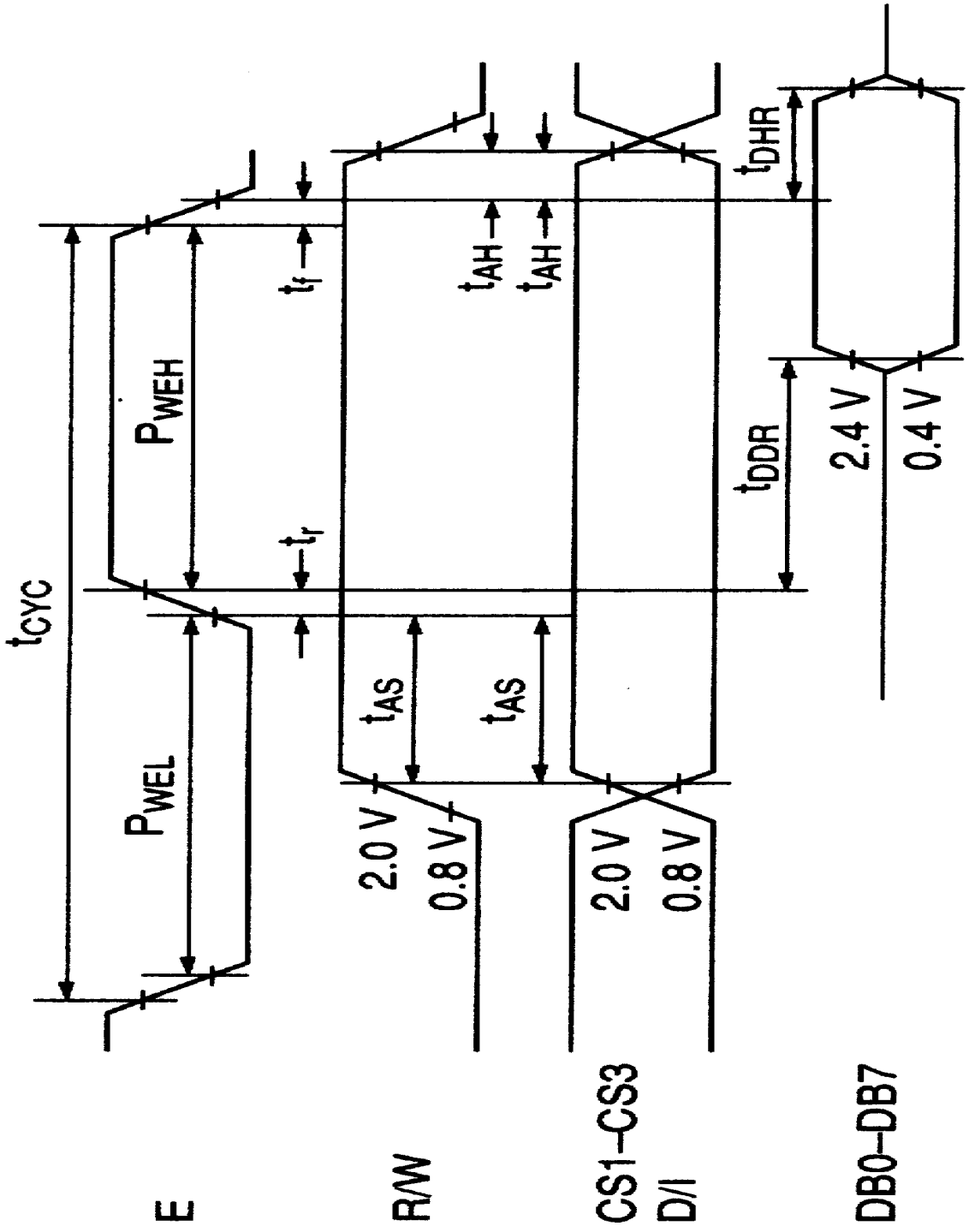

Fig. 3 CPU Read Timing.

4.4 Timing Diagram of V_{DD} against Vo.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against Vo.

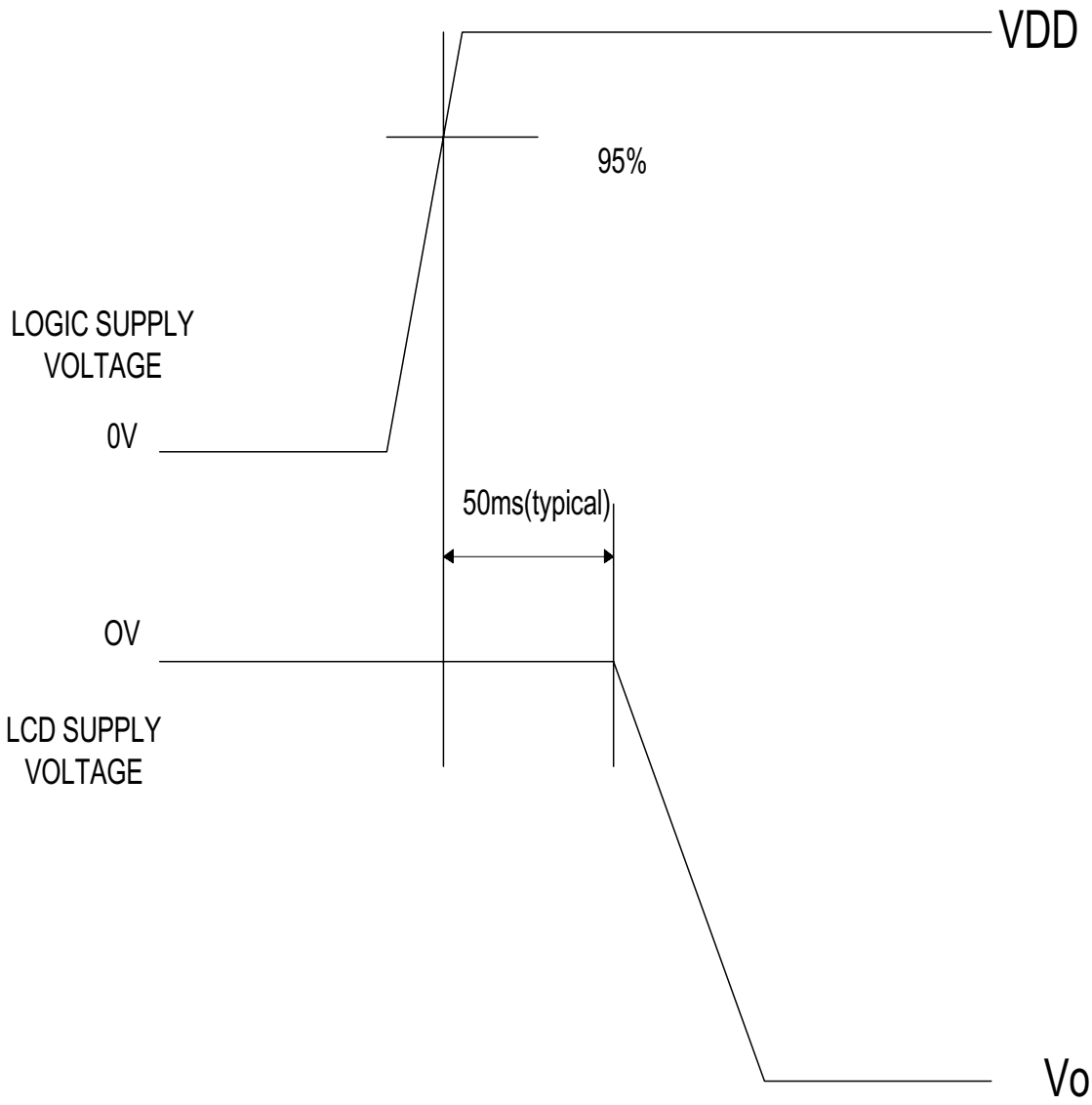

Figure 4: Timing diagram of VDD against Vo.

PRELIMINARY SPECIFICATION

FOR

LCD MODULE TYPE

ITEM NO.: MGLS12864T-04

MGLS12864T-RC-STD2

(DOC. REVISION 0.0)

DEPARTMENT	NAME	SIGNATURE	EFFECTIVE DATE
PREPARED BY	PHILIP CHENG		2000.11.13
APPROVED BY	K.P.HO		2000.11.13

DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
0.0	2000.11.13		PHILIP CHENG	MR. HO

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Preliminary Specification
for
LCD Module Type
Item No.: MGLS12864T-04
MGLS12864T-RC-STD2

1. General Description

- 128 x 64 dot matrix STN STD2 positive green-yellow reflective dot matrix LCD graphic module.
- Viewing direction: 6 o'clock.
- Driving scheme: 1/64 multiplexed drive, 1/9 bias.
- 'Toshiba' T6963C flat pack or equivalent dot matrix LCD controller.
- 'Toshiba' T6A39 flat pack or equivalent dot matrix liquid crystal graphic display column driver.
- 'Toshiba' T6A40 flat pack or equivalent dot matrix liquid crystal graphic display row driver.
- 8K byte display SRAM.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

. Table 1

Parameter	Specifications	Unit
Outline dimensions	78.0(W) x 70.0(H) x 10.0 MAX.(D)	mm
Viewing area	62.0(W) x 44.0(H)	mm
Active area	56.27(W) x 38.35(H)	mm
Display format	128(Horizontal) x 64(Vertical)	dots
Dot size	0.39(W) x 0.55(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.44(W) x 0.60(H)	mm
Weight	TBD	gram

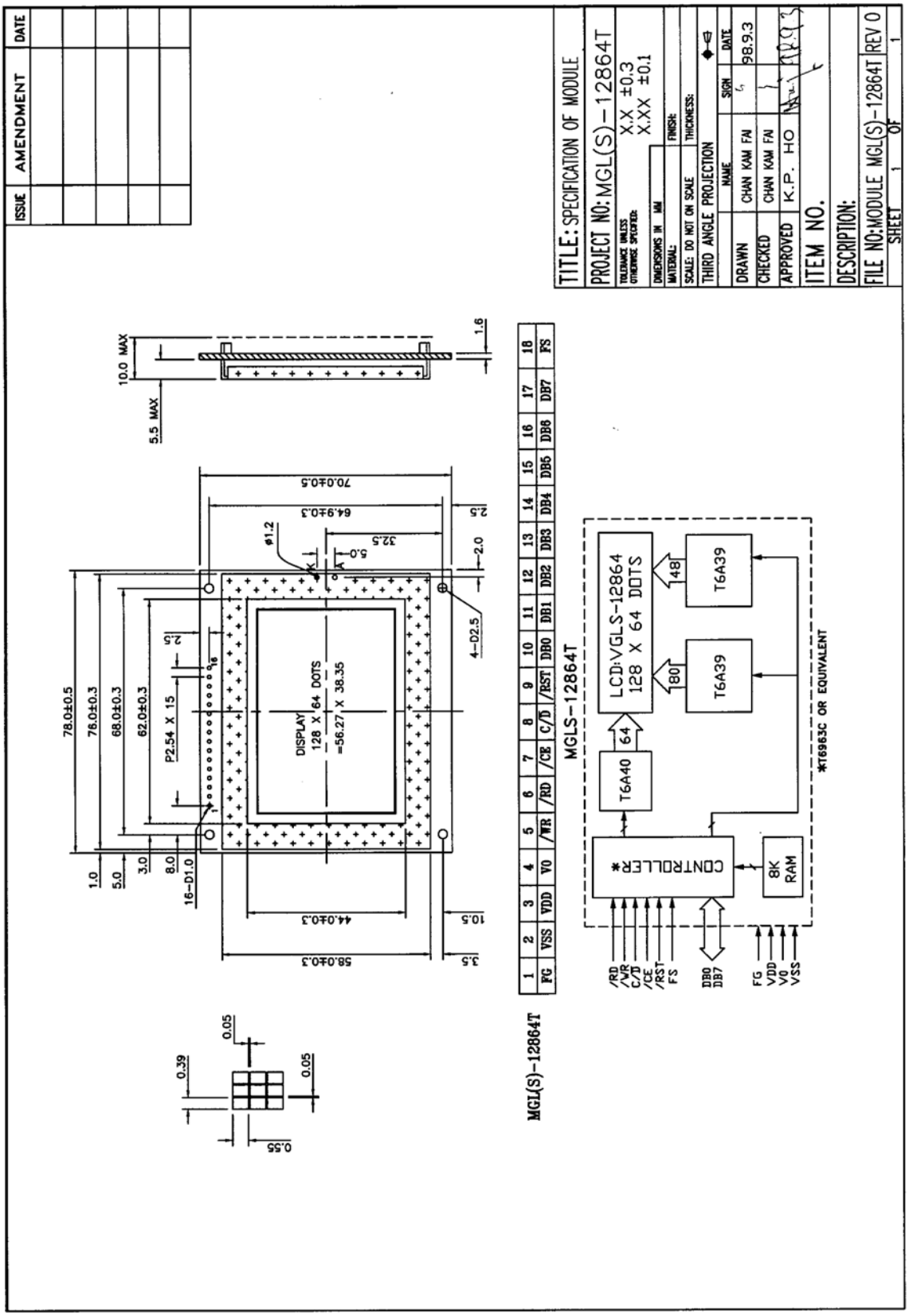

FIG. 1: Outline drawing

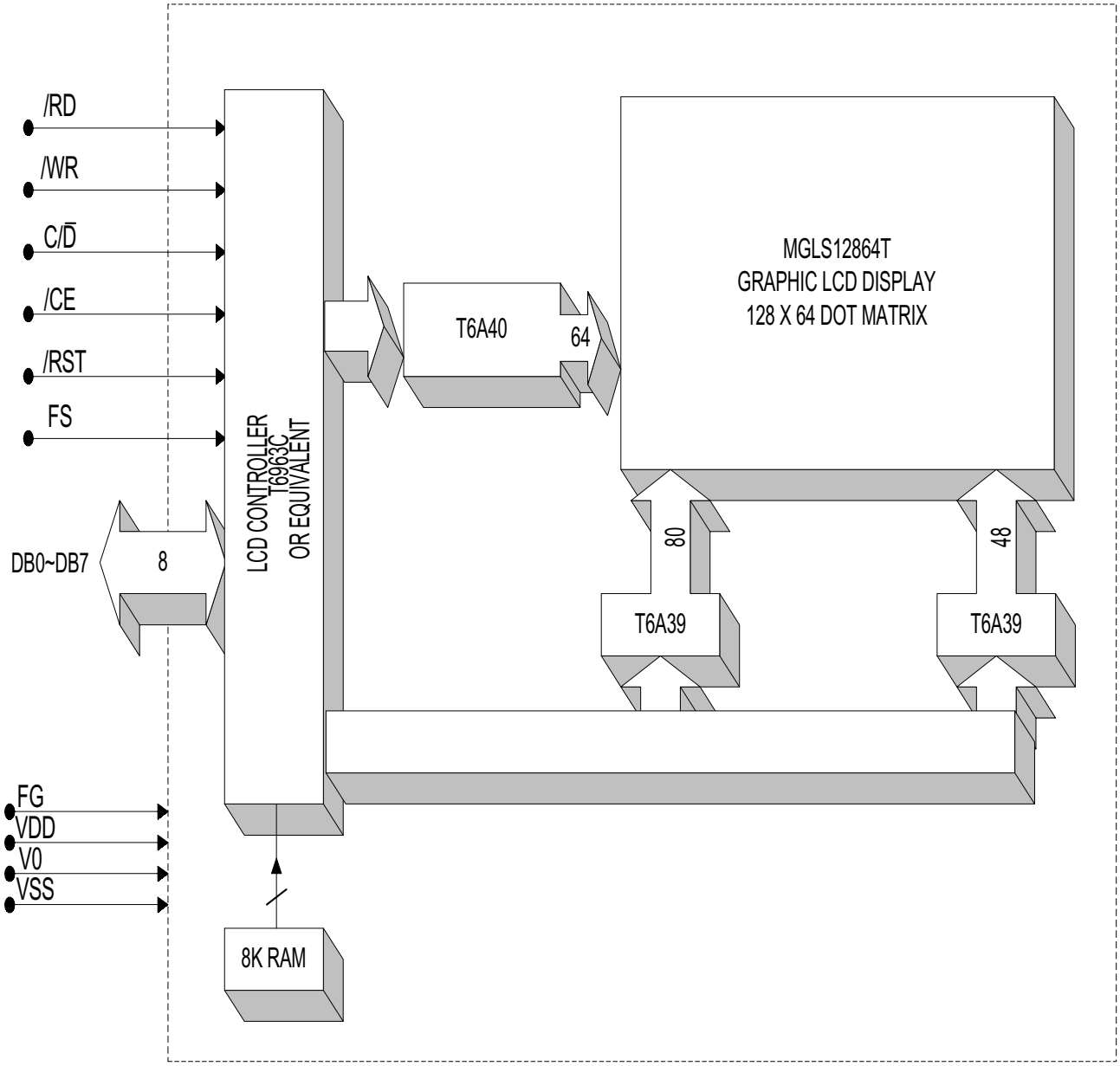

FIG. 2: Block diagram

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings (Ta = 25 °C)

Table2

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (Logic & LCD)	V_{DD} - Vss	-0.3	+7.0	V
Supply voltage (LCD drive)	V_{DD} - Vo	-0.3	+28.0	V
Input voltage	Vin	-0.3	V_{DD} +3.0	V

Note: The modules may be destroyed if they are used beyond the absolute maximum ratings.
All voltage values are referenced to Vss = 0V.

3.2 Environmental Condition

Table3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	Note 1		Note 1		no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Note 2		Note 2		3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Note 3		Note 3		3 directions

Note 1: 95% max. RH for Ta ≤ 40°C
< 95% RH for Ta > 40°C

Note 2: Frequency: 10 ~ 55 Hz
Amplitude: 0.75 mm
Duration: 20 cycles in each direction.

Note 3: Pulse duration: 11 ms
Peak acceleration: 981 m/s^2 = 100g
Number of shocks: 3 shocks in 3 mutually perpendicular axes.

4. Electrical Specifications

4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	FG	Frame ground (see note 1)
2	V_{SS}	Ground (0V)
3	V_{DD}	Power supply for logic (+5V)
4	Vo	Power supply for LCD drive
5	/WR	Command/Data write to module when “Low”
6	/RD	Command/Data read from module when “Low”
7	/CE	Chip enable of controller when “Low”
8	$\overline{C / D}$	Command/Data read/write. ”High” for command read/write and ”Low” for data read/write
9	/RST	Controller reset when “Low”
10	DB0	Data input/output (LSB)
11	DB1	Data input/output
12	DB2	Data input/output
13	DB3	Data input/output
14	DB4	Data input/output
15	DB5	Data input/output
16	DB6	Data input/output
17	DB7	Data input/output (MSB)
18	FS	Font select. “High” for 6 x 8 font & “Low” for 8 x 8 font.
-	K	Cathode of backlight
-	A	Anode of backlight

Note 1: This pin is electrically connected to the metal bezel (frame).
User can choose to connect this pin to V_{SS} or leave it open.

4.2 Typical Electrical Characteristics at Ta = +25 °C, V_{DD} = +5V±5%, Vss=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic & LCD)	V_{DD} -Vss		4.75	5.00	5.25	V
Supply voltage (LCD)	V_{DD} -V_0	V_{DD} = 5V, Note 1	-	TBD	-	V
Input signal voltage	V_{IH}	"H" level	V_{DD}-2.2	-	V_{DD}	V
	V_{IL}	"L" level	0	-	0.8	V
Supply current (Logic & LCD)	I_{DD}	V_{DD} = 5V, Checker board mode	-	TBD	-	mA
Supply current (LCD)	I_0	Checker board mode	-	TBD	-	mA

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

4.3 Timing Specifications

At Ta = 0 °C to +50 °C, V_{DD} = 5V±5%, V_{SS}=0V.

Refer to Fig. 3, the bus timing diagram.

Table 6

Parameter	Symbol	Min.	Max.	Unit
C/D Set-up time	t_{CDS}	100	-	ns
C/D Hold Time	t_{CDH}	10	-	ns
/CE,/RD,/WR Pulse Width	t_{CE}, t_{RD}, t_{WR}	80	-	ns
Data Set-up Time	t_{DS}	80	-	ns
Data Hold Time	t_{DH}	40	-	ns
Access Time	t_{ACC}	-	150	ns
Output Hold Time	t_{OH}	10	50	ns

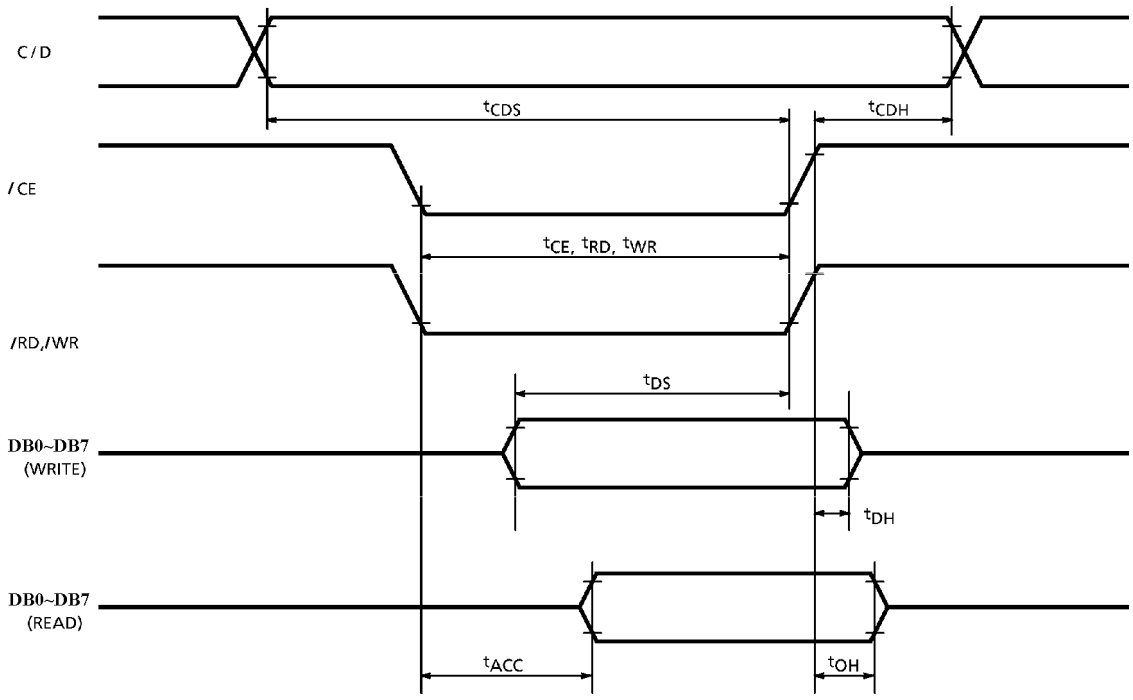

Figure 3: Bus Timing Diagram

4.4 Timing Diagram of V_{DD} against Vo.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against Vo.

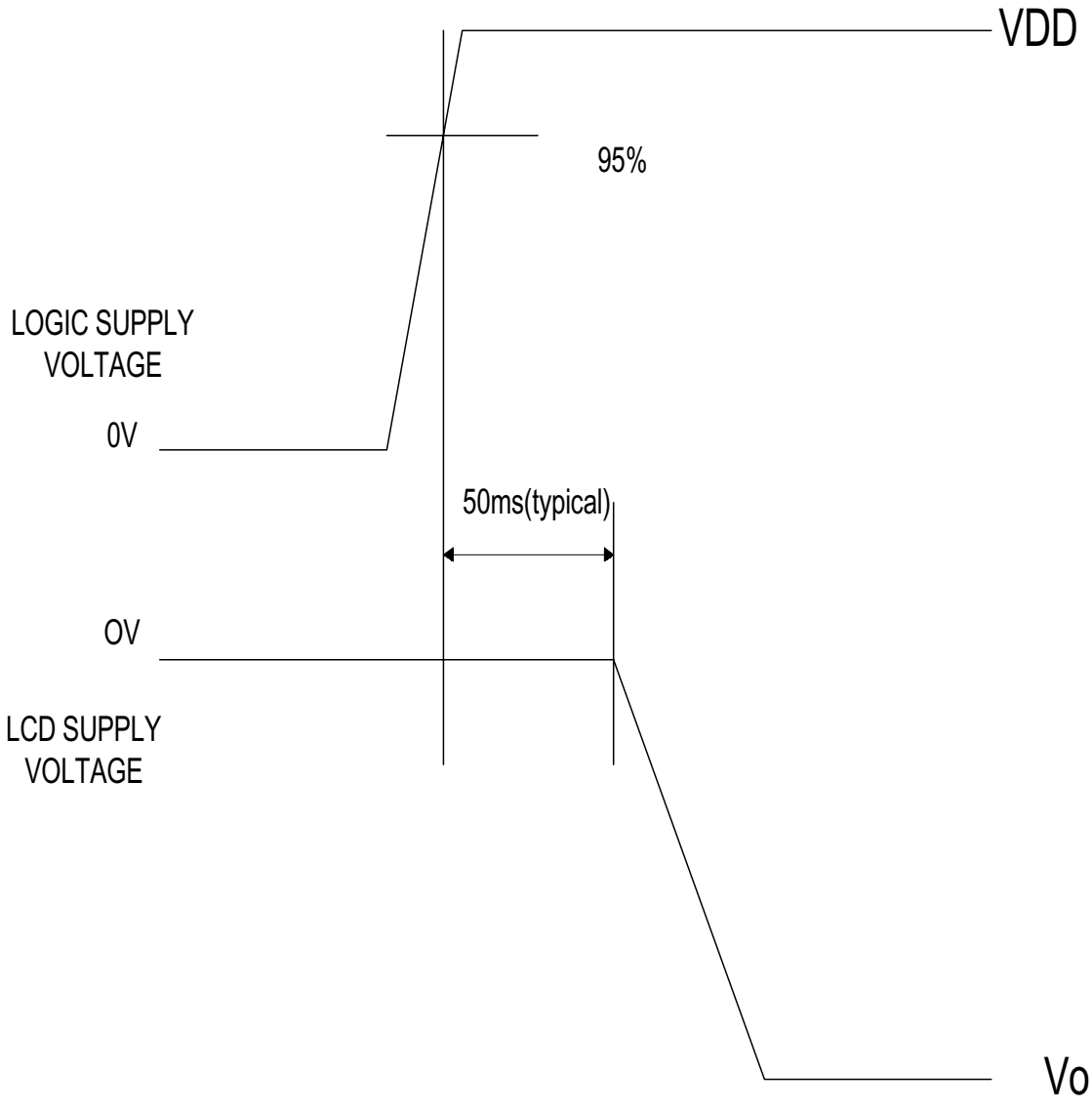

Figure 4: Timing diagram of VDD against Vo.