

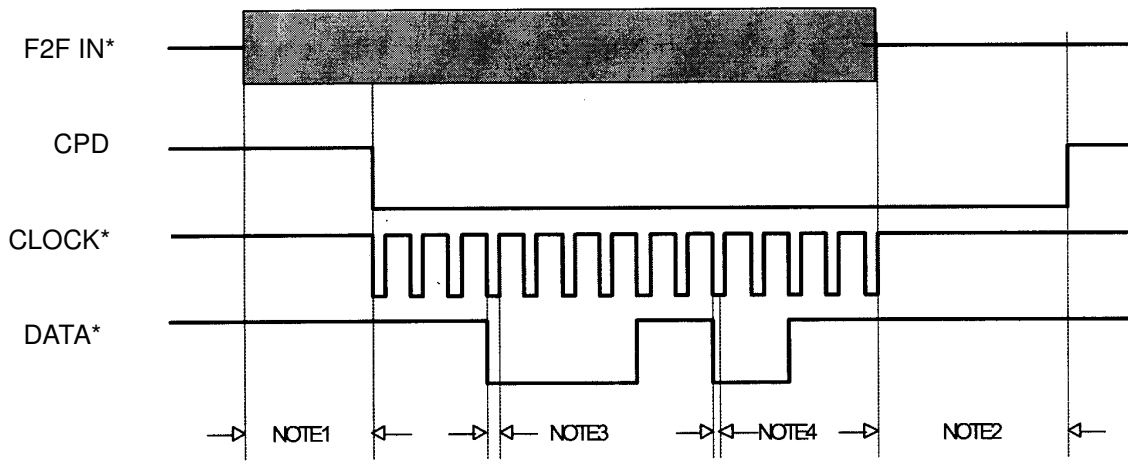


TITLE		Application Description for DigiHeads		PAGE																																																						
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MODEL		AP-I2 Series		DWG NO./ VER. JY0-62-001-SS / A																																																						
<p>1. This document is applicable to AP-I2 DigiHead Series, including all DigiHead models, in which F2F decoder chip IC2 are adopted.</p> <p>2. Terminal description</p> <table border="1"> <tr> <th>Terminal symbol</th> <th>Description</th> <th>Remarks</th> </tr> <tr> <td>V<sub>DD</sub></td> <td>Analog positive power supply</td> <td></td> </tr> <tr> <td>V<sub>SS</sub></td> <td>Analog negative power supply</td> <td></td> </tr> <tr> <td>CPD</td> <td>Card Present Detect</td> <td></td> </tr> <tr> <td>DATA*</td> <td>Track* read data</td> <td></td> </tr> <tr> <td>CLOCK*</td> <td>Track* read clock pulse</td> <td></td> </tr> </table> <p>Note: In this document, “*” represents for each track, for exsample CLOCK* means CLOCK-A, CLOCK-B or CLOCK-C for different tracks.</p> <p>3. Absolute maximum ratings (Non operating)</p> <table border="1"> <tr> <th>Parameter</th> <th>Symbol</th> <th>Min</th> <th>Max</th> <th>Note</th> </tr> <tr> <td>DC supply voltage</td> <td>V<sub>DD</sub></td> <td>-0.5V</td> <td>7.0V</td> <td></td> </tr> <tr> <td>Storage temperature</td> <td>T<sub>S</sub></td> <td>-25℃</td> <td>75℃</td> <td></td> </tr> <tr> <td>Lead temperature</td> <td>T<sub>L</sub></td> <td></td> <td>260℃</td> <td></td> </tr> <tr> <td>Lead time</td> <td></td> <td></td> <td>6 sec</td> <td></td> </tr> <tr> <td>Humidity</td> <td></td> <td>10%</td> <td>95%</td> <td></td> </tr> <tr> <td>Electronic discharge</td> <td></td> <td>±2000V</td> <td></td> <td>(1)</td> </tr> </table> <p>(1) Human body mode (MIL-STD-883C Method 3015.7)</p>						Terminal symbol	Description	Remarks	V <sub>DD</sub>	Analog positive power supply		V <sub>SS</sub>	Analog negative power supply		CPD	Card Present Detect		DATA*	Track* read data		CLOCK*	Track* read clock pulse		Parameter	Symbol	Min	Max	Note	DC supply voltage	V <sub>DD</sub>	-0.5V	7.0V		Storage temperature	T <sub>S</sub>	-25℃	75℃		Lead temperature	T <sub>L</sub>		260℃		Lead time			6 sec		Humidity		10%	95%		Electronic discharge		±2000V		(1)
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6. Signal timing diagram



△ CPD

CPD goes low after the 16 (17) flux reversals (default). CPD returns to high level approximately 50ms after CLOCK\*'s last transition.

△ CLOCK\*

CLOCK\* signal indicates DATA\*'s output is valid. The DATA\* output should be loaded for further use when the CLOCK\* signal goes low. (Negative edge)

△ DATA\*

DATA\* signal is valid when the CLOCK\* is low. If the DATA\* signal is high, the bit is zero (0). If the DATA\* signal is low, the bit is one (1).

Note:


(1) Programmable CPD delay for 16 or 8 flux reversals on request.

(2) Time out of CPD signal occurs approx. 50ms (Clock=2.5Mz) after last flux transition.

(3) Active duty cycle time is approx. 50% bit time (default). It is selectable as 25%, 50% or 75% bit time on request.

(4) The DATA\* is valid at 3.2μS (min) before the negative edge of the CLOCK\*.

(END)

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