THC63LVDM83R/THC63LVDM63R

REDUCED SWING LVDS 24Bit/18Bit COLOR HOST-LCD PANEL INTERFACE

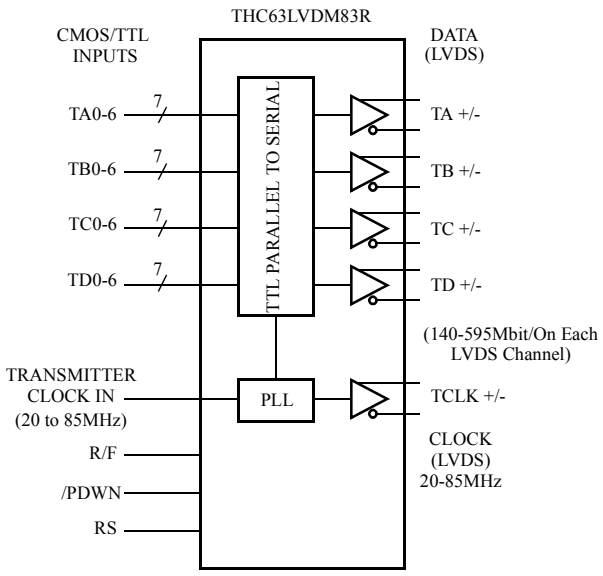
General Description

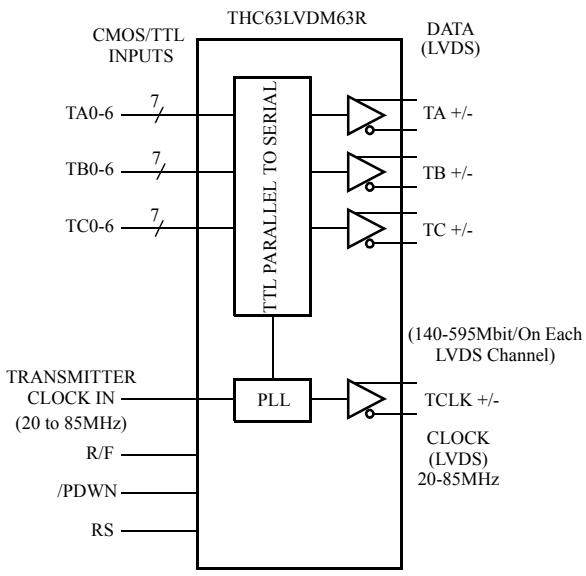
The THC63LVDM83R transmitter converts 28bits of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. At a transmit clock frequency of 85MHz, 28bits of RGB data and 4bits of LCD timing and control data (HSYNC, VSYNC, CNTL1, CNTL2) are transmitted at a rate of 595Mbps per LVDS channel. Also available is THC63LVDM63R that converts 21bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. Both transmitters can be programmed reduced swing LVDS through a dedicated pin for low power consumption and EMI.

Features

- 28:4 Data channel compression at up to 298 Megabytes per sec throughput
- Wide dot clock range: 20-85MHz suited for VGA, SVGA, XGA and SXGA
- Narrow bus (10 lines or 8 lines) reduces cable size
- Support Reduced swing LVDS for Low EMI
- 200mV swing LVDS/350mV swing LVDS selectable
- Support Spread Spectrum Clock Generator
- On chip Input Jitter Filtering
- PLL requires No external components
- Single 3.3V supply with 125mW(TYP)
- Power-Down Mode
- Low profile 56 or 48 Lead TSSOP Package
- Clock Edge Programmable
- Improved Replacement for the National DS90C383 or DS90C363

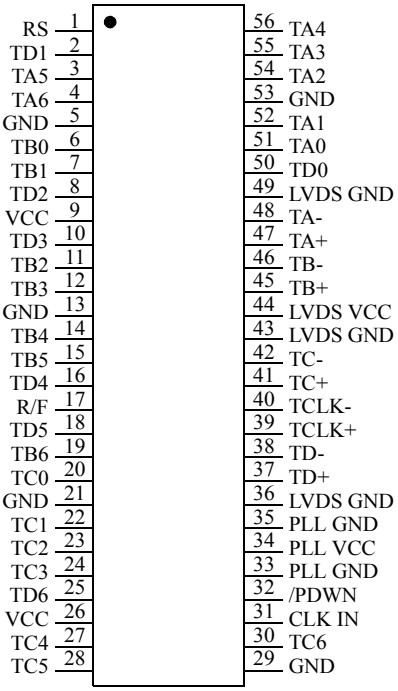
Block Diagram



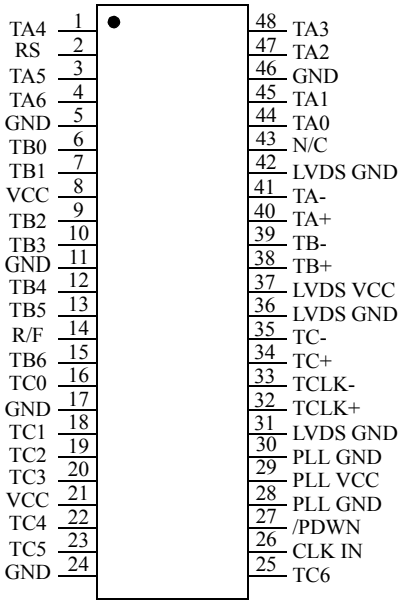


Pin Out

THC63LVDM83R



THC63LVDM63R



THC63LVDM83R Pin Description

Pin Name	Pin #	Type	Description
TA+, TA-	47, 48	LVDS OUT	LVDS Data Out.
TB+, TB-	45, 46	LVDS OUT	
TC+, TC-	41, 42	LVDS OUT	
TD+, TD-	37, 38	LVDS OUT	
TCLK+, TCLK-	39, 40	LVDS OUT	LVDS Clock Out.
TA0 ~ TA6	51, 52, 54, 55, 56, 3, 4	IN	Pixel Data Inputs.
TB0 ~ TB6	6, 7, 11, 12, 14, 15, 19	IN	
TC0 ~ TC6	20, 22, 23, 24, 27, 28, 30	IN	
TD0 ~ TD6	50, 2, 8, 10, 16, 18, 25	IN	
/PDWN	32	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)
RS	1	IN	LVDS swing control. RS: VCC → 350mV; : → :; GND → 200mV
R/F	17	IN	Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge
VCC	9, 26	Power	Power Supply Pins for TTL inputs and digital circuitry.
CLKIN	31	IN	Clock in.
GND	5, 13, 21, 29, 53	Ground	Ground Pins for TTL inputs and digital circuitry.
LVDS VCC	44	Power	Power Supply Pins for LVDS Outputs.
LVDS GND	36, 43, 49	Ground	Ground Pins for LVDS Outputs.
PLL VCC	34	Power	Power Supply Pin for PLL circuitry.
PLL GND	33, 35	Ground	Ground Pins for PLL circuitry.

THC63LVDM63R Pin Description

Pin Name	Pin #	Type	Description
TA+, TA-	40, 41	LVDS OUT	LVDS Data Out.
TB+, TB-	38, 39	LVDS OUT	
TC+, TC-	34, 35	LVDS OUT	
TCLK+, TCLK-	32, 33	LVDS OUT	LVDS Clock Out.
TA0 ~ TA6	44, 45, 47, 48, 1, 3, 4	IN	Pixel Data Inputs.
TB0 ~ TB6	6, 7, 9, 10, 12, 13, 15	IN	
TC0 ~ TC6	16, 18, 19, 20, 22, 23, 25	IN	
/PDWN	27	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)
RS	2	IN	LVDS swing control. RS: VCC → 350mV; : → :; GND → 200mV

Pin Name	Pin #	Type	Description
R/F	14	IN	Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge
VCC	8, 21	Power	Power Supply Pins for TTL inputs and digital circuitry.
CLKIN	26	IN	Clock in.
GND	5, 11, 17, 24, 46	Ground	Ground Pins for TTL inputs and digital circuitry.
LVDS VCC	37	Power	Power Supply Pins for LVDS Outputs.
LVDS GND	36, 42	Ground	Ground Pins for LVDS Outputs.
PLL VCC	29	Power	Power Supply Pin for PLL circuitry.
PLL GND	28, 30	Ground	Ground Pins for PLL circuitry.

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Driver Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	continuous
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +150°C
Resistance to soldering heat	+260°C /10sec
Maximum Power Dissipation @+25°C	0.5W

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$			±10	μA
I_{PD}	Pull Down Current	R/F pin, VIH=V_{CC}			100	μA
I_{RS}	RS Pull Down Current	RS pin, VIH=V_{CC}			100	μA

1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

LVDS Transmitter DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS=V_{CC}	250	350	450	mV
			Reduced swing RS=GND	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	VOUT=0V, RL=100Ω				-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN=0V, V_{OUT}=0V to V_{CC}				±10	μA

THC63LVDM83R Supply Current

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

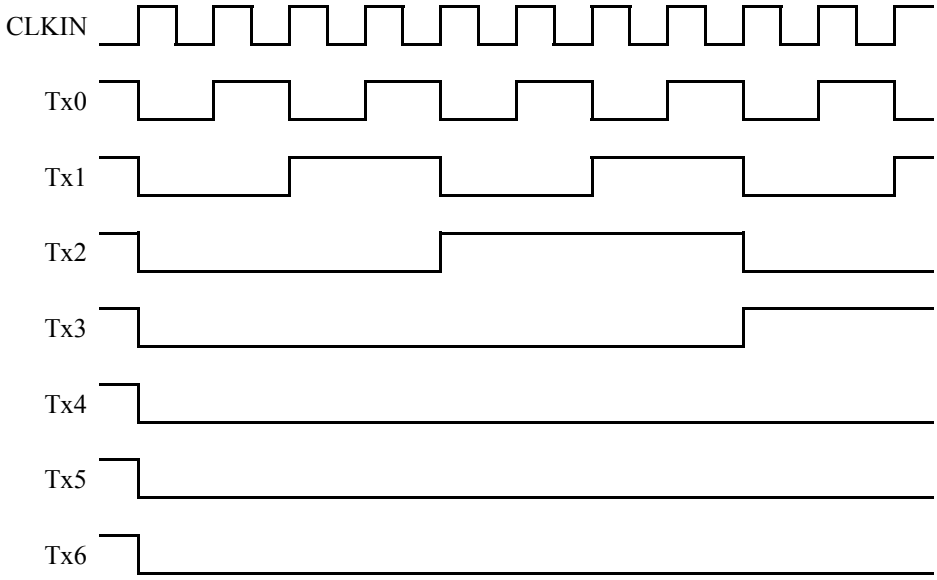
Symbol	Parameter	Condition(*)		Typ.	Max.	Units
I_{TCCG}	Transmitter Supply Current	RL=100Ω,CL=5pF V_{CC}=3.3V, RS=V_{CC} 16 Gray Scale Pattern	f=65MHz	36	46	mA
			f=85MHz	39	49	mA
		RL=100Ω,CL=5pF V_{CC}=3.3V, RS=GND 16 Gray Scale Pattern	f=65MHz	31	41	mA
			f=85MHz	34	44	mA
I_{TCCW}	Transmitter Supply Current	RL=100Ω,CL=5pF V_{CC}=3.3V, RS=V_{CC} Worst Cace Pattern	f=65MHz	38	48	mA
			f=85MHz	41	51	mA
		RL=100Ω,CL=5pF V_{CC}=3.3V, RS=GND Worst Cace Pattern	f=65MHz	33	43	mA
			f=85MHz	36	46	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L			10	μA

THC63LVDM63R Supply Current

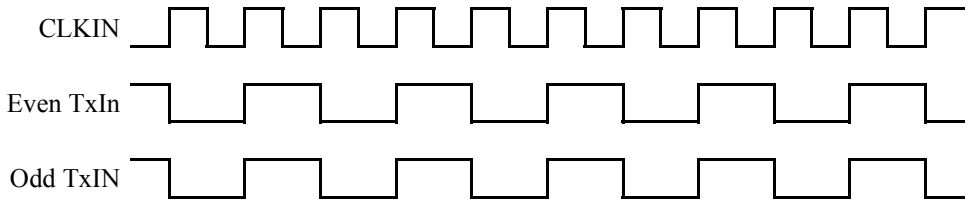
V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Condition(*)		Typ.	Max.	Units
I_{TCCG}	Transmitter Supply Current	RL=100Ω,CL=5pF V_{CC}=3.3V, RS=V_{CC} 16 Gray Scale Pattern	f=65MHz	33	41	mA
			f=85MHz	37	45	mA
		RL=100Ω,CL=5pF V_{CC}=3.3V, RS=GND 16 Gray Scale Pattern	f=65MHz	29	36	mA
			f=85MHz	33	39	mA
I_{TCCW}	Transmitter Supply Current	RL=100Ω,CL=5pF V_{CC}=3.3V, RS=V_{CC} Worst Cace Pattern	f=65MHz	35	43	mA
			f=85MHz	39	47	mA
		RL=100Ω,CL=5pF V_{CC}=3.3V, RS=GND Worst Cace Pattern	f=65MHz	31	38	mA
			f=85MHz	35	42	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L			10	µA

16 Gray Scale Pattern



Worst Case Pattern



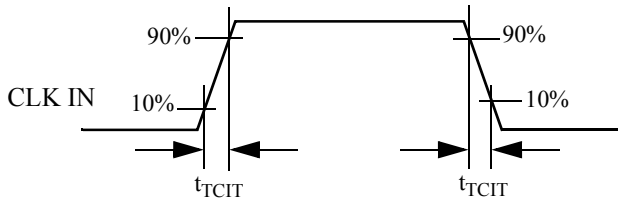
Switching Characteristics

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

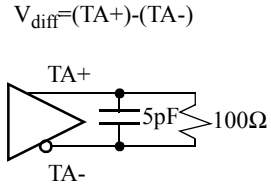
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{TCIT}	CLK IN Transition time			5.0	ns
t_{TCP}	CLK IN Period	11.76	T	50.0	ns
t_{TCH}	CLK IN High Time	0.35T	0.5T	0.65T	ns
t_{TCL}	CLK IN Low Time	0.35T	0.5T	0.65T	ns
t_{TCD}	CLK IN to TCLK+/- Delay		2T/7		ns
t_{TS}	TTL Data Setup to CLK IN	2.5			ns
t_{TH}	TTL Data Hold from CKL IN	2.5			ns
t_{LVT}	LVDS Transition Time		0.6	1.5	ns
t_{TOP1}	Output Data Position0 (T=11.76ns)	-0.2	0.0	+0.2	ns
t_{TOP0}	Output Data Position1 (T=11.76ns)	$\frac{T}{7}-0.2$	$\frac{T}{7}$	$\frac{T}{7}+0.2$	ns
t_{TOP6}	Output Data Position2 (T=11.76ns)	$2\frac{T}{7}-0.2$	$2\frac{T}{7}$	$2\frac{T}{7}+0.2$	ns
t_{TOP5}	Output Data Position3(T=11.76ns)	$3\frac{T}{7}-0.2$	$3\frac{T}{7}$	$3\frac{T}{7}+0.2$	ns
t_{TOP4}	Output Data Position4 (T=11.76ns)	$4\frac{T}{7}-0.2$	$4\frac{T}{7}$	$4\frac{T}{7}+0.2$	ns
t_{TOP3}	Output Data Position5 (T=11.76ns)	$5\frac{T}{7}-0.2$	$5\frac{T}{7}$	$5\frac{T}{7}+0.2$	ns
t_{TOP2}	Output Data Position6 (T=11.76ns)	$6\frac{T}{7}-0.2$	$6\frac{T}{7}$	$6\frac{T}{7}+0.2$	ns
t_{TPLL}	Phase Lock Loop Set			10.0	ms

AC Timing Diagrams

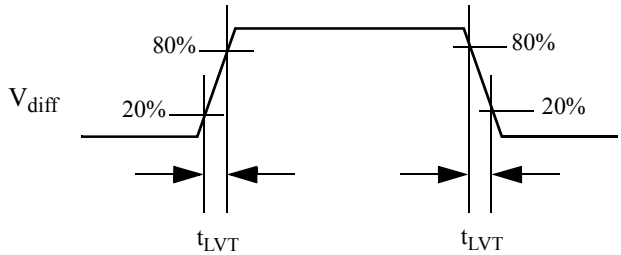
TTL Input



LVDS Output

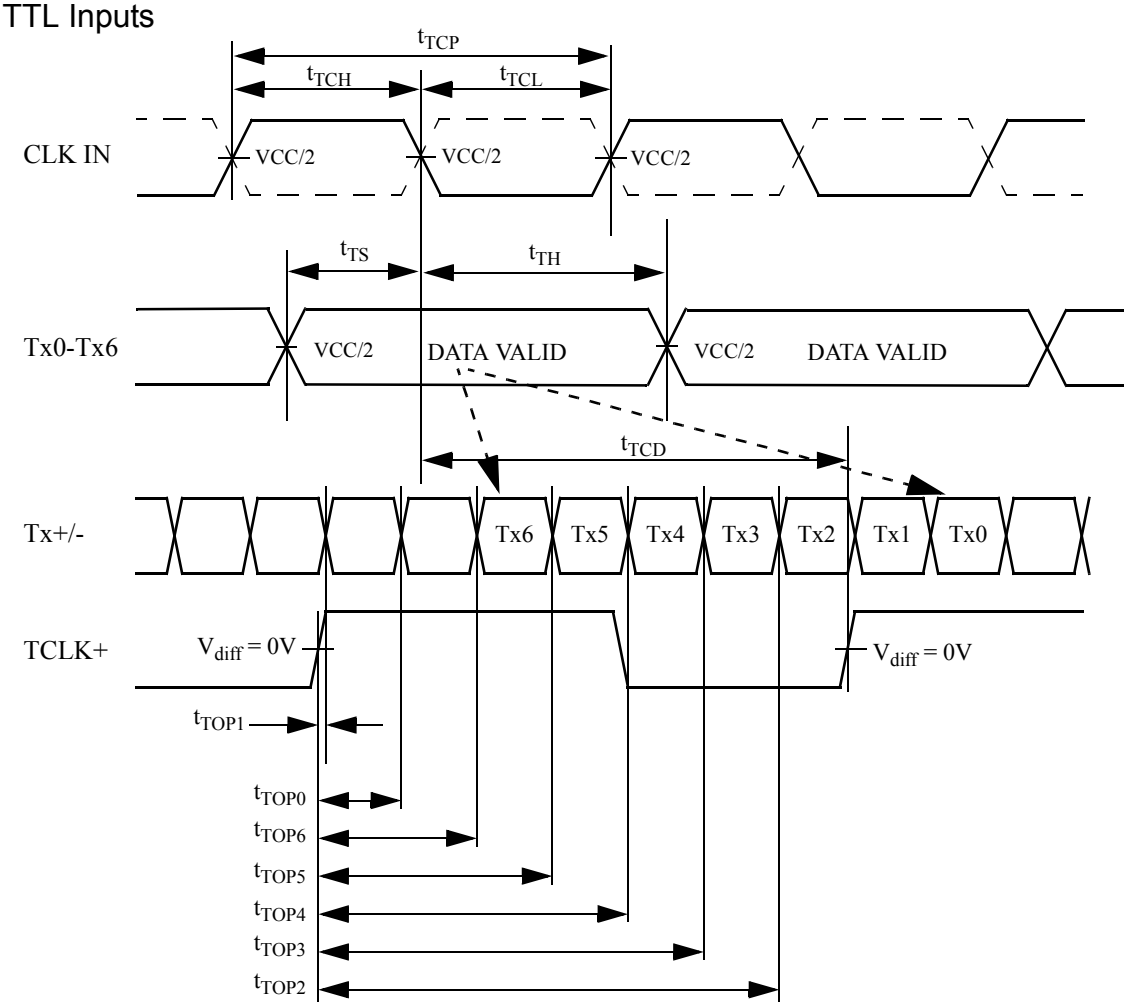


LVDS Output Load



AC Timing Diagrams

TTL Inputs

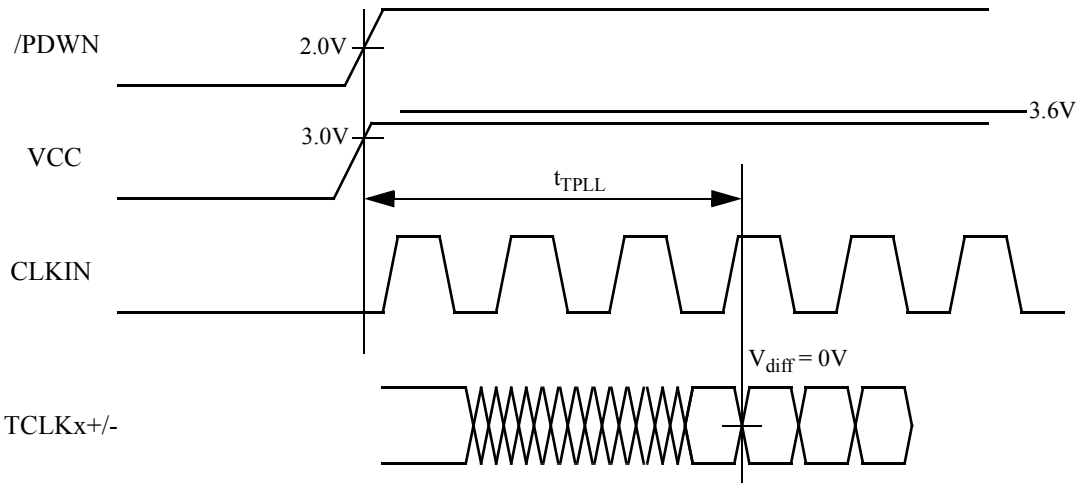


Note:

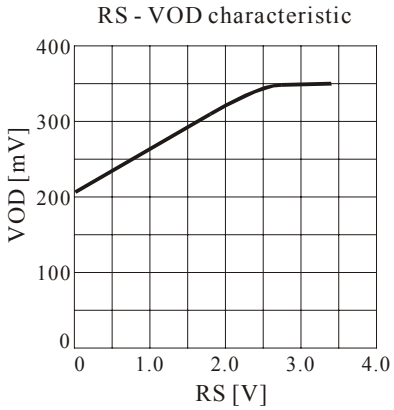
1)CLK IN: for THC63LVDM83R/THC63LVDM63R(R/F=GND), denote as solid line,
for THC63LVDM83R/THC63LVDM63R(R/F=VCC), denote as dashed line

2)V_{diff} = (Tyx+) - (Tyx-) , ---- (TCLKx+) - (TCLKx-)

Phase Lock Loop Set Time

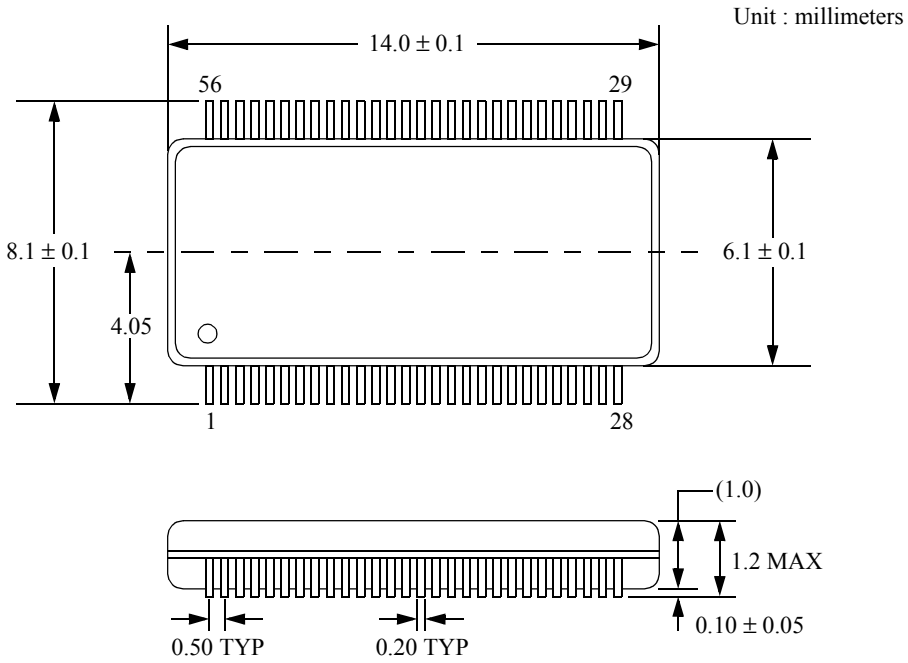


Reduced Swing Characteristic (T_A=25°C, V_{CC}=3.3V, RL=100Ω)

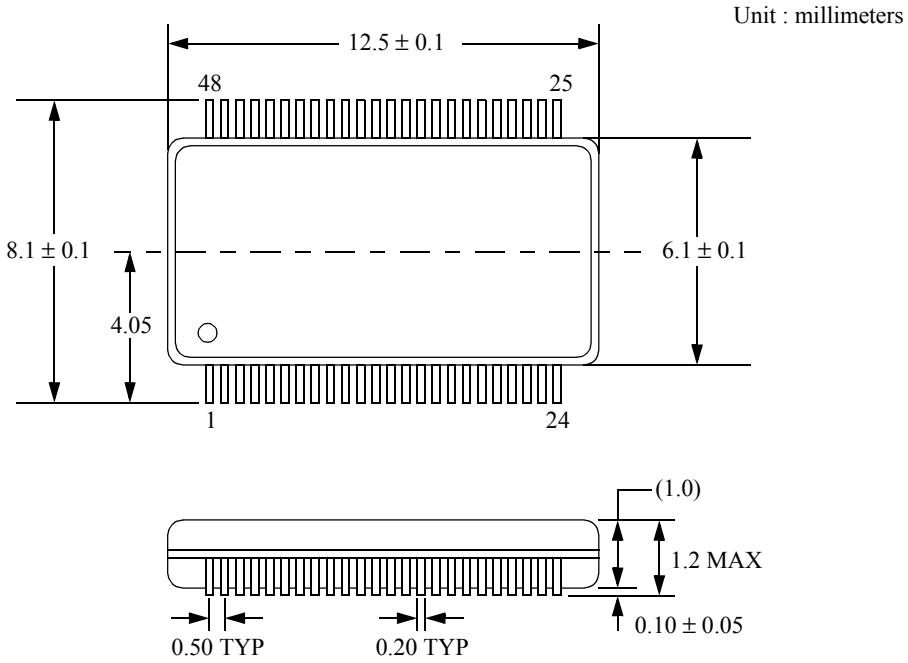


Package

56 Lead Molded Thin Shrink Small Outline Package, JEDEC



48 Lead Molded Thin Shrink Small Outline Package, JEDEC



Notes to Users:

1. The contents of this data sheet are subject to change without prior notice.
2. Circuit diagrams shown in this data sheet are examples of application. Therefore, please pay sufficient attention when designing circuits. Even if there are incorrect descriptions, we are not responsible for any problem due to them. Please note that incorrect descriptions sometimes cannot be corrected immediately if found.
3. Our copyright and know-how are included in this data sheet. Duplication of the data sheet and disclosure to other persons are strictly prohibited without our permission.
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