A GENERAL UNIFIED APPROACH TO MODELLING SWITCHING-CONVERTER POWER STAGES

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ABSTRACT

A method for modelling switching-converter power stages is developed, whose starting point is the unified state-space representation of the switched networks and whose end result is either a complete state-space description or its equivalent small-signal low-frequency linear circuit model.

A new canonical circuit model is proposed, whose fixed topology contains all the essential input-output and control properties of any dc-to-dc switching converter, regardless of its detailed configuration, and by which different converters can be characterized in the form of a table conveniently stored in a computer data bank to provide a useful tool for computer aided design and optimization. The new canonical circuit model predicts that, in general, switching action introduces both zeros and poles into the duty ratio to output transfer function in addition to those from the effective filter network.

1. INTRODUCTION

1.1 Brief Review of Existing Modelling Techniques

In modelling of switching converters in general, and power stages in particular, two main approaches - one based on state-space modelling and the other using an averaging technique - have been developed extensively, but there has been little correlation between them. The first approach remains strictly in the domain of equation manipulations, and hence relies heavily on numerical methods and computerized implementations. Its primary advantage is in the unified description of all power stages regardless of the type (buck, boost, buck-boost or any other variation) through utilization of the exact state-space equations of the two switched models. On the other hand, Processing Systems."

based on equivalent circuit manipulations, resulting in a single equivalent linear circuit model of the power stage. This has the distinct advantage of providing the circuit designer with physical insight into the behaviour of the original switched circuit, and of allowing the powerful tools of linear circuit analysis and synthesis to be used to the fullest extent in design of regulators incorporating switching converters.

1.2 Proposed New State-Space Averaging Approach

The method proposed in this paper bridges the gap earlier considered to exist between the state-space technique and the averaging technique of modelling power stages by introduction of state-space averaged modelling. At the same time it offers the advantages of both existing methods - the general unified treatment of the state-space approach, as well as an equivalent linear circuit model as its final result. Furthermore, it makes certain generalizations possible, which otherwise could not be achieved.

The proposed state-space averaging method, outlined in the Flowchart of Fig. 1, allows a unified treatment of a large variety of power stages currently used, since the averaging step in the state-space domain is very simple and clearly defined (compare blocks 1a and 2a). It merely consists of averaging the two exact state-space descriptions of the switched models over a single cycle T, where $f_s = 1/T$ is the switching frequency (block 2a). Hence there is no need for special "know-how" in massaging the two switched circuit models into topologically equivalent forms in order to apply circuit-oriented procedure directly, as required in [1] (block 1c). Nevertheless, through a hybrid modelling technique (block 2c), the circuit structure of the averaged circuit model (block 2b) can be readily recognized from the averaged state-space model (block 2a). Hence all the benefits of the previous averaging technique are retained. Even though this out- In either case, a perturbation and linearization

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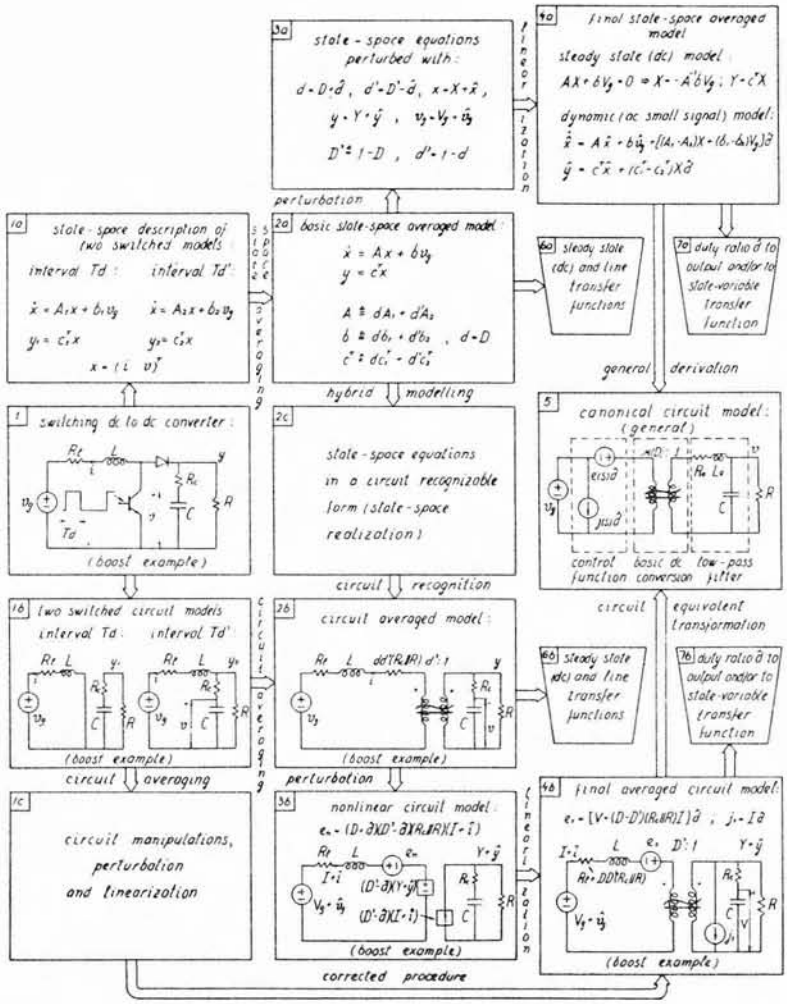

Fig. 1. Flowchart of averaged modelling approaches

process required to include the duty ratio modulation effect proceeds in a very straightforward and formal manner, thus emphasizing the corner-stone character of blocks 2a and 2b. At this stage (block 2a or 2b) the steady-state (dc) and line to output transfer functions are already available, as indicated by blocks 6a and 6b respectively, while the duty ratio to output transfer function is available at the final-stage model (4a or 4b) as indicated by blocks 7a and 7b. The two final stage models (4a and 4b) then give the complete description of the switching converter by inclusion of both independent controls, the line voltage variation and the duty ratio modulation.

Even though the circuit transformation path b might be preferred from the practical design standpoint, the state-space averaging path a is invaluable in reaching some general conclusions about the small-signal low-frequency models of any dc-to-dc switching converter (even those yet to be invented). Whereas, for path b, one has to be presented with the particular circuit in order to proceed with modelling, for path a the final state-space averaged equations (block 4a) give the complete model description through general matrices A_1, A_2 and vectors b_1, b_2, c_1^T, and c_2^T of the two starting switched models (block 1a). This is also why along path b in the Flowchart a particular example of a boost power stage with parasitic effects was chosen, while along path a general equations have been retained. Specifically, for the boost power stage $b_1 = b_2 = b$. This example will be later pursued in detail along both paths.

In addition the state-space averaging approach offers a clear insight into the quantitative nature of the basic averaging approximation, which becomes better the further the effective low-pass filter corner frequency f_c is below the switching frequency f_s, that is, $f_c/f_s \ll 1$. This is, however, shown to be equivalent to the requirement for small output voltage ripple, and hence does not pose any serious restriction or limitation on modelling of practical dc-to-dc converters.

Finally, the state-space averaging approach serves as a basis for derivation of a useful general circuit model that describes the input-output and control properties of any dc-to-dc converter.

1.3 New Canonical Circuit Model

The culmination of any of these derivations along either path a or path b in the Flowchart of Fig. 1 is an equivalent circuit (block 5), valid for small-signal low-frequency variations superimposed upon a dc operating point, that represents the two transfer functions of interest for a switching converter. These are the line voltage to output and duty ratio to output transfer functions.

The equivalent circuit is a canonical model that contains the essential properties of any dc-to-dc switching converter, regardless of the detailed configuration. As seen in block 5 for the general case, the model includes an ideal transformer that describes the basic dc-to-dc transformation ratio from line to output; a low-pass filter whose element values depend upon the dc duty ratio; and a voltage and a current generator proportional to the duty ratio modulation input.

The canonical model in block 5 of the Flowchart can be obtained following either path a or path b, namely from block 4a or 4b, as will be shown later. However, following the general description of the final averaged model in block 4a, certain generalizations about the canonical model are made possible, which are otherwise not achievable. Namely, even though for all currently known switching dc-to-dc converters (such as the buck, boost, buck-boost, Venable [3], Weinberg [4] and a number of others) the frequency dependence appears only in the duty-ratio dependent voltage generator but not in the current generator, and then only as a first-order (single-zero) polynomial in poles of the effective filter network which essentially constitute the line voltage to output transfer function. Moreover, in general, both duty-ratio dependent generators, voltage and current, are frequency dependent (additional zeros and poles). That in the particular cases of the boost or buck-boost converters this dependence reduces to a first order polynomial results from the fact that the order of the system which is involved in the switching action is only two. Hence from the general result, the order of the polynomial is at most one, though it could reduce to a pure constant, as in the buck or the Venable converter [3].

The significance of the new circuit model is that any switching dc-to-dc converter can be reduced to this canonical fixed topology form, at least as far as its input-output and control properties are concerned, hence it is valuable for duty cycle D (in general, the effective filter elements depend on duty ratio D), and the configuration chosen which optimizes the size and weight. Also, comparison of the frequency dependence of the two duty-ratio dependent generators provides insight into the question of stability once a regulator feedback loop is closed.

1.4 Extension to Complete Regulator Treatment

Finally, all the results obtained in modelling the converter or, more accurately, the network which effectively takes part in switching action, can easily be incorporated into more complicated systems containing dc-to-dc converters. For example, by modelling the modulator stage along the same lines, one can obtain a linear circuit model of a closed-loop switching regulator. Standard linear feedback theory can then be used for both analysis and synthesis, stability considerations, and proper design of feedback compensating networks for multiple loop as well as single-loop regulator configurations.

2. STATE-SPACE AVERAGING

In this section the state-space averaging method is developed first in general for any dc-to-dc switching converter, and then demonstrated in detail for the particular case of the boost power stage in which parasitic effects (esr of the capacitor and series resistance of the inductor) are included. General equations for both steady-state (dc) and dynamic performance (ac) are obtained, from which important transfer functions are derived and also applied to the special case of the boost power stage.

switching between two linear networks consisting of ideally lossless storage elements, inductances and capacitances. In practice, this function may be obtained by use of transistors and diodes which operate as synchronous switches. On the assumption that the circuit operates in the so-called "continuous conduction" mode in which the instantaneous inductor current does not fall to zero at any point in the cycle, there are only two different "states" of the circuit. Each state, however, can be represented by a linear circuit model (as shown in block 1b of Fig. 1) or by a corresponding set of state-space equations (block 1a). Even though any set of linearly independent variables can be chosen as the state variables, it is customary and convenient in electrical networks to adopt the inductor currents and capacitor voltages. The total number of storage elements thus determines the order of the system. Let us denote such a choice of a vector of state-
tion mode can be described by the state space
equations for the two switched models:

(i) interval Td: (ii) interval Td':

$$\dot{x} = A_1 x + b_1 v_g \qquad \dot{x} = A_2 x + b_2 v_g$$
$$y_1 = c_1^T x \qquad y_2 = c_2^T x \tag{1}$$

where Td denotes the interval when the switch is in the on state and $T(1-d) \equiv Td'$ is the interval for which it is in the off state, as shown in Fig. 2. The static equations $y_1 = c_1^T x$ and $y_2 = c_2^T x$ are necessary in order to account for the case when the output quantity does not

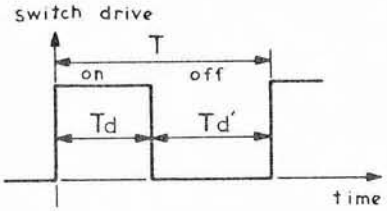

Fig. 2. Definition of the two switched intervals Td and Td'.

coincide with any of the state variables, but is rather a certain linear combination of the state variables.

Our objective now is to replace the state-space description of the two linear circuits emanating from the two successive phases of the switching cycle T by a single state-space description which represents approximately the behaviour of the circuit across the whole period T. We therefore propose the following simple averaging step: take the average of both dynamic and static equations for the two switched intervals (1), by summing the equations for interval Td multiplied by d and the equations for interval Td' multiplied by d'. The following <u>linear continuous system</u> results:

$$\dot{x} = d(A_1 x + b_1 v_g) + d'(A_2 x + b_2 v_g)$$
$$y = dy_1 + d'y_2 = (dc_1^T + d'c_2^T)x \tag{2}$$

After rearranging (2) into the standard linear continuous system state-space description, we obtain the basic averaged state-space description (over a single period T):

$$\dot{x} = (dA_1 + d'A_2)x + (db_1 + d'b_2)v_g$$
$$y = (dc_1^T + d'c_2^T)x \tag{3}$$

This model is the basic averaged model which is the starting model for all other derivations (both state-space and circuit oriented).

Note that in the above equations the duty ratio d is considered constant; it is not a time dependent variable (yet), and particularly not a switched discontinuous variable which changes between 0 and 1 as in [1] and [2], but is merely a fixed number for each cycle. This is evident from the model derivation in Appendix A. In particular, when d = 1 (switch constantly on) the averaged model (3) reduces to switched model (1i), and when d = 0 (switch off) it reduces to switched model (1ii).

In essence, comparison between (3) and (1) shows that the system matrix of the averaged model is obtained by taking the average of two switched model matrices A_1 and A_2, its control is the average of two control vectors b_1 and b_2, and its output is the average of two outputs y_1 and y_2 over a period T.

The justification and the nature of the approximation in substitution for the two switched models of (1) by averaged model (3) is indicated in Appendix A and given in more detail in [6]. The basic approximation made, however, is that of approximation of the fundamental matrix $e^{At} = I + At + \cdots$ by its first-order linear term. This is, in turn, shown in Appendix B to be the same approximation necessary to obtain the dc condition independent of the storage element values (L,C) and dependent on the dc duty ratio only. It also coincides with the requirement for low output voltage ripple, which is shown in Appendix C to be equivalent to $f_c/f_s \ll 1$, namely the effective filter corner frequency much lower than the switching frequency.

The model represented by (3) is an averaged model over a single period T. If we now assume that the duty ratio d is constant from cycle to cycle, namely, d = D (steady state dc duty ratio), we get:

$$\dot{x} = Ax + bv_g$$
$$y = c^T x \tag{4}$$

where

$$A = DA_1 + D'A_2$$
$$b = Db_1 + D'b_2 \tag{5}$$
$$c^T = Dc_1^T + D'c_2^T$$

Since (4) is a linear system, superposition holds and it can be perturbed by introduction of line voltage variations $\hat{v}_g$ as $v_g = V_g + \hat{v}_g$, where V_g is the dc line input voltage, causing a corresponding perturbation in the state vector $x = X + \hat{x}$, where again X is the dc value of the state vector and $\hat{x}$ the superimposed ac perturbation. Similarly, $y = Y + \hat{y}$, and

$$\dot{\hat{x}} = AX + bV_g + A\hat{x} + b\hat{v}_g$$
$$Y + \hat{y} = c^T X + c^T \hat{x} \tag{6}$$

Separation of the steady-state (dc) part from the dynamic (ac) part then results in the steady state (dc) model

$$AX + bV_g = 0;\ Y = c^T X \Rightarrow Y = -c^T A^{-1} b V_g \tag{7}$$

and the dynamic (ac) model

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + b\hat{v}_g \\ \hat{y} &= c^T\hat{x} \end{aligned} \tag{8}$$

It is interesting to note that in (7) the steady state (dc) vector X will in general only depend on the dc duty ratio D and resistances in the original model, but not on the storage element values (L's and C's). This is so because X is the solution of the linear system of equations

$$AX + bV_g = 0 \tag{9}$$

in which L's and C's are proportionality constants. This is in complete agreement with the first-order approximation of the exact dc conditions shown in Appendix B, which coincides with expression (7).

From the dynamic (ac) model, the line voltage to state-vector transfer functions can be easily derived as:

$$\begin{aligned} \frac{\hat{x}(s)}{\hat{v}_g(s)} &= (sI-A)^{-1}b \\ \frac{\hat{y}(s)}{\hat{v}_g(s)} &= c^T(sI-A)^{-1}b \end{aligned} \tag{10}$$

Hence at this stage both steady-state (dc) and line transfer functions are available, as shown by block 6a in the Flowchart of Fig. 1. We now undertake to include the duty ratio modulation effect into the basic averaged model (3).

2.2 Perturbation

Suppose now that the duty ratio changes from cycle to cycle, that is, $d(t) = D + \hat{d}$ where D is the steady-state (dc) duty ratio as before and $\hat{d}$ is a superimposed (ac) variation. With the corresponding perturbation definition $x = X + \hat{x}$,

$$\underbrace{X}_{\text{dc term}} + \underbrace{\hat{x}}_{\text{line variation}} + \underbrace{[(A_1-A_2)\hat{x} + (b_1-b_2)\hat{v}_g]\hat{d}}_{\text{duty ratio variation}} \tag{11}$$

nonlinear second-order term

$$Y + \hat{y} = \underbrace{c^T X}_{\text{dc term}} + \underbrace{c^T\hat{x}}_{\text{ac term}} + \underbrace{(c_1^T-c_2^T)X\hat{d}}_{\text{ac term}} + \underbrace{(c_1^T-c_2^T)\hat{x}\hat{d}}_{\text{nonlinear term}}$$

The perturbed state-space description is nonlinear owing to the presence of the product of the two time dependent quantities $\hat{x}$ and $\hat{d}$.

2.3 Linearization and Final State-Space Averaged Model

Let us now make the small-signal approximation, namely that departures from the steady state values are negligible compared to the steady state values themselves:

$$\frac{\hat{v}_g}{V_g} \ll 1, \qquad \frac{\hat{d}}{D} \ll 1, \quad \frac{\hat{x}}{X} \ll 1 \tag{12}$$

Then, using approximations (12) we neglect all nonlinear terms such as the second-order terms in (11) and obtain once again a linear system, but including duty-ratio modulation $\hat{d}$. After separating steady-state (dc) and dynamic (ac) parts of this linearized system we arrive at the following results for the final state-space averaged model.

Steady-state (dc) model:

$$X = -A^{-1}bV_g; \quad Y = c^T X = -c^T A^{-1} b V_g \tag{13}$$

Dynamic (ac small-signal) model:

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + b\hat{v}_g + [(A_1-A_2)X + (b_1-b_2)V_g]\hat{d} \\ \hat{y} &= c^T\hat{x} + (c_1^T-c_2^T)X\hat{d} \end{aligned} \tag{14}$$

In these results, A, b and c^T are given as before by (5).

Equations (13) and (14) represent the small-signal low-frequency model of any two-state switching dc-to-dc converter working in the continuous conduction mode.

It is important to note that by neglect of the nonlinear term in (11) the source of harmonics is effectively removed. Therefore, the linear description (14) is actually a linearized describing function result that is the limit of the describing function as the amplitude of the input signals $\hat{v}_g$ and/or $\hat{d}$ becomes vanishingly explained in [1], [2], or [8] in which small-signal assumption (12) is preserved. Very good agreement up to close to half the switching frequency has been demonstrated repeatedly ([1], [2], [3], [7]).

2.4 Example: Boost Power Stage with Parasitics

We now illustrate the method for the boost power stage shown in Fig. 3.

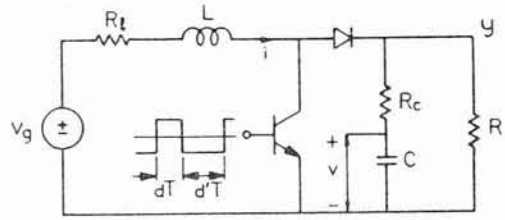

Fig. 3. Example for the state—space averaged modelling: boost power stage with parasitics included.

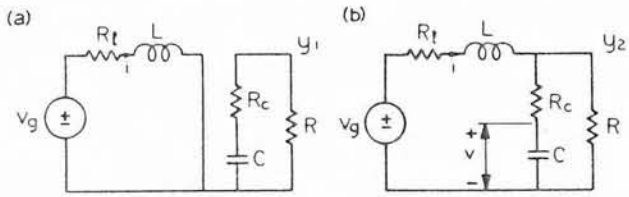

Fig. 4. Two switched circuit models of the circuit in Fig. 3 with assumption of ideal switches. All elements in the final state-space averaged model (13) and (14) are obtained: A_1, b_1, c_1^T from a) for interval Td, and A_2, b_2, c_2^T from b) for interval Td'.

With assumption of ideal switches, the two switched models are as shown in Fig. 4. For choice of state-space vector $x^T = (i\ v)$, the state space equations become:

$$y_1 = c_1^T x \qquad\qquad y_2 = c_2^T x$$

where

$$A_1 = \begin{bmatrix} -\frac{R_\ell}{L} & 0 \\ 0 & -\frac{1}{(R+R_c)C} \end{bmatrix} \qquad A_2 = \begin{bmatrix} -\frac{R_\ell + R_c \| R}{L} & -\frac{R}{L(R+R_c)} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix}$$

$$c_1^T = \begin{bmatrix} 0 & \frac{R}{R+R_c} \end{bmatrix} \qquad c_2^T = \begin{bmatrix} R \| R_c & \frac{R}{R+R_c} \end{bmatrix} \tag{16}$$

Note that (15) is the special case of (1) in which $b_1 = b_2 = b = [1/L\ \ 0]^T$.

Using (16) and (5) in the general result (13) and (14), we obtain the following final state-space averaged model.

Steady-state (dc) model:

$$X = \begin{bmatrix} I \\ V \end{bmatrix} = \frac{V_g}{R'} \begin{bmatrix} 1 \\ (1-D)R \end{bmatrix}; \quad Y = \frac{V_g (1-D) R}{R'} \tag{17}$$

in which I is the dc inductor current, V is the dc capacitor voltage, and Y is the dc output voltage.

Dynamic (ac small signal) model:

$$\frac{d}{dt}\begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} = \begin{bmatrix} -\frac{R_\ell + (1-D)(R_c \| R)}{L} & -\frac{(1-D)R}{L(R+R_c)} \\ \frac{(1-D)R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \frac{R}{L} \frac{(D'R+R_c)}{R+R_c} \\ -\frac{R}{(R+R_c)C} \end{bmatrix} \frac{V_g \hat{d}}{R'} \tag{18}$$

$$\hat{y} = \begin{bmatrix} (1-D)(R_c \| R) & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} - V_g \frac{R_c \| R}{R'} \hat{d}$$

in which $R' \triangleq (1-D)^2 R + R_\ell + D(1-D)(R_c \| R)$.

We now look more closely at the dc voltage transformation ratio in (17):

$$\frac{V}{V_g} = \frac{Y}{V_g} = \underbrace{\frac{1}{1-D}}_{\text{ideal dc gain}} \underbrace{\frac{(1-D)^2 R}{(1-D)^2 R + R_\ell + D(1-D)(R_c \| R)}}_{\text{correction factor}} \tag{19}$$

This shows that the ideal dc voltage gain is 1/D' when all parasitics are zero ($R_\ell = 0$, $R_c = 0$) and that in their presence it is slightly reduced by a correction factor less than 1. Also we observe that nonzero ESR of the capacitance ($R_c \neq 0$) (with discontinuity of output voltage was not included in [2], but was correctly accounted for in [1].

From the dynamic model (18) one can find the duty ratio to output and line voltage to output transfer functions, which agree exactly with those obtained in [1] by following a different method of averaged model derivation based on the equivalence of circuit topologies of two switched networks.

The fundamental result of this section is the development of the general state-space averaged model represented by (13) and (14), which can be easily used to find the small-signal low-frequency model of any switching dc-to-dc converter. This was demonstrated for a boost power stage with parasitics resulting in the averaged model (17) and (18). It is important to emphasize that, unlike the transfer function description, the state-space description (13) and (14) gives the complete system behaviour. This is very useful in implementing two-loop and multi-loop feedback when two or more states are used in a feedback path to modulate the duty ratio $\hat{d}$. For example, both output voltage and inductor current may be returned in a feedback loop.

3. HYBRID MODELLING

In this section it will be shown that for any specific converter a useful circuit realization of the basic averaged model given by (3) can always be found. Then, in the following section, the perturbation and linearization steps will be carried out on the circuit model finally to arrive at the circuit model equivalent of (13) and (14).

The circuit realization will be demonstrated for the same boost power stage example, for which the basic state-space averaged model (3) becomes:

$$\begin{bmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_\ell + d'(R_c \| R)}{L} & -\frac{d'R}{L(R+R_c)} \\ \frac{d'R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_g$$

$$y = \begin{bmatrix} d'(R_c \| R) & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} \tag{20}$$

In order to "connect" the circuit, we express the capacitor voltage v in terms of the desired output quantity y as:

$$v = \frac{R+R_c}{R} y - (1-d) R_c i$$

or, in matrix form

$$\begin{bmatrix} i \\ v \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -d'R_c & \frac{R+R_c}{R} \end{bmatrix} \begin{bmatrix} i \\ y \end{bmatrix} \tag{21}$$

Substitution of (21) into (20) gives

$$\begin{bmatrix} L\frac{di}{dt} \\ C\frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} \underbrace{-(R_\ell + dd'(R_c \| R)}_{\text{additional resistance}} & \underbrace{-d'}_{\text{ideal transformer}} \\ d' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i \\ y \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} v_g \tag{22}$$

From (22) one can easily reconstruct the circuit representation shown in Fig. 5.

The basic model (22) is valid for the dc regime, and the two dependent generators can be modeled as an ideal d':1 transformer whose range extends down to dc, as shown in Fig. 6.

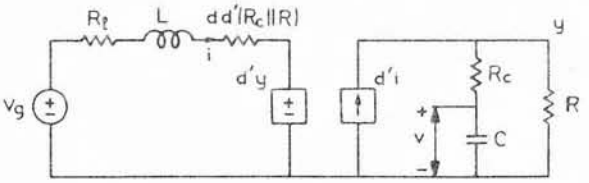

Fig. 5. Circuit realization of the basic state-space averaged model (20) through hybrid modelling.

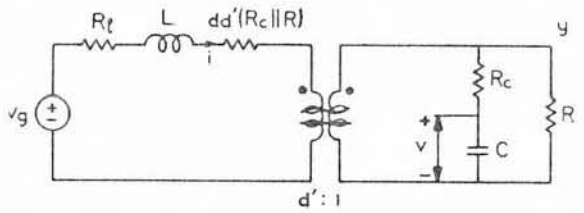

Fig. 6. Basic circuit averaged model for the boost circuit example in Fig. 3. Both dc-to-dc conversion and line variation are modelled when d(t)=D.

As before, we find that the circuit model in Fig. 6 reduces for d = 1 to switched model in Fig. 4a, and for d = 0 to switched model in Fig. 4b. In both cases the additional resistance $R_1 = dd'(R_c \| R)$ disappears, as it should.

If the duty ratio is constant so d = D, the dc regime can be found easily by considering inductance L to be short and capacitance C to be open for dc, and the transformer to have a D':1 ratio. Hence the dc voltage gain (19) can be directly seen from Fig. 6. Similarly, all line transfer functions corresponding to (10) can be easily found from Fig. 6.

It is interesting now to compare this ideal d':1 transformer with the usual ac transformer. While in the latter the turns ratio is fixed, the one employed in our model has a dynamic turns ratio d':1 which changes when the duty ratio is a function of time, d(t). It is through this ideal transformer that the actual controlling function is achieved when the feedback loop is closed. In addition the ideal transformer has a dc transformation ratio d':1, while a real transformer works for ac signals only. Nevertheless, the concept of the ideal transformer in Fig. 6 with such properties is a very useful one, since after all the switching converter has the overall property of a dc-to-dc transformer whose turns ratio can be dynamically adjusted by duty ratio modulation to achieve the controlling function. We will, however, see in the next section how this can be more explicitly modelled in terms of duty-ratio dependent generators only.

Following the procedure outlined in this section one can easily obtain the basic averaged circuit models of three common converter power stages, as shown in the summary of Fig. 7.

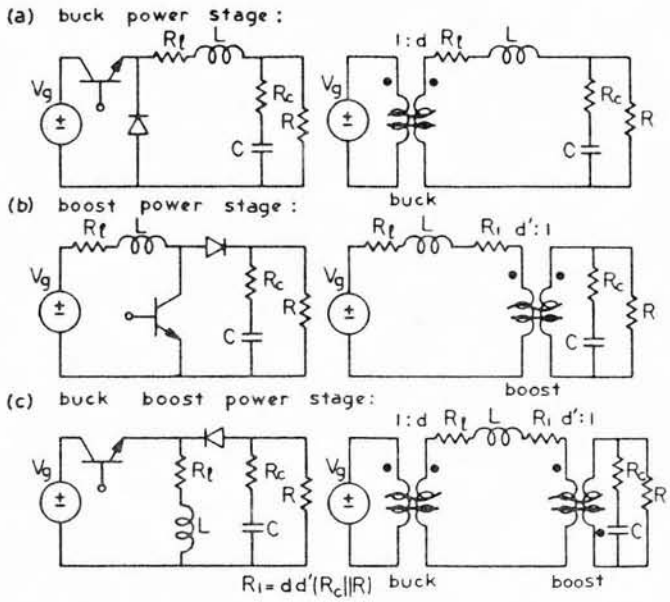

Fig. 7. Summary of basic circuit averaged models for three common power stages: buck, boost, and buck-boost.

The two switched circuit state-space models for the power stages in Fig. 7 are such that the general equations (1) reduce to the special cases $A_1 = A_2 = A$, $b_1 \neq b_2 = 0$ (zero vector) for the buck power stage, and $A_1 \neq A_2$, $b_1 = b_2 = b$ for the boost power stage, whereas for the buck-boost power stage $A_1 \neq A_2$ and $b_1 \neq b_2 = 0$ so that the general case is retained.

4. CIRCUIT AVERAGING

As indicated in the Introduction, in this section the alternative path b in the Flowchart of Fig. 1 will be followed, and equivalence with the previously developed path a firmly established. The final circuit averaged model for the same example of the boost power stage will be arrived at, which is equivalent to its corresponding state-space description given by (17) and (18).

The averaged circuit models shown in Fig. 7 could have been obtained as in [2] by directly averaging the corresponding components of the two switched models. However, even for some simple cases such as the buck-boost or tapped inductor boost [1] this presents some difficulty owing to the requirement of having two switched circuit models topologically equivalent, while there is no such requirement in the outlined procedure.

In this section we proceed with the perturbation and linearization steps applied to the circuit model, continuing with the boost power stage as an example in order to include explicitly the duty ratio modulation effect.

4.1 Perturbation

If the averaged model in Fig. 7b is perturbed according to $v_g = V_g + \hat{v}_g$, $i = I + \hat{i}$, $d = D + \hat{d}$, $d' = D' - \hat{d}$, $v = V + \hat{v}$, $y = Y + \hat{y}$ the nonlinear model in Fig. 8 results.

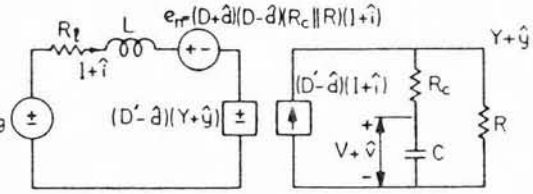

Fig. 8. Perturbation of the basic averaged circuit model in Fig. 6 includes the duty ratio modulation effect $\hat{d}$, but results in this nonlinear circuit model.

4.2 Linearization

Under the small-signal approximation (12), the following linear approximations are obtained:

$$e_n \approx DD'(R_c \| R)(I+\hat{i}) + \hat{d}(D'-D)(R_c \| R)I$$

$$(D'-\hat{d})(Y+\hat{y}) \approx D'(Y+\hat{y}) - \hat{d}Y$$

$$(D'-\hat{d})(I+\hat{i}) \approx D'(I+\hat{i}) - \hat{d}I$$

and the final averaged circuit model of Fig. 9 results. In this circuit model we have finally obtained the controlling function separated in terms of duty ratio $\hat{d}$ dependent generators e_1 and j_1, while the transformer turns ratio is dependent on the dc duty ratio D only. The circuit model obtained in Fig. 9 is equivalent to the state-space description given by (17) and (18).

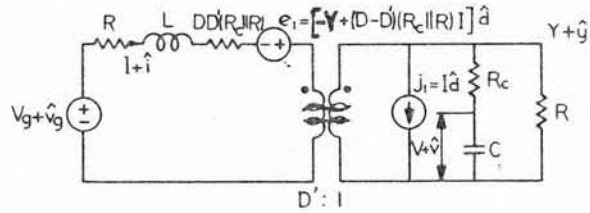

Fig. 9. Under small-signal assumption (12), the model in Fig. 8 is linearized and this final averaged circuit model of the boost stage in Fig. 3 is obtained.

5. THE CANONICAL CIRCUIT MODEL

Even though the general final state-space averaged model in (13) and (14) gives the complete description of the system behaviour, one might still wish to derive a circuit model describing its input-output and control properties as illustrated in Fig. 10.

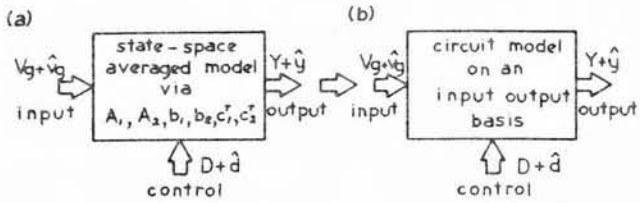

Fig. 10. Definition of the modelling objective: circuit averaged model describing input-output and control properties.

In going from the model of Fig. 10a to that of Fig. 10b some information about the internal behaviour of some of the states will certainly be lost but, on the other hand, important advantages will be gained as were briefly outlined in the Introduction, and as this section will illustrate.

We propose the following fixed topology circuit model, shown in Fig. 11, as a realization

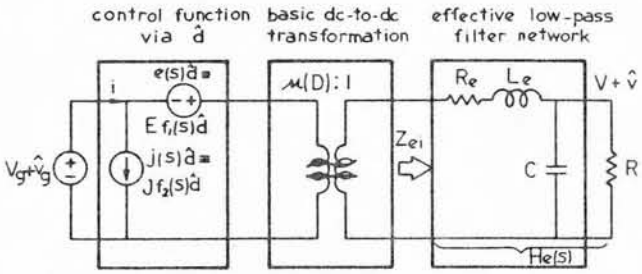

Fig. 11. Canonical circuit model realization of the "black box" in Fig. 10b, modelling the three essential functions of any dc-to-dc converter: control, basic dc conversion, and low-pass filtering.

of the "black box" in Fig. 10b. We call this model the canonical circuit model, because any switching converter input-output model, regardless of its detailed configuration, could be represented in this form. Different converters are represented simply by an appropriate set of formulas for the four elements $e(s)$, $j(s)$, μ, $H_e(s)$ in the general equivalent circuit. The polarity of the ideal μ:1 transformer is determined by whether or not the power stage is polarity inverting. Its turns ratio μ is dependent on the dc duty ratio D, and since for modelling purposes the transformer is assumed to operate down to dc, it provides the basic dc-to-dc level conversion. The single-section low-pass L_eC filter is shown in Fig. 11 only for illustration purposes, because the actual number and configuration of the L's and C's in the effective filter transfer function realization depends on the number of storage elements in the original converter.

The resistance R_e is included in the model of Fig. 11 to represent the damping properties of the effective low-pass filter. It is an "effective" resistance that accounts for various series ohmic resistances in the actual circuit (such as R_ℓ in the boost circuit example), the additional "switching" resistances due to discontinuity of the output voltage (such as $R_1 = DD'(R_c \| R)$ in the boost circuit example), and also a "modulation" resistance that arises from a modulation of the switching transistor storage time [1].

5.1 Derivation of the Canonical Model through State-Space

From the general state-space averaged model (13) and (14), we obtain directly using the Laplace transform:

$$\hat{x}(s)=(sI-A)^{-1}b\hat{v}_g(s)+(sI-A)^{-1}\left[(A_1-A_2)X+(b_1-b_2)V_g\right]\hat{d}(s)$$
$$\hat{y}(s)=c^T\hat{x}(s)+(c_1^T-c_2^T)X\hat{d}(s) \tag{23}$$

Now, from the complete set of transfer functions we single out those which describe the converter input-output properties, namely

$$\hat{y}(s) = G_{vg}\,\hat{v}_g(s) + G_{vd}\,\hat{d}(s)$$
$$\hat{i}(s) = G_{ig}\,\hat{v}_g(s) + G_{id}\,\hat{d}(s) \tag{24}$$

in which the G's are known explicitly in terms of the matrix and vector elements in (23).

Equations (24) are analogous to the two-port network representation of the terminal properties of the network (output voltage $\hat{y}(s)$ and input current $\hat{i}(s)$). The subscripts designate the corresponding transfer functions. For example G_{vg} is the source voltage $\hat{v}_g$ to output voltage $\hat{y}$ transfer function, G_{id} is the duty ratio $\hat{d}$ to input current $\hat{i}(s)$ transfer function, and so on.

For the proposed canonical circuit model in Fig. 11, we directly get:

$$\hat{y}(s) = (\hat{v}_g+e\hat{d})\,\frac{1}{\mu}\,H_e(s)$$
$$\hat{i}(s) = j\,\hat{d} + (e\hat{d}+\hat{v}_g)\,\frac{1}{\mu^2 Z_{ei}(s)} \tag{25}$$

or, after rearrangement into the form of (24):

$$\hat{y}(s) = \frac{1}{\mu}\,H_e(s)\,\hat{v}_g(s) + e\,\frac{1}{\mu}\,H_e(s)\hat{d}(s)$$
$$\hat{i}(s) = \frac{1}{\mu^2 Z_{ei}(s)}\,\hat{v}_g(s) + \left[j + \frac{e}{\mu^2 Z_{ei}(s)}\right]\hat{d}(s) \tag{26}$$

Direct comparison of (24) and (26) provides the solutions for $H_e(s)$, $e(s)$, and $j(s)$ in terms of the known transfer functions G_{vg}, G_{vd}, G_{ig} and G_{id} as:

$$e(s) = \frac{G_{vd}(s)}{G_{vg}(s)}\,, \qquad j(s) = G_{id}(s) - e(s)G_{ig}(s)$$
$$H_e(s) = \mu G_{vg}(s) \tag{27}$$

Note that in (27) the parameter $1/\mu$ represents the ideal dc voltage gain when all the parasitics are zero. For the previous boost power stage example, from (19) we get $\mu = 1-D$ and the correction factor in (19) is then associated with the effective filter network $H_e(s)$. However, μ could be found from

$$\frac{Y}{V_g} = -c^T A^{-1} b = \frac{1}{\mu} \times (\text{correction factor}) \qquad (28)$$

by setting all parasitics to zero and reducing the correction factor to 1.

The physical significance of the ideal dc gain μ is that it arises as a consequence of the switching action, so it cannot be associated with the effective filter network which at dc has a gain (actually attenuation) equal to the correction factor.

The procedure for finding the four elements in the canonical model of Fig. 11 is now briefly reviewed. First, from (28) the basic dc-to-dc conversion factor μ is found as a function of dc duty ratio D. Next, from the set of all transfer functions (23) only those defined by (24) are actually calculated. Then, by use of these four transfer functions G_{vd}, G_{vg}, G_{id}, G_{ig} in (27) the frequency dependent generators $e(s)$ and $j(s)$ as well as the low-pass filter transfer function $H_e(s)$ are obtained.

The two generators could be further put into the form

$$e(s) = Ef_1(s)$$

$$j(s) = Jf_2(s)$$

where $f_1(0) = f_2(0) = 1$, such that the parameters E and J could be identified as dc gains of the frequency dependent functions $e(s)$ and $j(s)$.

Finally, a general synthesis procedure [10] for realization of L,C transfer functions terminated in a single load R could be used to obtain a low-pass ladder-network circuit realization of the effective low-pass network $H_e(s)$. Though for the second-order example of $H_e(s)$ this step is trivial and could be done by inspection, for higher-order transfer functions the orderly procedure of the synthesis [10] is almost mandatory.

5.2 Example: Ideal Buck-boost Power Stage

For the buck-boost circuit shown in Fig. 7c

$$\begin{bmatrix} \frac{d\hat{v}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{D'}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \hat{v} \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \frac{-V}{D'RC} \end{bmatrix} \hat{d} \qquad (29)$$

in which the output voltage $\hat{y}$ coincides with the state-variable capacitance voltage $\hat{v}$.

From (28) and (29) one obtains $\mu = D'/D$. With use of (29) to derive transfer functions, and upon substitution into (27), there results

$$e(s) = \frac{-V}{D^2}\left(1 - s\frac{DL}{D'^2R}\right), \quad j(s) = \frac{-V}{(1-D)^2R}$$

$$H_e(s) = \frac{1}{1 + s/RC + s^2L_eC}, \quad \mu = \frac{1-D}{D} \qquad (30)$$

in which V is the dc output voltage.

The effective filter transfer function is easily seen as a low-pass LC filter with $L_e = L/D'^2$ and with load R. The two generators in the canonical model of Fig. 11 are identified by

$$E = \frac{-V}{D^2}, \qquad f_1(s) \equiv 1 - s\frac{DL}{D'^2R}$$

$$J = \frac{-V}{(1-D)^2R}, \qquad f_2(s) \equiv 1 \qquad (31)$$

We now derive the same model but this time using the equivalent circuit transformations and path b in the Flowchart of Fig. 1.

After perturbation and linearization of the circuit averaged model in Fig. 7c (with $R_\ell=0$, $R_c=0$) the series of equivalent circuits of Fig. 12 is obtained.

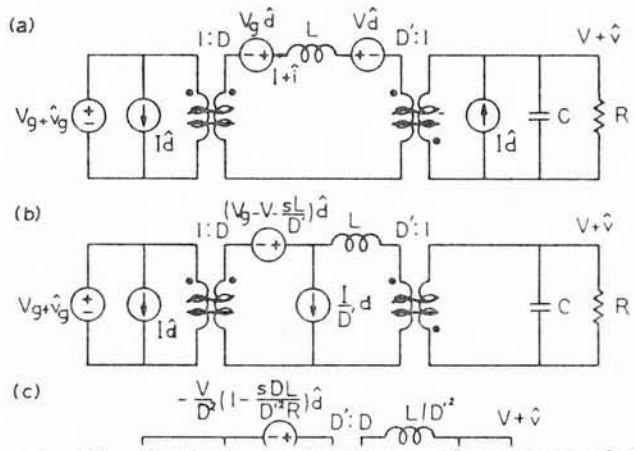

Fig. 12. Equivalent circuit transformations of the final circuit averaged model (a), leading to its canonical circuit realization (c) demonstrated on the buck-boost example of Fig. 7c (with $R_\ell=0$, $R_c=0$).

The objective of the transformations is to reduce the original four duty-ratio dependent generators in Fig. 12a to just two generators (voltage and current) in Fig. 12c which are at the input port of the model. As these circuit transformations unfold, one sees how the frequency dependence in the generators arises naturally, as in Fig. 12b. Also, by transfer of the two generators in Fig. 12b from the secondary to the primary of the 1:D transformer, and the inductance L to the secondary of the D':1 transformer, the cascade of two ideal transformers is reduced to the single transformer with equivalent turns ratio D':D. At the same time the effective filter network L_e, C, R is generated.

Expressions for the elements in the canonical equivalent circuit can be found in a similar way for any converter configuration. Results for the three familiar converters, the buck, boost, and buck-boost power stages are summarized in Table I.

	$A(D)$	E	$f_1(s)$	J	$f_2(s)$	L_e
buck	$\frac{1}{D}$	$\frac{V}{D^2}$	1	$\frac{V}{R}$	1	L
boost	$1-D$	V	$1-A\frac{L_e}{R}$	$\frac{V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$
buck-boost	$\frac{1-D}{D}$	$\frac{-V}{D^2}$	$1-A\frac{DLs}{R}$	$\frac{-V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$

Table I Definition of the elements in the canonical circuit model of Fig. 11 for the three common power stages of Fig. 7.

It may be noted in Table I that, for the buck-boost power stage, parameters E and J have negative signs, namely $E = -V/D^2$ and $J = -V/(D'^2R)$. However, as seen from the polarity of the ideal D':D transformer in Fig. 12c this stage is an inverting one. Hence, for positive input dc voltage V_g, the output dc voltage V is negative ($V < 0$) since $V/V_g = -D/D'$. Therefore $E > 0$, $J > 0$ and consequently the polarity of the voltage and current duty-ratio dependent generators is not changed but is as shown in Fig. 12c. Moreover, this is true in general: regardless of any inversion property of the power stage, the polarity of two generators stays the same as in Fig. 11.

5.3 Significance of the Canonical Circuit Model and Related Generalizations

pass filtering (represented by the effective low-pass filter network $H_e(s)$). Note also that the current generator $j(s)\hat{d}$ in the canonical circuit model, even though superfluous when the source voltage $v_g(s)$ is ideal, is necessary to reflect the influence of a nonideal source generator (with some internal impedance) or of an input filter [7] upon the behaviour of the converter. Its presence enables one easily to include the linearized circuit model of a switching converter power stage in other linear circuits, as the next section will illustrate.

Another significant feature of the canonical circuit model is that any switching dc-to-dc converter can be reduced by use of (23), (24), (27) and (28) to this fixed topology form, at least as far as its input-output and control properties are concerned. Hence the possibility arises for use of this model to compare in an easy and unique way various performance characteristics of different converters. Some examples of such comparisons are given below.

1. The filter networks can be compared with respect to their effectiveness throughout the dynamic duty cycle D range, because in general the effective filter elements depend on the steady state duty ratio D. Thus, one has the opportunity to choose the configuration and to optimize the size and weight.

2. Basic dc-to-dc conversion factors $\mu_1(D)$ and $\mu_2(D)$ can be compared as to their effective range. For some converters, traversal of the range of duty ratio D from 0 to 1 generates any conversion ratio (as in the ideal buck-boost converter), while in others the conversion ratio might be restricted (as in the Weinberg converter [4], for which $\frac{1}{2}<\mu<1$).

3. In the control section of the canonical model one can compare the frequency dependences of the generators e(s) and j(s) for different converters and select the configuration that best facilitates stabilization of a feedback regulator. For example, in the buck-boost converter e(s) is a polynomial, containing actually a real zero in the right half-plane, which undoubtedly causes some stability problems and need for proper compensation.

4. Finally, the canonical model affords a very convenient means to store and file information on various dc-to-dc converters in a computer memory in a form comparable to Table I. Then, thanks to the fixed topology of the canonical circuit model, a single computer program can be used to calculate and plot various quantities as functions of frequency (input and output impedance, audio susceptibility, duty ratio to output transfer response, and so on). Also, various input filters and/or additional output filter networks can easily be added if desired.

functions of complex frequency s. Hence, in general both some new zeros and poles are introduced into the duty ratio to output transfer function owing to the switching action, in addition to the poles and zeros of the effective filter network (or line to output transfer function). However, in special cases, as in all

those shown in Table I, the frequency dependence might reduce simply to polynomials, and even further it might show up only in the voltage dependent generators (as in the boost, or buck-boost) and reduce to a constant ($f_2(s) \equiv 1$) for the current generator. Nevertheless, this does not prevent us from modifying any of these circuits in a way that would exhibit the general result -- introduction of both additional zeros as well as poles.

Let us now illustrate this general result on a simple modification of the familiar boost circuit, with a resonant L_1, C_1 circuit in series with the input inductance L, as shown in Fig. 13.

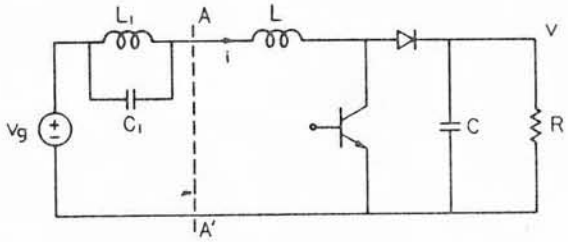

Fig. 13. Modified boost circuit as an illustration of general frequency behaviour of the generators in the canonical circuit model of Fig. 11.

By introduction of the canonical circuit model for the boost power stage (for the circuit to the right of cross section AA') and use of data from Table I, the equivalent averaged circuit model of Fig. 14a is obtained. Then, by application of the equivalent circuit transformation as outlined previously, the averaged model in the canonical circuit form is obtained in Fig. 14b. As can be seen from Fig. 14b, the voltage generator has a double pole at the resonant frequency $\omega_r = 1/\sqrt{L_1 C_1}$ of the parallel L_1, C_1 network. However, the effective filter transfer function has a double zero (null in magnitude) at precisely the same location such that the two

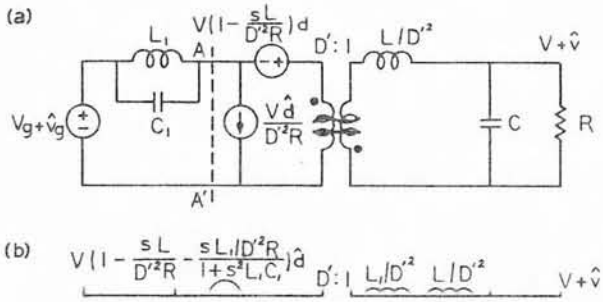

Fig. 14. Equivalent circuit transformation leading to the canonical circuit model (b) of the circuit in Fig. 13.

pairs effectively cancel. Hence, the resonant null in the magnitude response, while present in the line voltage to output transfer function, is not seen in the duty ratio-to output transfer function. Therefore, the positive effect of rejection of certain input frequencies around the resonant frequency ω_r is not accompanied by a detrimental effect on the loop gain, which will not contain a null in the magnitude response.

This example demonstrates yet another important aspect of modelling with use of the averaging technique. Instead of applying it directly to the whole circuit in Fig. 13, we have instead implemented it only with respect to the storage element network which effectively takes part in the switching action, namely L, C, and R. Upon substitution of the switched part of the network by the averaged circuit model, all other linear circuits of the complete model are retained as they appear in the original circuit (such as L_1, C_1 in Fig. 14a). Again, the current generator in Fig. 14a is the one which reflects the effect of the input resonant circuit.

In the next section, the same property is clearly displayed for a closed-loop regulator-converter with or without the input filter.

6. SWITCHING MODE REGULATOR MODELLING

This section demonstrates the ease with which the different converter circuit models developed in previous sections can be incorporated into more complicated systems such as a switching-mode regulator. In addition, a brief discussion of modelling of modulator stages in general is included, and a complete general switching-mode regulator circuit model is given.

A general representation of a switching-mode regulator is shown in Fig. 15. For concreteness, the switching-mode converter is represented by a buck-boost power stage, and the input and possible additional output filter are represented by a

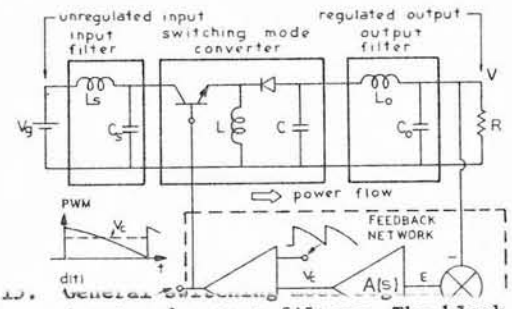

Fig. 15. General switching-mode regulator with input and output filters. The block diagram is general, and single-section LC filters and a buck-boost converter are shown as typical realizations.

single-section low-pass LC configuration, but the discussion applies to any converter and any filter configuration.

The main difficulty in analysing the switching mode regulator lies in the modelling of its nonlinear part, the switching-mode converter. However, we have succeeded in previous sections in obtaining the small-signal low-frequency circuit model of any "two-state" switching dc-to-dc converter, operating in the continuous conduction mode, in the canonical circuit form. The output filter is shown separately, to emphasize the fact that in averaged modelling of the switching-mode converter only the storage elements which are actually involved in the switching action need be taken into account, thus minimizing the effort in its modelling.

The next step in development of the regulator equivalent circuit is to obtain a model for the modulator. This is easily done by writing an expression for the essential function of the modulator, which is to convert an (analog) control voltage V_c to the switch duty ratio D. This expression can be written $D = V_c/V_m$ in which, by definition, V_m is the range of control signal required to sweep the duty ratio over its full range from 0 to 1. A small variation v_c superimposed upon V_c therefore produces a corresponding variation $\hat{d} = \hat{v}_c/V_m$ in D, which can be generalized to account for a nonuniform frequency response as

$$\hat{d} = \frac{f_m(s)}{V_m}\,\hat{v}_c \qquad (32)$$

in which $f_m(0) = 1$. Thus, the control voltage to duty ratio small-signal transmission characteristic of the modulator can be represented in general by the two parameters V_m and $f_m(s)$, regardless of the detailed mechanism by which the modulation is achieved. Hence, by substitution for $\hat{d}$ from (32) the two generators in the canonical circuit model of the switching converter can be expressed in terms of the ac control voltage $\hat{v}_c$, and the resulting model is then a linear ac equivalent circuit that represents the small-signal transfer properties of the nonlinear processes in the modulator and converter.

It remains simply to add the linear amplifier and the input and output filters to obtain the ac equivalent circuit of the complete closed-loop regulator as shown in Fig. 16.

The modulator transfer function has been incorporated in the generator designations, and the generator symbol has been changed from a circle to a square to emphasize the fact that, in the closed-loop regulator, the generators no longer are independent but are dependent on another signal in the same system. The connection from point Y to the error amplifier, via the reference voltage summing node, represents the basic voltage feedback necessary to establish the system as a voltage regulator. The dashed connection from point Z indicates a possible additional feedback sensing; this second feedback signal may

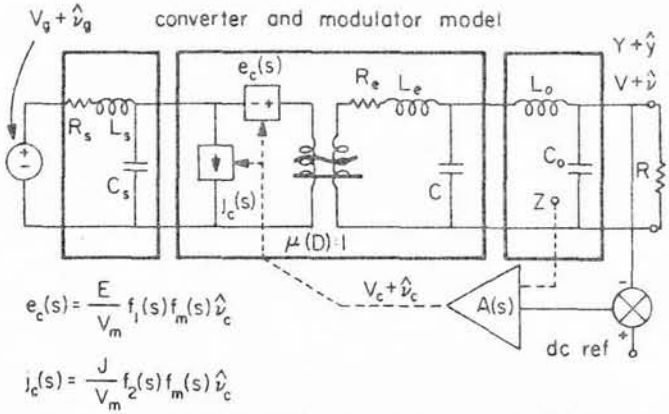

Fig. 16. General small-signal ac equivalent circuit for the switching-mode regulator of Fig. 15.

be derived, for example, from the inductor flux, inductor current, or capacitor current, as in various "two-loop" configurations that are in use [9].

Once again the current generator in Fig. 16 is responsible for the interaction between the switching-mode regulator-converter and the input filter, thus causing performance degradation and/or stability problems when an arbitrary input filter is added. The problem of how properly to design the input filter is treated in detail in [7].

As shown in Fig. 16 we have succeeded in obtaining the linear circuit model of the complete switching mode-regulator. Hence the well-known body of linear feedback theory can be used for both analysis and design of this type of regulator.

7. CONCLUSIONS

A general method for modelling power stages of any switching dc-to-dc converter has been developed through the state-space approach. The fundamental step is in replacement of the state-space descriptions of the two switched networks by their average over the single switching period T, which results in a single continuous state-space equation description (3) designated the basic averaged state-space model. The essential approximations made are indicated in the Appendices, and are shown to be justified for any practical dc-to-dc switching converter.

The subsequent perturbation and linearization step under the small-signal assumption (12) leads to the final state-space averaged model given by (13) and (14). These equations then serve as the basis for development of the most important qualitative result of this work, the canonical circuit model of Fig. 11. Different converters are represented simply by an appropriate set of formulas ((27) and (28)) for four elements in this general equivalent circuit. Besides its unified description, of which several

examples are given in Table I, one of the advantages of the canonical circuit model is that various performance characteristics of different switching converters can be compared in a quick and easy manner.

Although the state-space modelling approach has been developed in this paper for two-state switching converters, the method can be extended to multiple-state converters. Examples of three-state converters are the familiar buck, boost, and buck-boost power stages operated in the discontinuous conduction mode, and dc-to-ac switching inverters in which a specific output waveform is "assembled" from discrete segments are examples of multiple-state converters.

In contrast with the state-space modelling approach, for any particular converter an alternative path via hybrid modelling and circuit transformation could be followed, which also arrives first at the final circuit averaged model equivalent of (13) and (14) and finally, after equivalent circuit transformations, again arrives at the canonical circuit model.

Regardless of the derivation path, the canonical circuit model can easily be incorporated into an equivalent circuit model of a complete switching regulator, as illustrated in Fig. 16.

Perhaps the most important consequence of the canonical circuit model derivation via the general state-space averaged model (13), (14), (23) and (24) is its prediction through (27) of additional zeros as well as poles in the duty ratio to output transfer function. In addition frequency dependence is anticipated in the duty ratio dependent current generator of Fig. 11, even though for particular converters considered in Table I, it reduces merely to a constant. Furthermore for some switching networks which would effectively involve more than two storage elements, higher order polynomials should be expected in $f_1(s)$ and/or $f_2(s)$ of Fig. 11.

The insights that have emerged from the general state-space modelling approach suggest that there is a whole field of new switching dc-to-dc converter power stages yet to be conceived. This encourages a renewed search for innovative circuit designs in a field which is yet young, and promises to yield a significant number of inventions in the stream of its full development. This progress will naturally be fully supported by new technologies coming at an ever increasing pace. However, even though the efficiency and performance of currently existing converters will increase through better, faster transistors, more ideal capacitors (with lower esr) and so on, it will be primarily the responsibility of the circuit designer and inventor to put these components to best use in an optimal topology. Search for new circuit configurations, and how best to use present and future technologies, will be of prime importance in achieving the ultimate goal of near-ideal general switching dc-to-dc converters.

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