High Side MOSFET Gate Drive: The Power of Well Implemented Pulse Transformers

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Many different techniques and circuits are available for providing high side N-Channel MOSFET gate drive. Most techniques implement gate drive using pulse transformers or charge pump solutions. In this application note we examine the performance capabilities and other properties of one particular pulse transformer high side gate drive circuit (shown in figure 1).

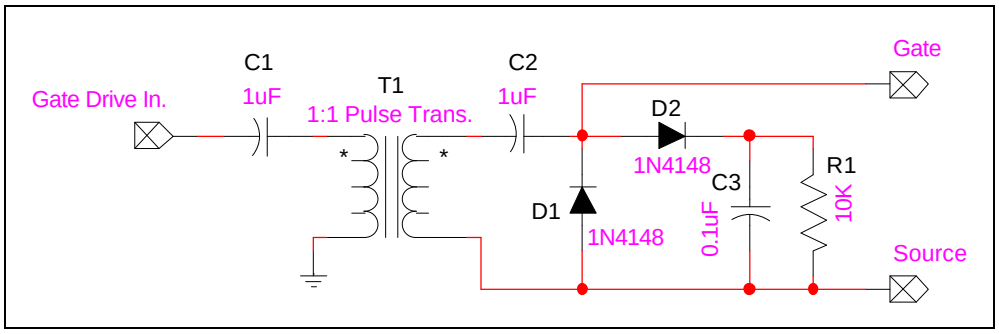

Figure 1
T1: Amidon Associates core FT37-77, Primary 25T, Secondary 25T bifilar wound
Core Specifications: Permeability 2000, O.D. 0.375 in., I.D. 0.187 in., A_e 0.076 cm^2

Circuit Operation:
A low impedance MOSFET gate drive signal is AC coupled to the primary of a small pulse transformer through a non-polarized capacitor (C1). This AC coupling insures volt-second balance is applied to the transformer over all duty ratios from 1%-99%. Capacitor C2 and diode D1 form a charge pump to recreate the incoming gate drive signal.

Diode D2, capacitor C3, and resistor R1 form an RCD (resistor, capacitor, diode) snubber to dissipate voltage transients caused by loosely coupled secondary inductance. During gate transitions uncoupled secondary inductance will produce a voltage spike. Without the RCD snubber this spike may be large enough to puncture the MOSFET's gate oxide layer destroying the MOSFET. A standard gate resistor will not be able to protect the MOSFET. During normal operation the voltage across capacitor C3 is maintained at about 10V. If inductive transient voltages higher than +10V plus one diode drop (from D2) appear at the MOSFET gate, capacitor C3 acts as a low impedance shunt. Positive voltages higher than 10V plus one diode drop get clipped by quickly charging C3. Resistor R1 must be of sufficiently small value to dissipate all of this extra energy before the next cycle or capacitor C3 will charge to an indeterminately higher voltage until resistor R1 does dissipate enough energy. At higher frequencies resistor R1 will have less time between cycles to dissipate this extra energy, and the value will likely need to be decreased (unless transformer modifications are also made which further reduce the amount of uncoupled secondary inductance).

Negative voltage transients that would otherwise occur at the gate during turn-off get temporarily absorbed by capacitor C2 through diode D1. During gate turn-on this extra charge is pumped over to capacitor C3 through diode D2 and must also eventually be dissipated by resistor R1.

The input and output signals are in phase with the exception of a very small delay caused by the leakage inductance in T1 increasing rise and fall times. Transformer T1 should therefore be designed for minimum leakage inductance (i.e. bifilar windings on a low leakage core). High voltage primary/secondary isolation can be obtained by using well insulated wire (as apposed to magnet wire), however a core with more window area than T1 of figure 1 may be needed.

This circuit does not eliminate the need for a low impedance ground referenced gate driver. Peak gate charging and discharging currents are furnished instantly through the pulse transformer from the input gate drive signal. This circuit can provide useable duty ratios from 1%-99%. Duty ratios from 0%-99% may also be practical; however the first few pulses in a pulse train after a long delay will likely be clipped as capacitor C3 charges to its full voltage. This may cause problems in pulse width modulated (PWM) switching power supplies that switch over to pulse frequency modulation (PFM) at very low load currents. As currently drawn the circuit will easily operate over a frequency range from 35kHz-200kHz. For higher and lower frequencies slight circuit modifications might be necessary to obtain good performance. At lower frequencies primary and secondary turns may need to be increased, and at high frequencies the value of R1 and the turns on T1 may need to be decreased. With small circuit modifications operation down to 10kHz and up to 2MHz should be practical.

Measuring the Performance of Pulse Transformer Isolated Gate Drive of Figure 1:

In order to measure the performance of figure 1, one must pay significant attention to minimize the limiting impact other circuit devices might cause. Specifically we must use a low impedance gate driver. We will need an oscillator that is capable of operating over extremely large (99%) and small (1%) duty ratios. The oscillator and gate driver we selected is depicted in figure 2.

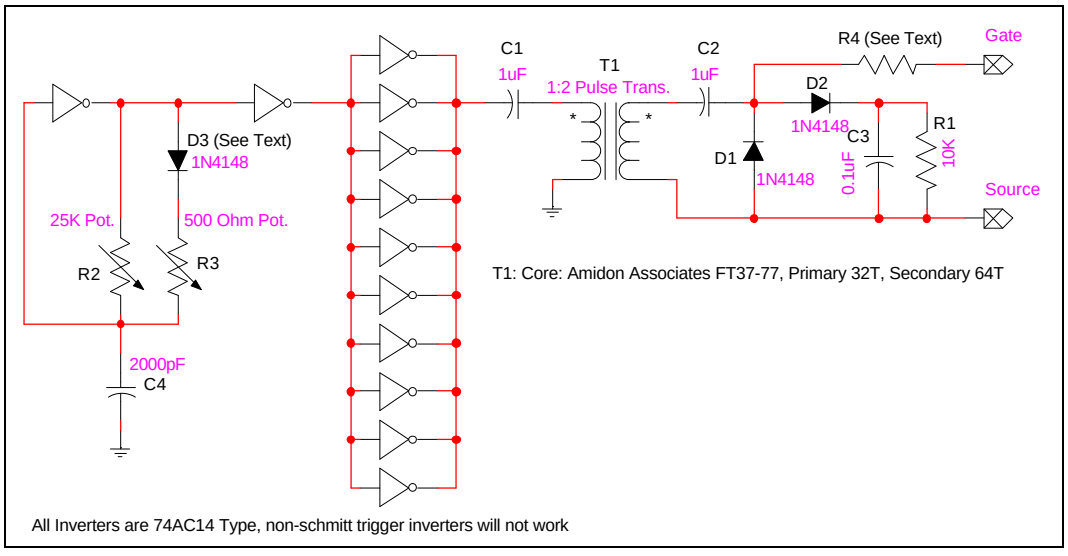

Figure 2, Test Circuit Schematics

The leftmost inverter of figure 2 forms a CMOS Schmitt trigger inverter type oscillator with components R2 and C4. By default it will oscillate with 50% duty ratio, and the frequency is adjustable over a wide range by adjusting potentiometer R2. Components R3 and D3 are needed to modify the base 50% duty ratio. When diode D3 points in the direction shown, this circuit will oscillate with a duty ratio less than 50%. By reversing diode D3 duty ratios greater than 50% can be obtained.

The array of (10) inverters are used as the gate driver. 74AC14 Type gates can continuously sink/source 24mA of current. According to Fairchild Semiconductor's datasheets[(1)] for the 74AC14, each gate has a guaranteed "maximum dynamic output current" of +/- 75mA at 5.5V Vcc. Using this figure we can calculate/estimate the maximum output impedance of each inverter using Ohm's Law.

X_R=5.5V/0.075A
X_R=73.3 Ohms

This suggests the maximum output impedance of our array of inverters is 7.3 Ohms (at 5.5V Vcc). In practice the typical output impedance may be lower than this figure. This fairly low impedance gate driver should allow the pulse transformer circuit to demonstrate most of its capabilities. Since we are using 5V logic as a gate driver, we have modified the turns ratio to 1:2 so that nominally 10V will be produced to fully enhance normal MOSFETs.

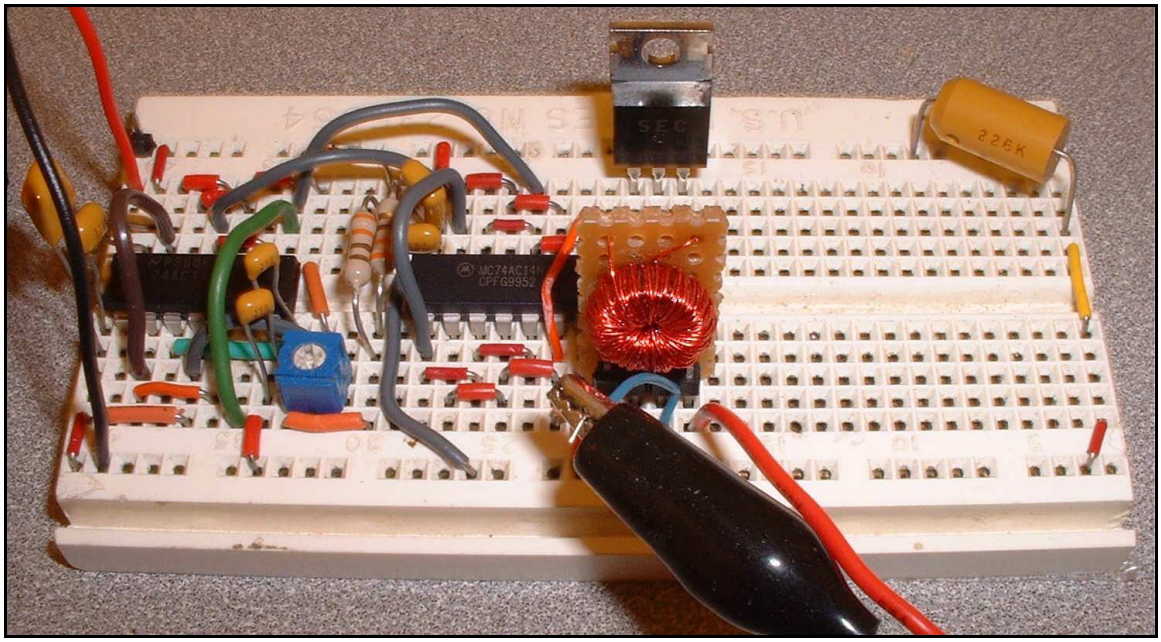

Figure 3, The Test Circuit

In this application note we will not attempt to drive large MOSFETs at 200kHz with duty ratio extremes of 1% or 99%. Large MOSFETs such as the MTB75N05HD can have very considerable switching rise and fall times. The aforementioned MOSFET has a typical turn on time of 185ns, turn off time of 170ns, and maximum turn on time of 370ns, maximum turn off

time of 340ns as specified in On Semiconductor's datasheet[(2)]. At 200kHz 1% duty ratio the MOSFET would need to turn fully on and off in a mere 50ns according to the calculations:
Time per Period = 1/200,000 = 5us
Assuming 1% duty ratio, the MOSFET will be on for 1% of that 5us, or:
On Time = 5us x 0.01 = 50ns

Large MOSFETs such as the MTB75N05HD cannot switch anywhere near this fast irregardless of the gate drive scheme used; therefore we will use lower frequencies of about 50kHz with fairly small fast MOSFETs for extreme duty ratio testing. At very large and small duty ratios the time constant of the gate resistor (used to damp gate ringing caused by parasitic inductance) can also have a significant impact on switching performance. As an example a small 1nF load with a 10 ohm series resistor has a time constant of 10ns. Since it takes approximately three time constants to reach 90% of full voltage across the capacitor, rise/fall times cannot be lower than about 30ns.

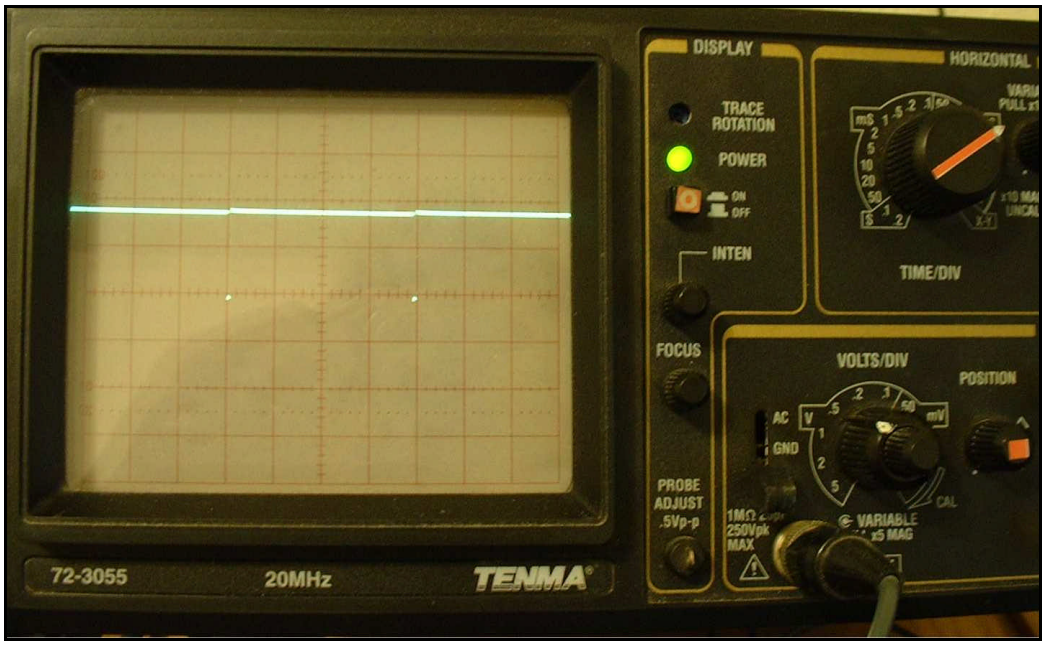

Figure 4, Horizontal 5us/div. Vertical 5V/div. (probe 10X attenuation in use)

Figure 4 shows the trace produced at the output of figure 2 with no load (except the 25pF capacitance of the oscilloscope probe and other stray capacitance) at about 50kHz 99% duty ratio. The value of R4 in figure 2 for this test is zero ohms. On time is about 19.7us, off time about 200ns. The off time only appears as little dots in the figure. The output voltage is slightly under 10V.

Figure 5 shows the trace produced when the circuit of figure 2 drives a fixed 1nF capacitor at 50kHz 99% duty ratio. This test was conducted with a value of 0 ohms for R4 in figure 2. Notice the thickening of the vertical part of the trace as compared to figure 4, however wave shaping is still very close to ideal. Also notice the small "blip" appearing at the top of each turn on (and how the low voltage at off time is slightly lower than ground), this is caused by uncoupled inductance in T1 and other parasitic inductance. The uncoupled inductance causes a spike that is clipped at one diode drop above/below the ideal transformer output voltage. Also notice that this trace fully reaches 10V when on whereas in figure 4 the voltage appearing was slightly less. Interestingly the output voltage is somewhat dependant upon the load capacitance and upon the frequency. It would therefore be wise to specifically optimize the value of R1 and the number of turns/turns ratio in figure 2 for different loads.

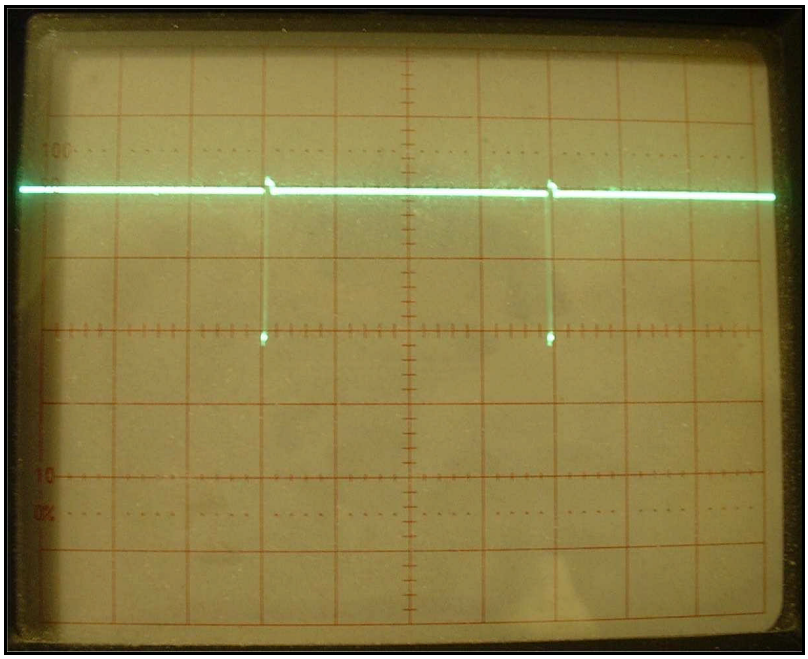

Figure 5, Horizontal 5us/div. Vertical 5V/div.

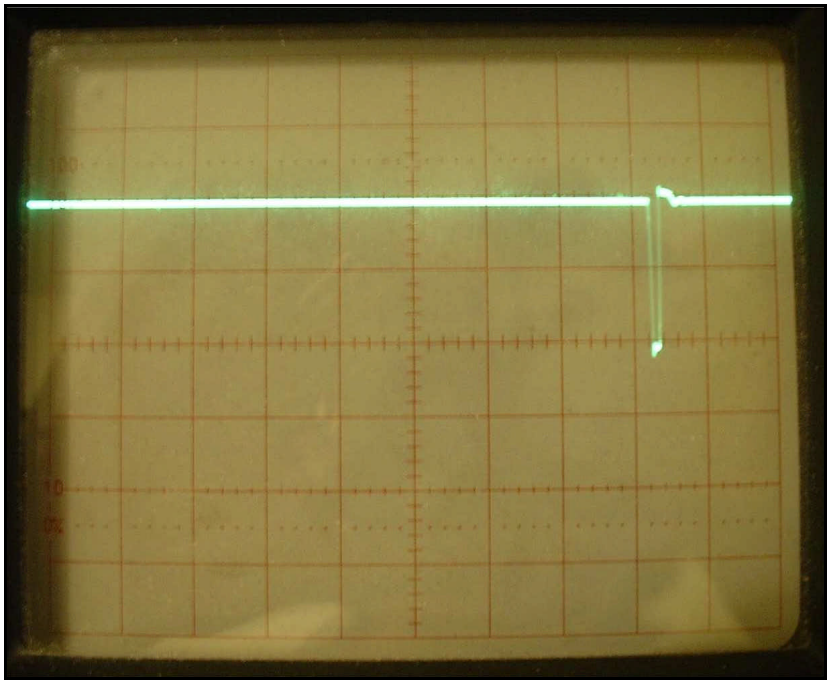

Figure 6, Horizontal 2us/div. Vertical 5V/div.

Figure 6 was taken under the same conditions as figure 5 but the horizontal timescale has been decreased to 2us per division. Turn on and turn off time is very fast.

Figure 7 shows the gate waveform when two Si9410DY SO-8 MOSFETs are tied in parallel and are actively switching nominally 4.8V into an 18 ohm resistive load (to produce some Miller effect). Gate resistor R4 of figure 2 remains at 0 ohms. A single Si9410DY MOSFET has a published[3] typical gate charge of 24nC, 50nC max. When driving two in parallel the effective gate charge would typically be 48nC, 100nC maximum. Fall time is clearly longer than rise time. The point where the MOSFET actually switches on is just barely visible in figure 7 where the trace appears slightly bolder (on the rising side at about 3V). The top of the 'v' shaped curve appears to be a little under 400ns wide but at 50kHz 99% duty ratio the off time should be 200ns. Since actual switching occurs at about 3V, it would appear the actual off time of the MOSFET is around 200ns.

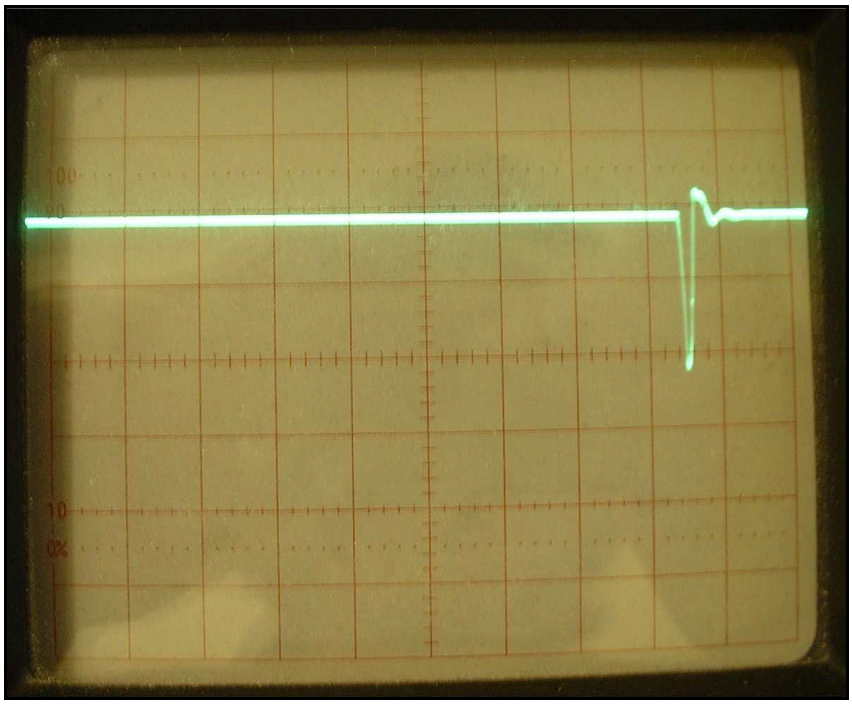

Figure 7, Horizontal 2us/div. Vertical 5V/div.

Figure 8 demonstrates figure 2's phase delay between input gate signals (bottom trace) and actual gate response (top trace) on an MTP3055E with zero volts drain-source through a 10 ohm gate resistor. Phase delay between signals is negligible. The frequency is about 260kHz, and we observe potentially objectionable spikes on the gate even though the MOSFET is not switching any load. This figure demonstrates the need to decrease the number of turns used on the pulse transformer windings for high frequency operation. Uncoupled inductance in the

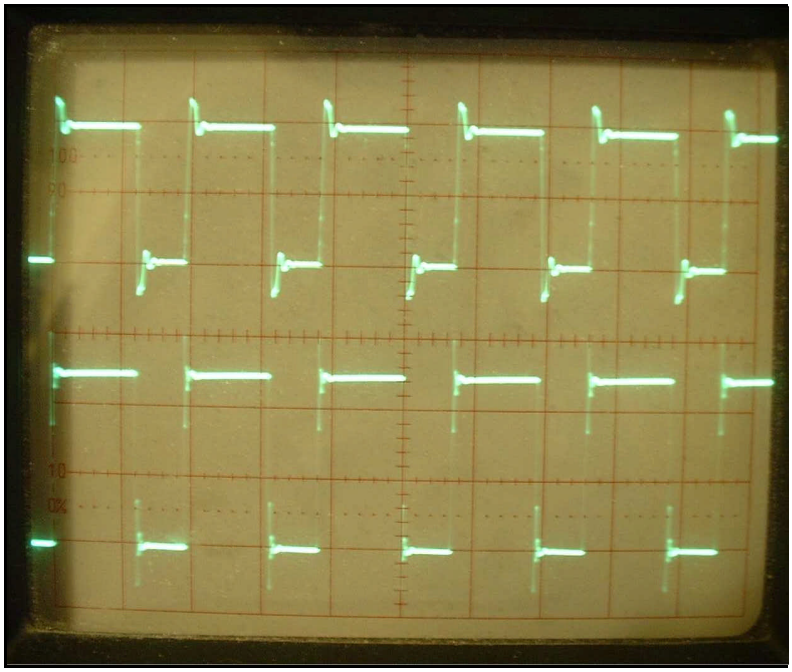

Figure 8, Horizontal 2us/div. Bottom Trace Vertical 2V/div. Top Trace 5V/div.

pulse transformer generally increases proportional to the square of the turns, and can quickly become a problem at high frequencies.

Figure 9 demonstrates volt-second balance applied to the primary of the transformer with a duty ratio of about 91% at 365kHz while driving a 1nF load using the circuit in figure 1. A 1:1 pulse transformer as described in figure 1 was used for this test. Volt-second balance is continuously applied to the core over all duty ratios from 1%-99% because the input signal is AC coupled through capacitor C1 of figure 1.

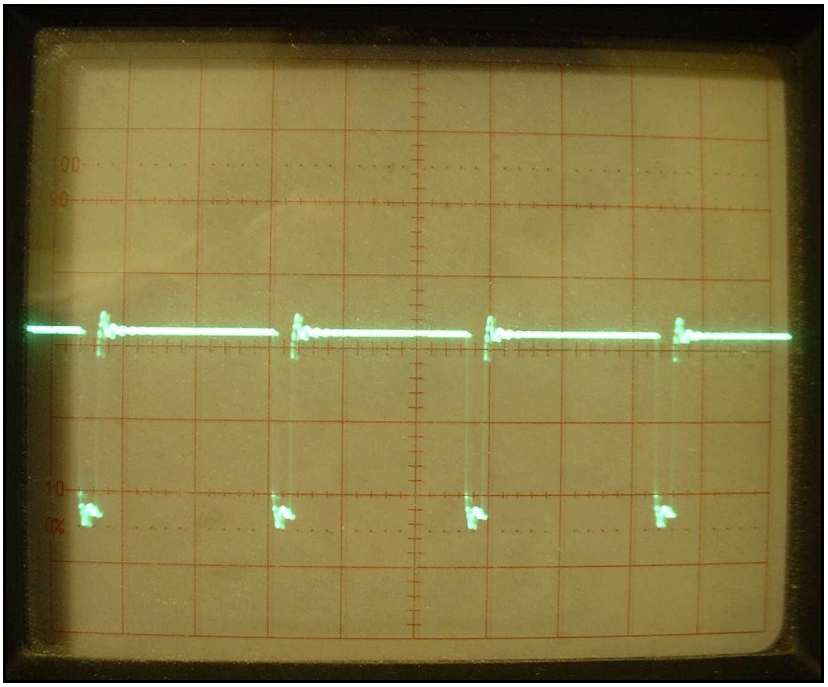

Figure 9, Horizontal 1us/div. Vertical 2V/div.

References:

Web addresses valid as of December 8, 2001

(1)
Fairchild Semiconductor's 74AC14 datasheet:
http://www.fairchildsemi.com/ds/74/74AC14.pdf

Mailing Address of World Headquarters:

82 Running Hill Road
South Portland, ME 04106
U.S.A.

Tel: 207-775-8100
Tel: 800-341-0392 (outside Maine)
Tel: 800-832-5505 (inside Maine)

(2)
On Semiconductor's MTB75N05HD datasheet:
http://www.onsemi.com/pub/Collateral/MTB75N05HD-D.PDF

North American Technical Support: 800-282-9855
Corporate Offices: 602-244-6600

(3)
Vishay Siliconix's Si9410DY datasheet:
http://www.vishay.com/doc?70122

Related Information:

International Rectifier
"Gate Drive Characteristics and Requirements for HEXFETs"
AN-937
http://www.irf.com/technical-info/appnotes/an-937.pdf

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