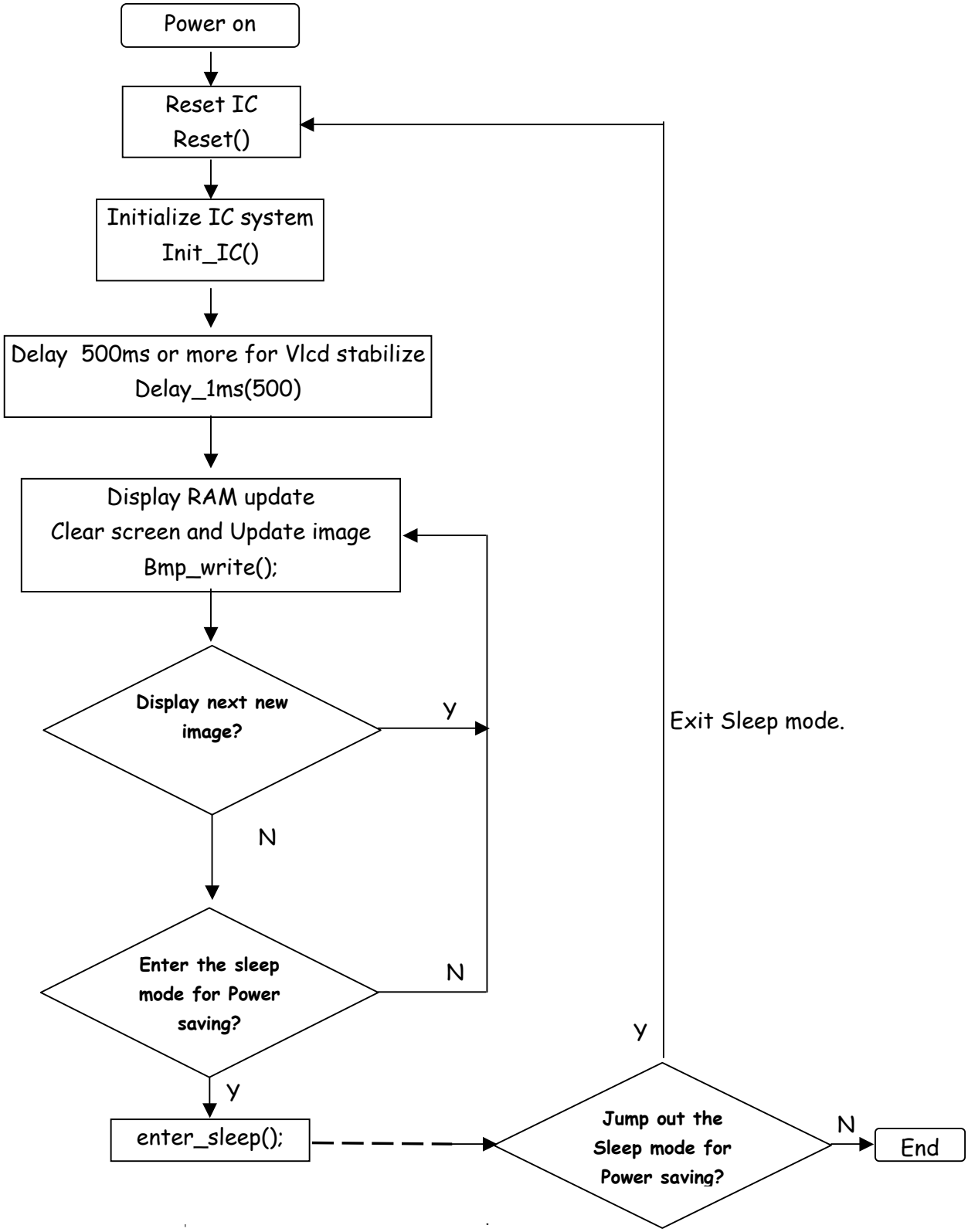
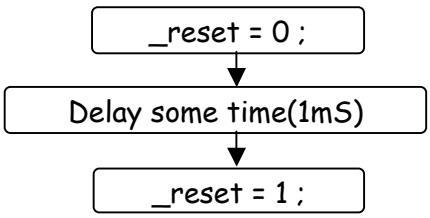
The GD1001 IC program flow chart

(1) Program Flow Block Diagram. (Pls refer to the Driving example(v4.1).c file)



The GD1001 IC program flow chart

(2) Reset:



(3) Initialized Module

1) Enable analog block	command	0xa3
	command	0x1a
2) Enable Oscillator	command	0xf6
	command	0x40
3) Set the Driving Parameters	command	0x80
4) Set temperature value	command	0x00
Set VA clear hold time (for 18mS)	command	0x0C
5) Set VA idle hold time (for 12mS)	command	0x0a
Set AA clear hold time (for 100mS)	command	0x15
6) Set AA idle hold time (for 12mS)	command	0x0a
Set Driving using time (for 18mS)	command	0x0c
7) Set clear voltage (for 24V)	command	0x40(24V)
Set drive voltage (for 24V)	command	0x40(24V)
8) Enable Bias Ladder	command	0xe9
	command	0x84
9) Enable Booster and High Volt Buffer	command	0x2f
10) Set the multiplex ratio (set to 64)	command	0xa8
	command	0x40
11) Set Module bias (set to 1/ 7)	command	0xa2
	command	0x02
12) Set the normal or Reverse Display (set to normal)	command	0xa6
13) Set the Segment Re-map (setting from S0-->S127)	command	0xa0
14) Set the Common Re-map (setting C63--->C0)	command	0xc8
15) Set Display Start line (set to C0)	command	0x40
16) VA clear repeat times(set to 0x00)	command	0x93
	command	0x00
17) VA idle repeat times (set to 0x00)	command	0x94
	command	0x00
18) AA clear repeat times (set to 0x00)	command	0x95
	command	0x00
19) AA idle repeat times (set to 0x00)	command	0x96
	command	0x00
20)Driving repeat times (set to 0x00)	command	0x97
	command	0x00
21)Driving update command	command	0x31

If you want to modify the parameter, pls refer to Figure 1 .

If you want to modify the parameter, pls refer to Figure 2 .

The GD1001 IC program flow chart

Note:

1) The reference codes are mix of single and double byte command operation.

2) Pls write the Driving update command after finishing all he command, otherwise, the commands that is wrote is invalid.

3) All the above initialisation sequence must be followed before writing to graphic RAM.

4) For 4 wire SPI Command and Data Timing characteristics-->pls refer to Figure 3.

Figure 1 Clear, idle & driving phase programmable time duration

$X_4X_3X_2X_1X_0$	Time for 1 pixel /ms
00000	0.08
00001	0.2
00010	0.4
00011	0.8
00100	1
00101	2
00110	4
00111	6
01000	8
01001	10
01010	12
01011	14
01100	18
01101	20
01110	25
01111	30

$X_4X_3X_2X_1X_0$	Time for 1 pixel /ms
10000	35
10001	40
10010	50
10011	60
10100	80
10101	100
10110	150
10111	200
11000	250
11001	350
11010	500
11011	750
11100	1,000
11101	2,000
11110	4,000
11111	10,000

Figure 2 Voltage Setting Table (For Clear and Driving Voltage Setting)

X6X5X4X3X2X1X0	Vcp1/V
0001000	10
0001001	10.25
0001010	10.5
0001011	10.75
0001100	11
0001101	11.25
0001110	11.5
0001111	11.75
0010000	12
0010001	12.25
0010010	12.5
0010011	12.75
0010100	13
0010101	13.25
0010110	13.5
0010111	13.75
0011000	14
0011001	14.25
0011010	14.5
0011011	14.75
0011100	15
0011101	15.25
0011110	15.5
0011111	15.75
0100000	16
0100001	16.25
0100010	16.5
0100011	16.75
0100100	17
0100101	17.25
0100110	17.5
0100111	17.75
0101000	18
0101001	18.25
0101010	18.5
0101011	18.75
0101100	19
0101101	19.25
0101110	19.5
0101111	19.75

X6X5X4X3X2X1X0	Vcp1/V
0110000	20
0110001	20.25
0110010	20.5
0110011	20.75
0110100	21
0110101	21.25
0110110	21.5
0110111	21.75
0111000	22
0111001	22.25
0111010	22.5
0111011	22.75
0111100	23
0111101	23.25
0111110	23.5
0111111	23.75
1000000	24
1000001	24.25
1000010	24.5
1000011	24.75
1000100	25
1000101	25.25
1000110	25.5
1000111	25.75
1001000	26
1001001	26.25
1001010	26.5
1001011	26.75
1001100	27
1001101	27.25
1001110	27.5
1001111	27.75
1010000	28
1010001	28.25
1010010	28.5
1010011	28.75
1010100	29
1010101	29.25
1010110	29.5
1010111	29.75

X6X5X4X3X2X1X0	Vcp1/V
1011000	30
1011001	30.25
1011010	30.5
1011011	30.75
1011100	31
1011101	31.25
1011110	31.5
1011111	31.75
1100000	32
1100001	32.25
1100010	32.5
1100011	32.75
1100100	33
1100101	33.25
1100110	33.5
1100111	33.75
1101000	34
1101001	34.25
1101010	34.5
1101011	34.75
1101100	35

Figure 3 4-wires Serial Interface Timing Characteristics

Conditions:

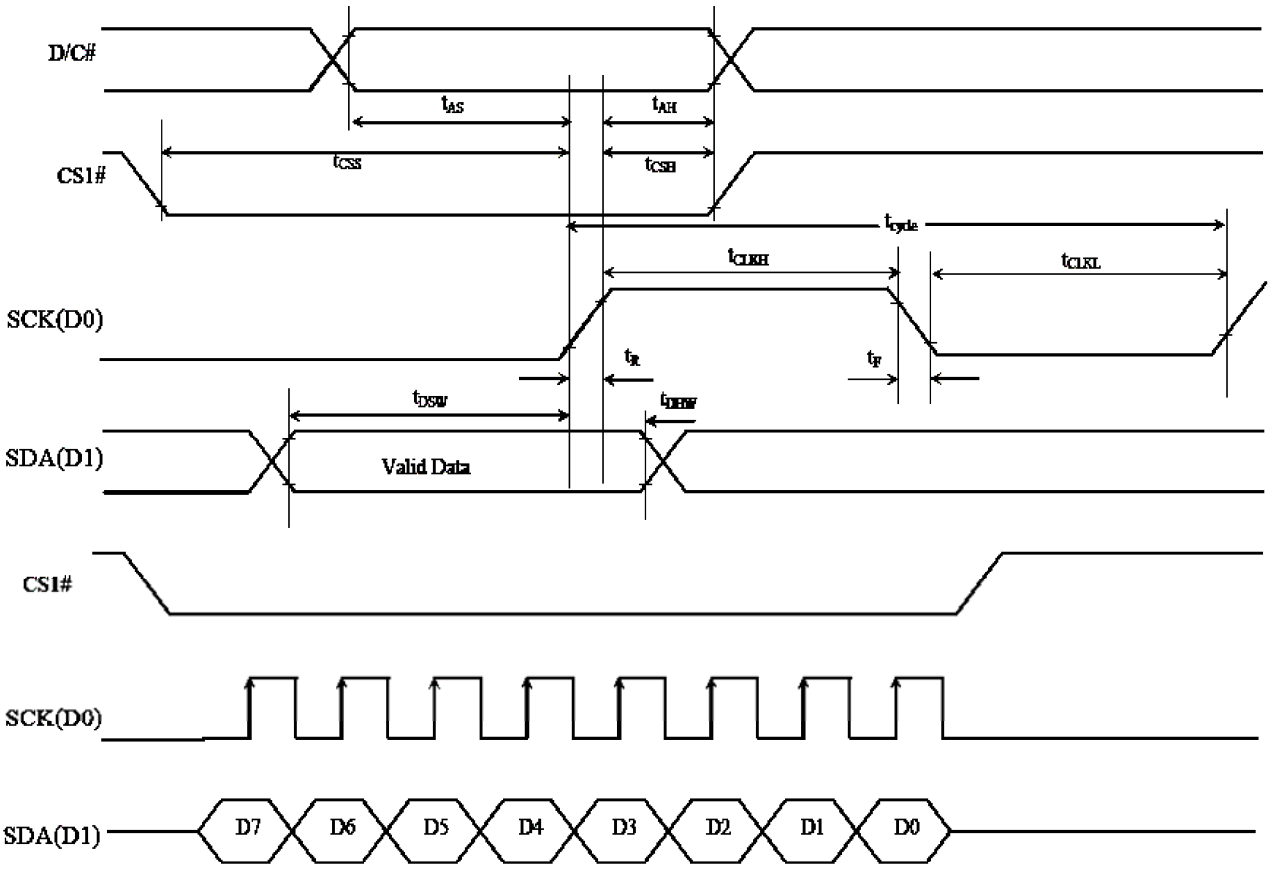
T_A = -35 to 85°C

$V_{DD} = V_{CI} = V_{DDIO}$ = 2.4V to 3.5V

4-wires Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	60	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
T_{CLKL}	Clock Low Time	30	-	-	ns
T_{CLKH}	Clock High Time	30	-	-	ns
t_{CSS}	Chip Select Setup Time (for D7 input)	30	- -	- -	ns
t_{CSH}	Chip Select Hold Time (for D0 input)	30	- -	- -	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

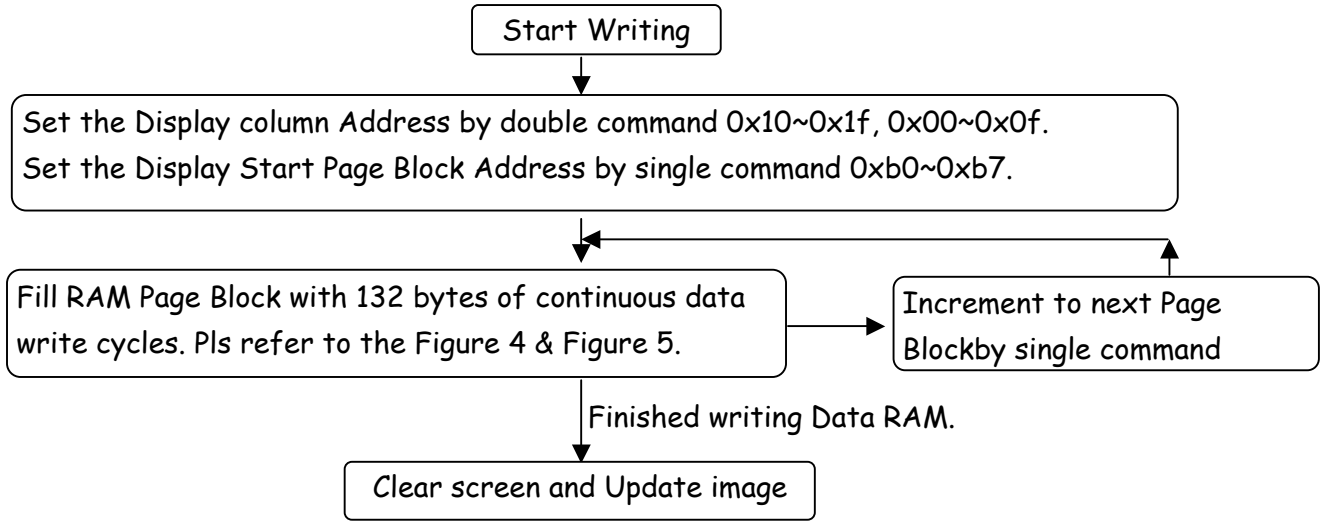
4-wires Serial Interface Timing Characteristics



(4) Clear Screen and Update image:

1) VA clear repeat times	command	0x93	Clear Screen
	command	0x01	
2)VA idle repeat times	command	0x94	
	command	0x01	
3)AA clear repeat times	command	0x95	
	command	0x01	
4)AA idle repeat times	command	0x96	
	command	0x01	
5)Driving repeat times	command	0x97	
	command	0x00	
6)Set the Driving scheme	command	0x32	
	command	0x21	
7)Driving update command	command	0x31	
8) VA clear repeat times	command	0x93	Update image
	command	0x00	
9)VA idle repeat times	command	0x94	
	command	0x00	
10)AA clear repeat times	command	0x95	
	command	0x00	
11)AA idle repeat times	command	0x96	
	command	0x00	
12)Driving repeat times	command	0x97	
	command	0x01	
13)Set the Driving scheme	command	0x32	
	command	0x20	

(5) Write Data RAM:



Note:

1) Writing Data to Graphic Display Data RAM involves **command** and **data** writes -->pls refer to Fig. 3.

2) Mapping to pixels of Graphic Display Data RAM(GDDRAM) ---->pls refer to Fig. 4, 5, & 6.

3) Please note that Each byte of pixel data is mapped to a vertical column of 8 bits (Fig 4).

4) Please note that all 132 columns of data must be written before advancing to next page block (Fig 5).

Figure 4 Enlargement of GDDRAM (No COM re-mapping and column-remapping)

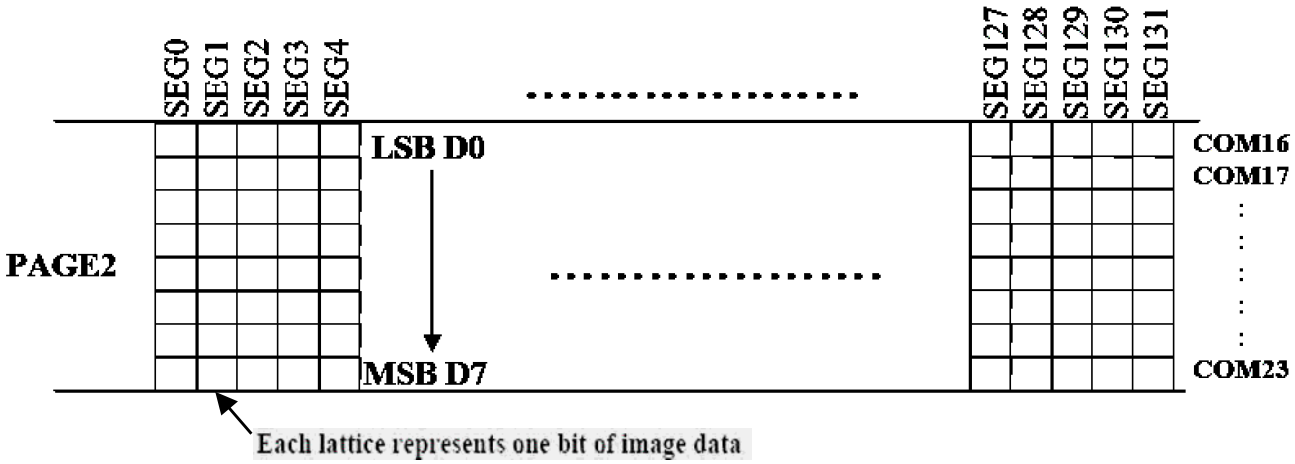


Figure 5 Address Pointer Movement of Horizontal addressing mode

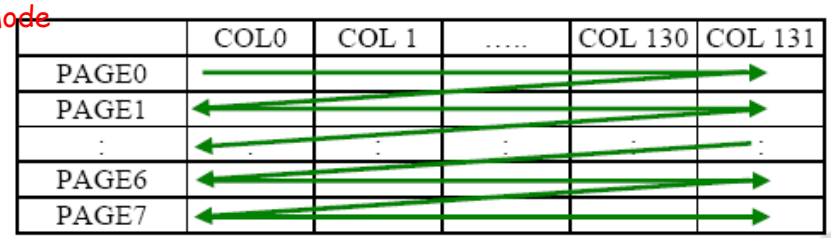
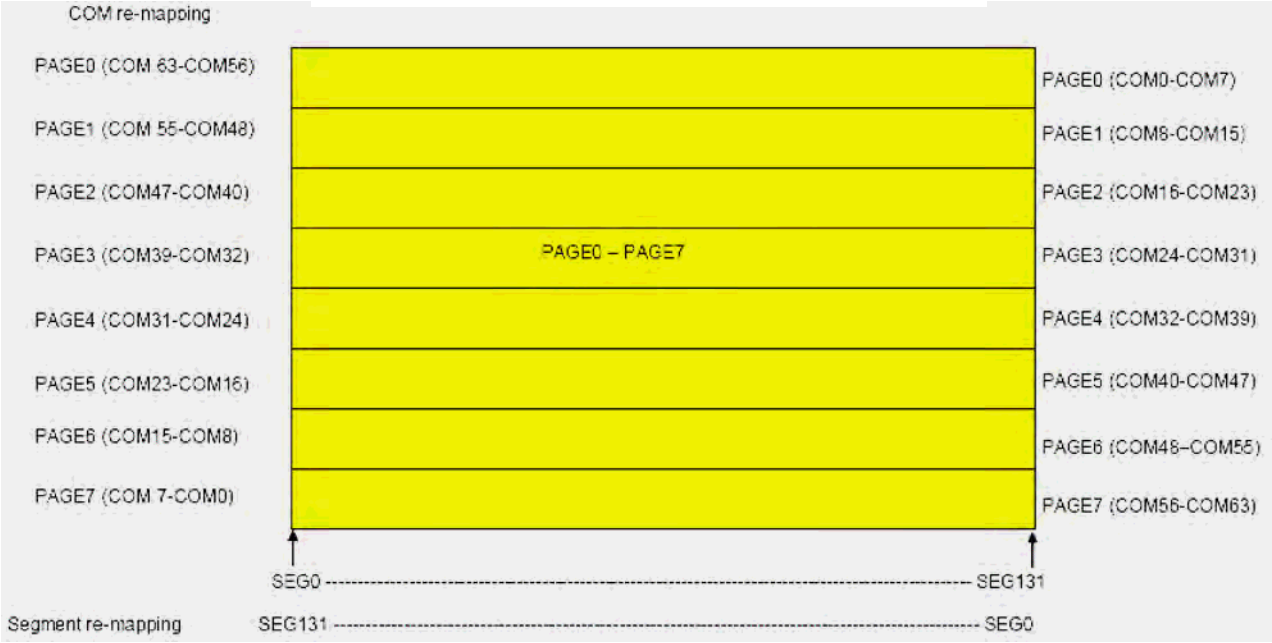


Figure 6 GDDRAM pages structure Module



(6) To enter Sleep Mode:

1) Disable Booster and High Volt Buffer	command	0x2a
2) Disable the Bias Driven	command	0xe9
	command	0x00
3) Disable the OSC	command	0xf6
	command	0x00
4) Disable the Analog Circuitry	command	0xa3
	command	0x00
5) Analog Control Auto OFF	command	0xa9
	command	0x00
6) Driving update command	command	0x31

Remark:

Sleep Mode should be used if Vdd cannot be powered off.

For best power savings, Vdd should be "Powered off"

(7) Partial Scan

1) set the display offset	command	0xd3
	command	(0x40-offset)
3) Set the multiplex ratio(partial high)	command	0xa8
	command	partial high
4) Set display startline	command	0x40 + startline(first line of the start page)
5) Driving update command	command	0x31

Example:Display a partial (from Com16 to Com36)

Define some partial scan parameter:

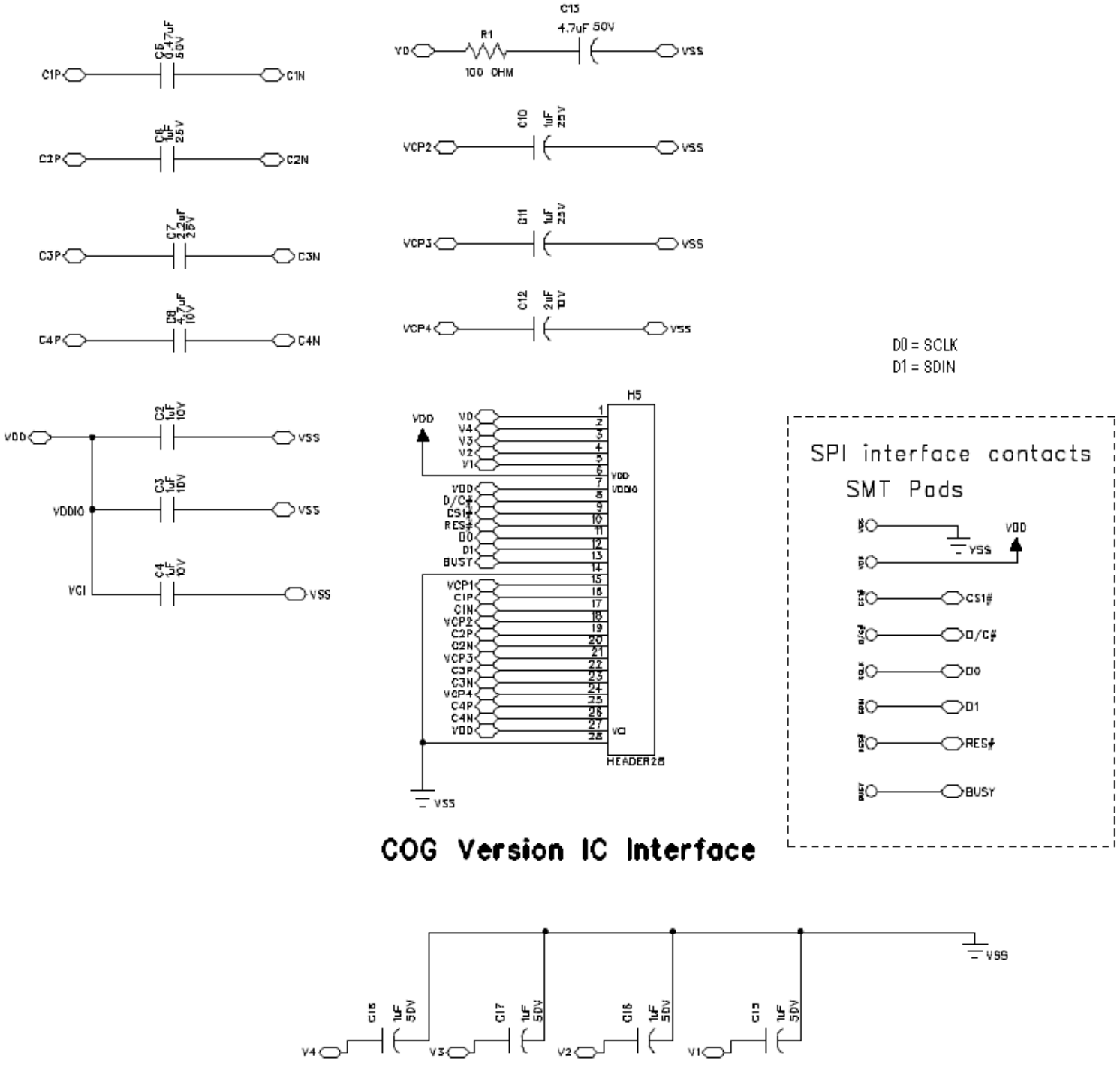
1) partial high = 0x14 (20 -->Com36-Com16)

2) scan_start page:--> the third page (Page 2) scan_end page: --> the fifth page (page 4)

3) offset = 0x1b (To move display from away Com0 by 27 Com_lines)

4) startline = 0x10 (C16-->the first line of the start page)

(8) Schematic:



COG Version IC Interface

(9) Electronic character:

	Status	Min	Type	Max	Unit
Vdd:	Active	3.1	3.3	3.5	V
Idd:	Active	-	0.4	0.5	mA
Vci	Active	Vdd	-	3.5	V
Ici	Active	-	2.1	3.0	mA
Vlcd:	Active	-	24	-	V
Idd	Sleep	-	-	5.0	uA
Ici	Sleep	-	-	5.0	uA