iPlay™

Media Player Controller

MP650UCG
Datasheet

Revision 0.95

2010-03-24

Magic Pixel Inc.

Revision History

Date	Revision	Description
Nov. 10. 2009	0.9	Initial Draft
Mar. 23, 2010	0.95	1. Update General Description and Feature list 2. Correct FGPIO index for FXD_RB pin of sec. 4.2 3. Supplement ADC_IN3~0 pin descriptions of sec. 4.2 4. Supplement power-on strap descriptions of sec. 4.3.1 5. Supplemental descriptions for boot-up configurations of sec. 5.1 6. Revise IDU function description of sec. 5.5 7. Revise Operating conditions and DC characteristics of Chapter 6

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1 General Description

The MP650UCG is a highly-integrated SOC (System-On-Chip) that's suitable for various multimedia applications like digital picture frame, media player and etc. It is capable of real-time decoding for various audio, video and image contents. A high-performance JPEG engine is included. A variety of JPEG data formats are supported. The embedded Video engine supports a variety of video compression standards, including MPEG-1/2/4 and H.264. It also supports Sorenson Spark FLV format for internet video. A flexible Image Processing Unit is built in to support high-quality image and color processing. It also includes a Special Effect controller to support various image effects in real time.

A 32-bit RISC CPU is built in to allow flexible system control. Proprietary instructions are included to improve performance and save power of S/W audio codec. A boot ROM which supports booting from NAND Flash or SD card is embedded. External NOR Flash for code storage is not needed. However, booting from Serial NOR Flash is also supported. The Serial NOR Flash can also be used as data storage in either boot-up scheme. An effective DMA and SDRAM/DDR controller is specially designed to optimize memory bandwidth efficiency.

A Stereo Audio DAC & Line Out Driver are integrated. I2S digital interface is also supported to utilize external audio codec to extend audio functions. The user can playback MP3, WMA as the background music when playing Slide-Show.

MP650UCG provides a versatile hardwired interface to support most popular memory card standards, including Compact Flash, SD/ mini SD/ Micro SD (It can support SD2.0 for SDHC specification), MMC/RS-MMC, xD, Memory Stick/Pro/**MSPROHG**. It offers the maximum flexibility to the customer. Secondary SD interface is included for peripheral, or SD card expansion.

The NAND Flash controller built into MP650UCG is equipped with flexible timing and parameter adjustment. The programmable configurations are designed to cover varieties of SLC/MLC/TLC NAND Flash in not only the existing technology, but also the future ones. As NAND Flash technology advances, it also demands higher bits ECC capability due to higher data error probability. To satisfy this requirement, MP650UCG has included a configurable ECC controller that supports up to 24-bit BCH ECC per 1KB.

Various display output formats, including CCIR-601/656/709, RGB-666/656, serial RGB, are supported by the Display Controller. It also includes a digital Timing Controller (TCON) with flexible timing configuration for glue-less panel connection.

2 sets of PWM are supported for external voltage boosters, which can be used as panel VGL/VGH and backlight drivers.

For data transfer to/from PC/Pict-Bridge enabled printer, it provides both USB and popular UART interfaces. It includes dual USBOTG high-speed controllers which are compliant with the USB 2.0 standard. It enables high-speed communications with a variety of hosts or devices, like PC, Camera, Printer and etc.

For flexible peripheral control and user interface, it provides several GPIOs. Most function pins can also be configured as GPIO. It also includes an IR (Infra-Red) controller supporting NEC Button and Remote Point Mouse protocols. I2C master and slave functions are supported to facilitate peripheral control and extend system functions. Several ADC are included to support various information inputs, like key control, battery detection, and etc.

With abundant features, superior performance and quality and highly integrated peripheral support, MP650UCG provides a best cost-effective solution for media player applications.

2 Features

- ■ **Power**
  - ➢ Dual Power. 1.2V for core, 3.3V/2.5V for I/O, 3V for RTC

- ■ **Image Processing Unit**
  - ➢ Hardware scaling engine to scale up and down images for resolution conversion
  - ➢ Configurable Edge detection and sharpness enhancement
  - ➢ RGB Color management engine with 24 independent color angles
  - ➢ RGB Color management SW tool to allow independent skin tone / preference colors setting
  - ➢ YCbCr Color Control with 256 regions independent color hue adjustment
  - ➢ Dual image windows overlay
  - ➢ De-interlacing for interlaced video (Up to D1@60 field/sec)
  - ➢ Hardware special photo effect controller.(High contrast, Color Mix, Black/White, Comic-style)

- ■ **JPEG Codec**
  - ➢ Support image resolution up to 64K x 64K for decoding , up to 8K x 8K for encoding
  - ➢ High speed JPEG compression and decompression (>40M Pixel/sec in 100MHZ)
  - ➢ Support JPEG decoding input formats : YCbCr 422h/422v/444/420, Y-only, 1/2/3/4-component Raw Data with 2-Huff, 2-Q tables at max
  - ➢ Support JPEG encoding output formats : YCbCr 422h
  - ➢ Support programmable image sub-sampling down to 1/8 ratio in H and V after JPEG decompression
  - ➢ Support HW image rotation (90/-90/180 degree) / Zoom In / Panning.
  - ➢ Picture Luma /Chroma statistics histogram for adaptive image processing

- ■ **Audio/Video decoding HW accelerator**
  - ➢ Support MPEG Audio Layer 1, 2, MP3, WMA, OGG, AAC_LC, AMR audio decoding.
  - ➢ Full bit-rate support for MP3, WMA
  - ➢ Hardware video decoding engine for H.264, MPEG-1,2,4,M-JPEG, H.263 & Flash Video(FLV-Sorenson Spark)
    - ● **H.264 1280x720p@30 frame/sec**
      - ✓ Profile Support: Baseline, Main & High profiles
      - ✓ Level Support : Level 1.0~3.1
    - ● **MPEG-4 1280x720p@30 frame/sec**
      - ✓ Profile Support: Simple & Advanced Simple profiles
      - ✓ Level Support : Level 0~5
    - ● **FLV(Sorenson Spark) 1280x720p@30 frame/sec**

- **MPEG-1 1280x720@30 frame/sec**
- **MPEG-2 1280x720@30 frame/sec**
  - ✓ Profile Support: Baseline, Main profile
  - ✓ Level Support : Low & Main levels
- **H.263 1280x720p@30 frame/sec**
  - ✓ Profile Support: Profile 0
  - ✓ Level Support : Level 10~70
- **Motion-JPEG 1280x720p@30 frame/sec**
- ** DDR-I is necessary for 1280x720p video decoding*

■ Memory Interface

- ➢ Support DDR-I up to 64MB (16bit data bus), 166MHZ
- ➢ Support SDRAM up to 32MB (16bit data bus), 166MHZ
- ➢ SPI NOR flash support, 1-bit with max capacity 4MB

■ Multiple Boot up methods

- ➢ Boot from SPI NOR flash
- ➢ Boot from embedded ROM
- ➢ Loader and code from NAND in user mode
- ➢ Loader and code from SD card for production test mode
- ➢ Support In System (NAND) Programming (ISP)

■ Memory Card/NAND Flash Interface

- ➢ Support Security Disk (SD1.2/2.0), Multi-Media Card (MMC, MMC4.0/3.2),Memory Stick Pro & 8 bit mode MSPROHG, xD Picture Card(1.0/1.1)
- ➢ Support Compact Flash (2.0/3.0/4.0/4.1)
- ➢ Support SLC/MLC/TLC type NAND Flash memory with page size 512B, 1K/2K/4K and 8KB
- ➢ Programmable ECC with Hamming 1 bit and BCH - 8/12/16-bit-ECC per 512-byte and 24-bit ECC per 1K-byte for 3X nm NAND Flash (3-bit per cell)
- ➢ Support auto page read and write, including FTL, ECC & data, for NAND Flash access to reduce SW overhead
- ➢ Support 3,4,5 and 6 NAND row address cycles, support 2-die NAND chip
- ➢ Support multi-sector DMA and deep FIFOs for better through-put
- ➢ Support card-to-card and card-to/from-NAND copy.
- ➢ Support 2nd SD Card or SDIO (Independent DMA and controller)

■ Audio Interface

- ➢ Embedded Stereo Audio DAC with max 48KHz
- ➢ Embedded Stereo Line out driver
- ➢ I^{2}S digital interface for external audio Codec

■ **USB Interface**

➢ Dual USB OTG 2.0 ports for versatile USB dongle applications

➢ Support Direct Print function (Pict-Bridge)

➢ Power saving control to comply with USB spec.

➢ Support uploading and downloading capability

➢ Support USB Mass Storage Class for both High Speed Device and High Speed Host functions

■ **Display Interface**

➢ Supported digital output format : CCIR-601/656/709, RGB-666/656, serial RGB

➢ Support digital input format : XRGB-888 , RGB-888, YCbCr 444/422

➢ Output Resolution up to 1024x768 with SDRAM, and 1280x800 or 1366x768 with DDR

➢ Independent RGB gamma adjustment (32-step Piecewise-linear)

➢ Programmable (Spatial or temporal) dithering for RGB666 panels

➢ Embedded Digital TCON for up to 800x600 resolution

➢ OSD engine supports 2-, 4- or 8-bit palette-indexed Bit-mapped On Screen Display (OSD).

➢ One programmable Color Space Converter

■ **LDO (Charge Pump for Panel)**

➢ Two set of Max 1.5Mhz PWM with driver transistor protection support for VGH/VGL & backlight LED driver

■ **RTC**

➢ 3.0V single voltage supply with 64-bits storage registers built-in

➢ Calibration adjustment support

➢ Alarm function and output pin support

■ **Low speed ADC**

➢ 4 ADC input ports support for key control, battery detection or other purposes.

➢ Maximum sample rate: 3.3Msps @20MHz clock

■ **Power Management and EMI**

➢ 4 phase-locked loop (PLL) on chip for versatile clocking applications

➢ Patented Spread Spectrum function inside the PLL to reduce EMI peaks

➢ Dedicated clock for USB

➢ Support deep power down mode

➢ Support Alarm trigger system wake up or GPIO wake-up

■ **CPU**

➢ Embedded high performance 32-bit RISC processor with 8KB instruction cache and 2KB data cache.

➢ On chip 24KB SRAM and 512MB memory addressing capability

➢ Support up to 166MHz system & CPU clock

➢ MAC Unit with MPX audio accelerator built into CPU core

■ **I2C/UART/IR/Timer/GPIO**

➢ Dual UART ports with one port supporting flow control, max baud rate is 8Mbps

➢ Support generic DMA for memory fill and copy actions (linear or 2D mode) and prioritized DMA channels support

➢ I2C Master interface support

➢ I2C Slave interface support

➢ IR support with NEC and Remote Point Mouse Protocol

➢ 6 timers with 32 bits counters

➢ Flexible GPIO control for variety of peripheral control

■ **Package**

➢ 216-pin LQFP (24mm x 24mm x 1.4mm)

■ **System Development Kit & Software Support**

➢ Support real time OS : u-iTron 4.0

➢ Reference PCB Design Schematics and Layout Guides

➢ System Application Notes

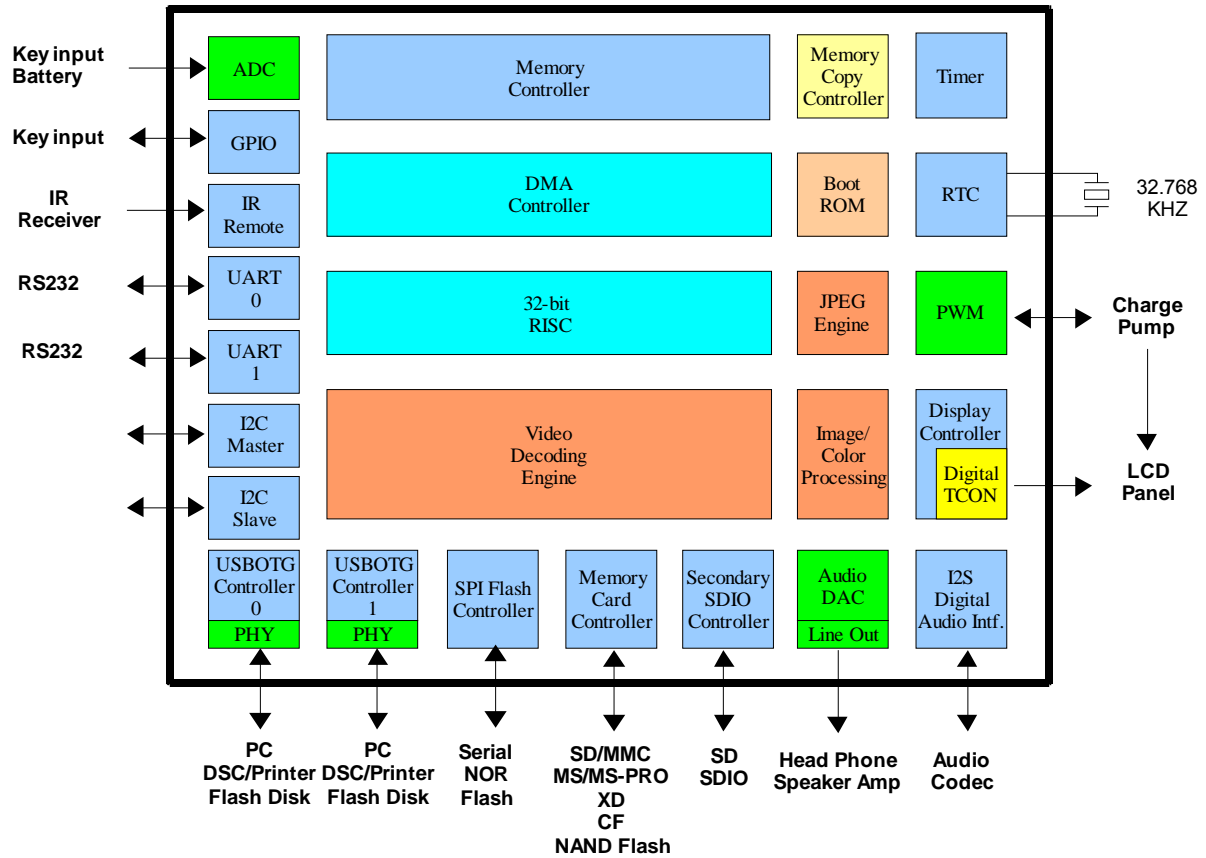➢ UI (User Interface) Builder

3   Block diagram

Fig. 3-1 MP650UCG Block Diagram

4 Pin Assignment

4.1 Pin Diagram

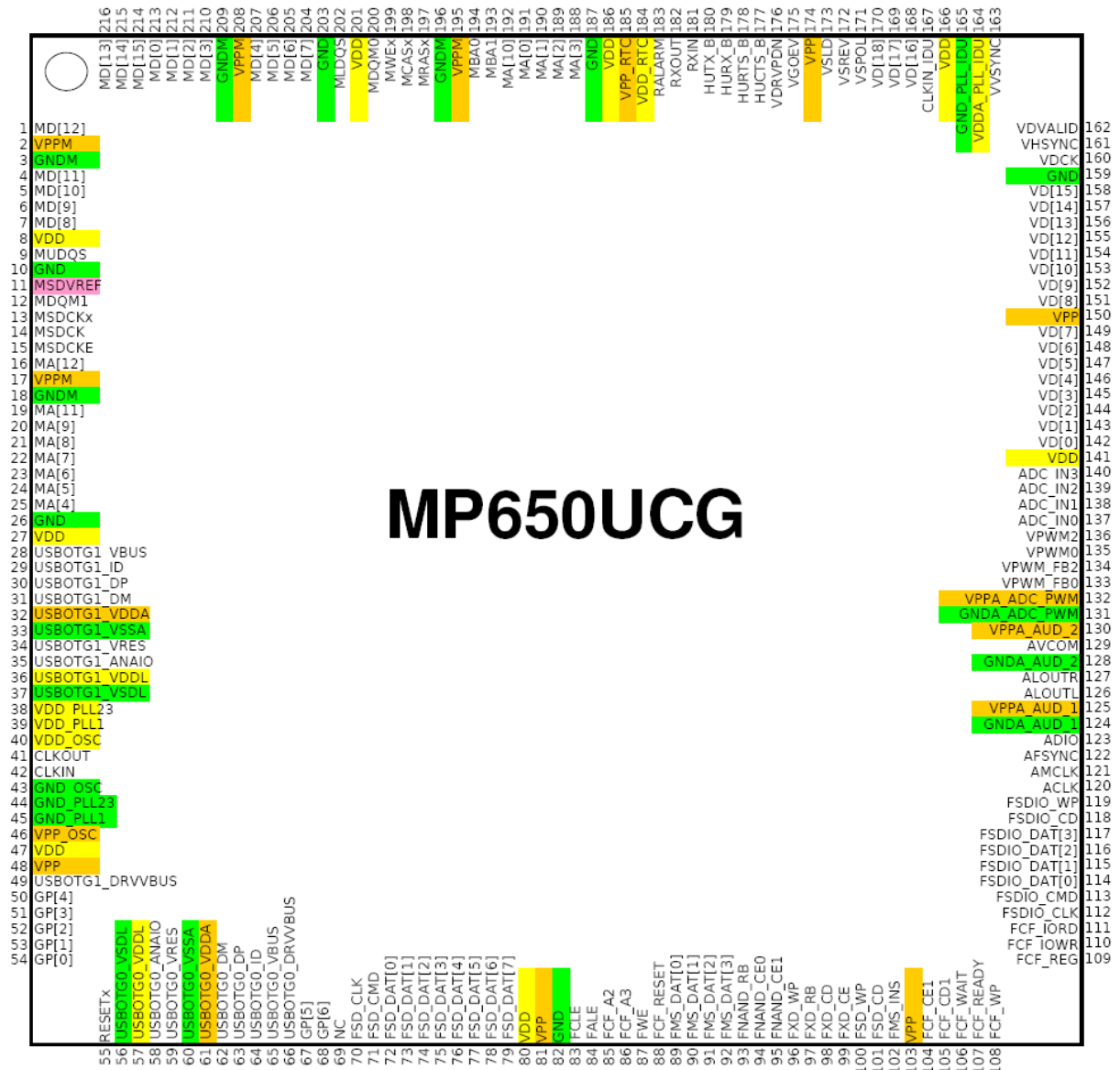**Fig. 4-1 MP650UCG Block Diagram**

4.2 Pin Description

Pin Name	Pin Number	I/O	Description
DRAM Interface			
MD[15:0]	214, 215, 216,1, 4, 5, 6, 7, 204, 205, 206, 207, 210, 211, 212, 213	I/O	SDRAM/DDR Data
MA[12:0]	16, 19, 192, 20, 21 22, 23, 24, 25, 188, 189, 190, 191	O	SDRAM/DDR Address
MBA0	194	O	SDRAM/DDR Bank Address bit 0
MBA1	193	O	SDRAM/DDR Bank Address bit 1
MRASx	197	O	SDRAM/DDR RASx, Row Address Strobe
MCASx	198	O	SDRAM/DDR CASx, Column Address Strobe
MWEx	199	O	SDRAM/DDR WEx
MDQM0	200	O	SDRAM/DDR low byte Data Mask, for MD[7:0]
MDQM1	12	O	SDRAM/DDR high byte Data Mask, for MD[15:8]
MSDCK	14	O	SDRAM/DDR Clock
MSDCKx	13	O	DDR Inverted Clock
MSDCKE	15	O	SDRAM/DDR Clock Enable
MLDQS	202	O	DDR low-byte Data Strobe, for MD[7:0]
MUDQS	9	O	DDR high-byte Data Strobe, for MD[15:8]
MSDVREF	11	P	DDR Voltage Reference. Set to VPPM/2 for proper operation
Memory Card and NAND Flash Interface			
FSD_CLK	70	I/O	It's the clock signal CLK for SD/MMC and MS/MS-PRO. It can also be configured as general input/output, FGPIO[0]. As SPI Serial Flash is selected, it's the serial clock output, SCLK.
FSD_CMD	71	I/O	It's a multi-function pin. It's the CMD signal for SD/MMC. It's the RE# output for NAND/xD. When Compact Flash is selected, it's the OE#. It can also be configured as general input/output, FGPIO[1].

FSD_DAT[7:0]	79 ~ 72	I/O	It's the data bus for NAND Flash, xD, 8-bit MMC and Compact Flash. For SD, and 4-bit MMC, only FSD_DAT[3:0] is effective. For MS-PRO HG, {FSD_DAT[7:4], MS_DAT[3:0]} forms the 8-bit data bus. When configured as GPIO, they are corresponding to FGPIO[9:2]. As SPI Serial Flash is selected, the corresponding pins are remapped as below: *FSD_DAT[4] – Serial data input, SI from Serial Flash* *FSD_DAT[6] – WP# output to Serial Flash* *FSD_DAT[7] – HOLD# output to Serial Flash*
FWE	87	I/O	It's the WE# signal for NAND Flash, xD and Compact Flash. It can also be configured as general input/output, FGPIO[10].
FCLE	83	I/O	It's the Command Latch Enable signal, CLE, for NAND Flash and xD. When Compact Flash is selected, it's the bit 0 of Address output, A0. When configured as general input/output, it's corresponding to FGPIO[11].
FALE	84	I/O	It's the Address Latch Enable signal, ALE, for NAND Flash and xD. For MS/MS-PRO, it's the BS signal. When Compact Flash is selected, it's the bit 1 of Address output,A1. When configured as general input/output, it's corresponding to FGPIO[12].
FCF_A2	85	I/O	It's the bit 2 of Address output, A2,for Compact Flash. When configured as general input/output, it's corresponding to FGPIO[13].
FCF_A3	86	I/O	It's the bit 3 of Address output, A3,for Compact Flash. When configured as general input/output, it's corresponding to FGPIO[14].
FCF_RESET	88	I/O	It's the RESET# output for Compact Flash. When configured as general input/output, it's corresponding to FGPIO[15].
FMS_DAT[3:0]	92 ~ 89	I/O	It's the data bus [3:0] for MS and MS-PRO. For MS-PRO HG, it's the data bus [3:0]. The high nibble data bus [7:4] come from FSD_DAT[7:4]. When configured as general input/output, it's corresponding to FGPIO[19:16].

FCF_WAIT	106	I/O	It's the WAIT# output for Compact Flash. When configured as general input/output, it's corresponding to FGPIO[20].
FNAND_RB	93	I/O	It's the RDY/BSY# signal for NAND Flash. When pulled low, it indicates that the NAND Flash is busy and not be able to accept new commands. When configured as general input/output, it's corresponding to FGPIO[21].
FNAND_CE0	94	I/O	It's the Chip Enable output 0 for NAND Flash. It's active low. It's also the Chip Enable output when SPI Serial Flash is selected. When configured as general input/output, it's corresponding to FGPIO[22].
FNAND_CE1	95	I/O	It's the 2nd Chip Enable output for NAND Flash. It's active low. When configured as general input/output, it's corresponding to FGPIO[23]
FXD_CE	99	I/O	It's the Chip Enable output for xD. It's active low. When configured as general input/output, it's corresponding to FGPIO[24].
FCF_CE1	104	I/O	It's the R/W access Enable output for Compact Flash. It should be connected to CE0# of the Compact Flash. When configured as general input/output, it's corresponding to FGPIO[25].
FCF_CD1	105	I/O	It's the Card Detection input for Compact Flash. It can be connected to either CD0# or CD1# of the Compact Flash. It's active low. When configured as general input/output, it's corresponding to FGPIO[26].
FXD_CD	98	I/O	It's the Card Detection input for xD. It's active low. When configured as general input/output, it's corresponding to FGPIO[27].
FSD_CD	101	I/O	It's the Card Detection input for SD/MMC. It's active low. When configured as general input/output, it's corresponding to FGPIO[28].
FMS_INS	102	I/O	It's the Card Insertion input for MS/MS-PRO. It indicates that the MS/MS-PRO card is plugged in when asserted low. When configured as general input/output, it's corresponding to FGPIO[29].

FSD_WP	100	I/O	It's the Write Protect input for SD/MMC. When pulled low, it indicates that the SD/MMC card is prohibited from write access. When configured as general input/output, it's corresponding to FGPIO[30].
FXD_WP	96	I/O	It's the Write Protect output for xD. Pull it to low to prohibit xD card from write access. As SPI Serial Flash is selected, it's the serial data output to the Flash. When configured as general input/output, it's corresponding to FGPIO[31].
FCF_WP	108	I/O	It's the Write Protect input for the Compact Flash interface. When configured as general input/output, it's corresponding to FGPIO[32].
FCF_REG	109	I/O	It's the REG# output for Compact Flash. When configured as general input/output, it's corresponding to FGPIO[33].
FCF_IOWR	110	I/O	It's the IOWR# output for the Compact Flash interface. It's not effective if memory mode is selected for Compact Flash. When configured as general input/output, it's corresponding to FGPIO[34].
FCF_IORD	111	I/O	It's the IORD# output for the Compact Flash interface. It's not effective if memory mode is selected for Compact Flash. When configured as general input/output, it's corresponding to FGPIO[35].
FSDIO_CLK	112	I/O	It's the clock output for the 2nd SD interface. When configured as general input/output, it's corresponding to FGPIO[36].
FSDIO_CMD	113	I/O	It's the CMD signal for the 2nd SD interface. When configured as general input/output, it's corresponding to FGPIO[37].
FSDIO_DAT[3:0]	117 ~ 114	I/O	It's the data bus for the 2nd SD interface. When configured as general input/output, it's corresponding to FGPIO[41:38].
FCF_READY	107	I/O	It's the READY input for Compact Flash. When configured as general input/output, it's corresponding to FGPIO[42].
FSDIO_CD	118	I/O	It's the Card Detection input for the 2nd SD interface. When configured as general input/output, it's corresponding to FGPIO[43].

FSDIO_WP	119	I/O	It's the Write Protect input for the 2nd SD interface. When configured as general input/output, it's corresponding to FGPIO[44].
FXD_RB	97	I/O	It's the RDY/BSY# signal for xD. When pulled low, it indicates that the xD card is busy and not be able to accept new commands. When configured as general input/output, it's corresponding to FGPIO[45].
Display Interface			
VD[7:0]	149 ~ 142	I/O	For CCIR-656, it's the 8-bit pixel output. For CCIR-601, it's the 8-bit luma (Y) output. If RGB-888 is selected, it's the R[7:0] output. If built-in TCON is selected, VD[7:6] is the G[1:0], and VD[5:0] the R[5:0] output of RGB-666. If Serial RGB is selected, it's the 8-bit pixel output. When configured as general input/output, it's corresponding to VGPIO[7:0].
VD[15:8]	158 ~ 151	I/O	For CCIR-601, it's the 8-bit Chroma (C) output. If RGB-888 is selected, it's the G[7:0] output. If built-in TCON is selected, VD[11:8] is the G[5:2], and VD[15:12] the B[3:0] output of RGB-666. When configured as general input/output, it's corresponding to VGPIO[15:8].
VD[16]	168	I/O	If RGB-888 is selected, it's the B[0] output. If built-in TCON is selected, it's the B[4] output of RGB-666. When configured as general input/output, it's corresponding to VGPIO[16].
VD[17]	169	I/O	If RGB-888 is selected, it's the B[1] output. If built-in TCON is selected, it's the B[5] output of RGB-666. When configured as general input/output, it's corresponding to VGPIO[17].
VD[18]	170	I/O	If RGB-888 is selected, it's the B[2] output. If built-in TCON is selected, it can be configured as the Gate Driver Polarity Select, GPOL. When configured as general input/output, it's corresponding to VGPIO[18].
VDCK	160	I/O	It's the pixel clock output for all types of panels. When configured as general input/output, it's corresponding to VGPIO[19].

VHSYNC	161	I/O	It's the HSYNC output for CCIR-601, RGB-888 and Serial RGB. If built-in TCON is selected, it can be configured as the Horizontal Start Pulse, STH. When configured as general input/output, it's corresponding to VGPIO[20].
VDVALID	162	I/O	It's the Data Valid output, DVALID, for CCIR-601, RGB-888 and Serial RGB. If built-in TCON is selected, it can be configured as the Gate Driver Start Pulse, STV. When configured as general input/output, it's corresponding to VGPIO[21].
VVSYNC	163	I/O	It's the VSYNC output for CCIR-601, RGB-888 and Serial RGB. If built-in TCON is selected, it can be configured as the Gate Driver Shift Clock, CKV. When configured as general input/output, it's corresponding to VGPIO[22].
VSPOL	171	I/O	If RGB-888 is selected, it's the B[3] output. If built-in TCON is selected, it can be configured as the Source Driver Polarity Select, SPOL . When configured as general input/output, it's corresponding to VGPIO[23].
VSREV	172	I/O	If RGB-888 is selected, it's the B[4] output. If built-in TCON is selected, it can be configured as the Source Driver Data Reverse Control, SREV . When configured as general input/output, it's corresponding to VGPIO[24].
VSLD	173	I/O	If RGB-888 is selected, it's the B[5] output. If built-in TCON is selected, it can be configured as the Source Driver Latch Pulse and Output Enable, SLD . When configured as general input/output, it's corresponding to VGPIO[25].
VGOEV	175	I/O	If RGB-888 is selected, it's the B[6] output. If built-in TCON is selected, it can be configured as the Gate Driver Output Enable, GOEV. When configured as general input/output, it's corresponding to VGPIO[26].
VDRVPDN	176	I/O	If RGB-888 is selected, it's the B[7] output. If built-in TCON is selected, it can be configured to output with required timing. When configured as general input/output, it's corresponding to VGPIO[27].

CKIN_IDU	167	I/O	It can be used as the clock input to PLL_IDU. When configured as general input/output, it's corresponding to VGPIO[28].
Panel Power Interface			
VPWM0	135	IO	By default, it's the primary PWM output for external panel power charge pump, like VGL/VGH. When configured as Alternative function 1, it's a general input/output, PGPIO[0]. When configured as Alternative function 2, it's the I2C Master clock output.
VPWM_FB0	133	AIO	By default, it's the voltage divider analog input to the primary PWM generator. PWM output will be enabled only if the input voltage level is greater than internal bias, which is typically set to 1.2V. It can also be configured to function as digital pin. When configured as Alternative function 1, it's a general input/output, PGPIO[1]. When configured as Alternative function 2, it's the I2C Master data input/output.
VPWM2	136	IO	By default, it's the secondary PWM output for external panel power charge pump, like LED Backlight. When configured as Alternative function 1, it's a general input/output, PGPIO[2]. When configured as Alternative function 2, it's the I2C Slave clock output.
VPWM_FB2	134	AIO	By default, it's the voltage divider analog input to the secondary PWM generator. PWM output will be enabled only if the input voltage level is greater than internal bias, which is typically set to 1.2V. It can also be configured to function as digital pin. When configured as Alternative function 1, it's a general input/output, PGPIO[3]. When configured as Alternative function 2, it's the I2C Slave data input/output.
USB Interface			
USBOTG0_VRES	59	AIO	External resistor connection for current reference of USBOTG0 PHY.
USBOTG0_VBUS	65	AIO5V	5V VBUS for USBOTG0.
USBOTG0_DM	62	AIO	Negative output channel of USBOTG0 that is connected to the serial USB cable.
USBOTG0_DP	63	AIO	Positive output channel of USBOTG0 that is connected to the serial USB cable.
USBOTG0_ID	64	AIO	USB ID pin of mini-AB receptacle for USBOTG0.
USBOTG0_ANAIO	58	AIO	USBOTG0 PHY debug pin.

USBOTG0_DRVVBUS	66	I/O	By default, it's the USBOTG0 5V power driving enable. It can also be used as GPIO, OGPIO[0], by configuring to Alternative function 1.
USBOTG1_VRES	34	AIO	External resistor connection for current reference of USBOTG1 PHY.
USBOTG1_VBUS	28	AIO5V	5V VBUS for USBOTG1
USBOTG1_DM	31	AIO	Negative output channel of USBOTG1 that is connected to the serial USB cable.
USBOTG1_DP	30	AIO	Positive output channel of USBOTG1 that is connected to the serial USB cable.
USBOTG1_ID	29	AIO	USB ID pin of mini-AB receptacle for USBOTG1.
USBOTG1_ANAIO	35	AIO	USBOTG1 PHY debug pin.
USBOTG1_DRVVBUS	49	I/O	By default, it's the USBOTG1 5V power driving enable. It can also be used as GPIO, OGPIO[1], by configuring to Alternative function 1.
GPIO Interface			
GP[0]	54	I/O	By default, it's the general input/output, GP[0]. It can also be used as the RX input of the primary UART. When Alternative function 3 is selected, it's the I2C Master clock output.
GP[1]	53	I/O	By default, it's the general input/output, GP[1]. When Alternative function 1 is selected, it's the TX output of the primary UART. When Alternative function 3 is selected, it's the I2C Master data input/output.
GP[2]	52	I/O	By default, it's the general input/output, GP[2]. It can also be configured as the CTS input of the primary UART. When Alternative function 3 is selected, it's the Timer 2 output which can be used to generate PWM signal. It can also be used as the IR input from external IR receiver.
GP[3]	51	I/O	By default, it's the general input/output, GP[3]. When Alternative function 1 is selected, it's the RTS output of the primary UART. When Alternative function 3 is selected, it's the Timer 3 output which can be used to generate PWM signal.
GP[4]	50	I/O	By default, it's the general input/output, GP[4]. When Alternative function 2 is selected, it's a buffer output of the 12MHZ clock input from the CLKIN pin.

GP[5]	67	I/O	By default, it's the general input/output, GP[5]. When Alternative function 2 is selected, it's Timer 4 output which can be used to generate PWM signal.
GP[6]	68	I/O	By default, it's the general input/output, GP[6]. When Alternative function 2 is selected, it's Timer 5 output which can be used to generate PWM signal.
Secondary UART Interface			
HURX_B	179	I/O	By default, it's a general input/output, UGPIO[4]. It can also be used as the RX input of the secondary UART.
HUTX_B	180	I/O	By default, it's a general input/output, UGPIO[5]. When Alternative function 1 is selected, it's the TX output of the secondary UART.
HUCTS_B	177	I/O	By default, it's a general input/output, UGPIO[6]. It can also be used as the CTS input of the secondary UART.
HURTS_B	178	I/O	By default, it's a general input/output, UGPIO[7]. When Alternative function 1 is selected, it's the RTS output of the secondary UART.
I2S Digital Audio Interface			
ACLK	120	I/O	By default, it's a general input/output, AGPIO[0]. When configured as Alternative function 1, it's the bit clock output to external audio codec.
AMCLK	121	I/O	By default, it's a general input/output, AGPIO[1]. When configured as Alternative function 1, it's the master clock input/output from/to external audio codec.
AFSYNC	122	I/O	By default, it's a general input/output, AGPIO[2]. When configured as Alternative function 1, it's the Frame Sync output to external audio codec.
ADIO	123	I/O	By default, it's a general input/output, AGPIO[3]. When configured as Alternative function 1, it's the data input/output from/to external audio codec.
Analog Audio Interface			
ALOUTL	126	AO	Left channel of Audio Line Output
ALOUTR	127	AO	Right channel of Audio Line Output
AVCOM	129	AIO	Analog reference voltage for the audio DAC. It's typically set to half of the audio power, VPPA_AUD.
Analog ADC Interface			

ADC_IN0	137	AIO	By default, it's the channel 0 ADC input.
			It can also be configured to function as digital pin. When configured as default digital function, it's a general input/output, KGPIO[0].
			If configured as Alternative function 1, it's the master clock input/output, AMCLK, from/to the external audio codec.
			When configured as Alternative function 2, it's the I2C Slave data input/output.
ADC_IN1	138	AIO	By default, it's the channel 1 ADC input.
			It can also be configured to function as digital pin. When configured as default digital function, it's a general input/output, KGPIO[1].
			If configured as Alternative function 1, it's the frame synchronization output, AFSYNC, to the external audio codec.
			When configured as Alternative function 2, it's the RX input of the primary UART.
ADC_IN2	139	AIO	By default, it's the channel 2 ADC input.
			It can also be configured to function as digital pin. When configured as default digital function, it's a general input/output, KGPIO[2].
			If configured as Alternative function 1, it's the audio data input/output, ADIO, from/to the external audio codec.
			When configured as Alternative function 2, it's the TX output of the primary UART.
ADC_IN3	140	AIO	By default, it's the channel 3 ADC input.
			It can also be configured to function as digital pin. When configured as default digital function, it's a general input/output, KGPIO[3].
			If configured as Alternative function 1, it's the RTC 1HZ clock output.
			When configured as Alternative function 2, it's the 3D_CLK output to 3D panels.
RTC Interface			
RXIN	181	I	It's the 32.768KHZ RTC Oscillator input
RXOUT	182	O	It's the 32.768KHZ RTC Oscillator output
RALARM	183	I/O	By default, it's the RTC Alarm output. It will be asserted when the RTC counter equals the RTC ALARM setting.
			It can also be configured as a general input/output.
System Interface			
RESETx	55	I	It's the hardware reset input, active low.
CLKIN	42	I	It's the 12MHZ main oscillator input.
CLKOUT	41	O	It's the 12MHZ main oscillator output.
Power/Ground			

VPPM	2, 17, 195, 208	P	It's the I/O power for SDRAM/DDR interface. It's separated from the other I/O powers. It's typically 3.3V for SDRAM, and 2.5V for DDR.
GNDM	3, 18, 196, 209	P	It's the I/O ground for SDRAM/DDR interface. It's separated from the other I/O ground.
USBOTG0_VDDA	61	P	It's the 3.3V analog power for USBOTG0 PHY.
USBOTG0_VSSA	60	P	It's the analog ground corresponding to 3.3V analog power for USBOTG0 PHY.
USBOTG0_VDDL	57	P	It's the 1.2V analog power for USBOTG0 PHY.
USBOTG0_VSDL	56	P	It's the analog ground corresponding to 1.2V analog power for USBOTG0 PHY.
USBOTG1_VDDA	32	P	It's the 3.3V analog power for USBOTG1 PHY.
USBOTG1_VSSA	33	P	It's the analog ground corresponding to 3.3V analog power for USBOTG1 PHY.
USBOTG1_VDDL	36	P	It's the 1.2V analog power for USBOTG1 PHY.
USBOTG1_VSDL	37	P	It's the analog ground corresponding to 1.2V analog power for USBOTG1 PHY.
VPP_OSC	46	P	It's the 3.3V I/O power for the 12MHZ main oscillator I/O.
VDD_OSC	40	P	It's the 1.2V core power for the 12MHZ main oscillator I/O.
VDD_PLL23	38	P	It's the 1.2V power for PLL_2 and PLL_3.
GND_PLL23	44	P	It's the analog ground for PLL_2 and PLL_3.
VDD_PLL1	39	P	It's the 1.2V power for PLL_1.
GND_PLL1	45	P	It's the analog ground for PLL_1.
VDDA_PLL_IDU	164	P	It's the 1.2V power for PLL_IDU.
GND_PLL_IDU	165	P	It's the analog ground for PLL_IDU.
VPPA_AUD_1	125	P	It's the 3.3V analog power for the audio DAC.
VPPA_AUD_2	130	P	It's the 3.3V analog power for the audio DAC.
GNDA_AUD_1	124	P	It's the analog ground corresponding to VPPA_AUD_1 for the audio DAC.
GNDA_AUD_2	128	P	It's the analog ground corresponding to VPPA_AUD_2 for the audio DAC.
VPPA_ADC_PWM	132	P	It's the 3.3V analog power for the ADCs and PWMs.
GNDA_ADC_PWM	131	P	It's the analog ground for the ADCs and PWMs.
VDD_RTC	184	P	It's the 1.2V power input for the RTC core. If internal RTC 3V-to-1.2V DC converter is enabled, it is used as external capacitor connection.
VPP_RTC	185	P	It's the dedicated I/O power for RTC.
VPP	48, 81, 103, 150, 174	P	3.3V digital I/O power
VDD	8, 27, 47, 80, 141, 166, 186, 201	P	1.2V digital core power
GND	10, 26, 82, 159, 187, 203	P	Digital ground

4.3 Pin Configuration

4.3.1 *Power-on Strap*

MP650UCG defines several power-on strap configurations through pins VD[7:0] and VHSYNC. The states of the power-on strap pins are latched by the rising edge of the internal delayed RESETx signal. They are then utilized by the chip itself or boot code to determine the key configurations for proper operation. Each power-on strap pin should be pulled up to VPP or down to GND through a resistor typically in 10K ohm.

Power-on Strap Pin	Function	Description
VD[0]	Reserved	Leave it floating or pull it down for proper operation
VD[1]	DRAM_Type	0 – SDRAM 1 – DDR SDRAM
VD[3:2]	DRAM_SIZE	2'b00 – 4Mb*16 2'b01 – 8Mb*16 2'b10 – 16Mb*16 2'b11 – 32Mb*16 → applicable only for DDR
VD[4]	INT_BOOT_SEL	Load software code from: 0 – SD Card 1 – NAND Flash
VD[7:5]	NF_ROW_CYC[2:0]	Number of NAND Flash Row Address Cycle = NF_ROW_CYC[2:0] + 1
VHSYNC	BTDEVICE	Boot up from: 0 – Internal ROM 1 – SPI Serial Flash

Note: 0 state means pull low to GND; 1 means pull high to VPP.

4.3.2 *SDRAM/DDR Interface*

Pin Name	SDRAM	DDR
MD[15:0]	DQ[15:0]	DQ[15:0]
MA[12:0]	A[12:0]	A[12:0]
MBA0	BA0	BA0
MBA1	BA1	BA1
MRASx	RAS#	RAS#
MCASx	CAS#	CAS#
MWEx	WE#	WE#
MDQM0	LDQM	LDQM
MDQM1	UDQM	UDQM
MSDCK	CLK	CLK
MSDCKx	-	CLK#
MSDCKE	CKE	CKE
MLDQS	-	LDQS
MUDQS	-	UDQS

The CS# input of the SDRAM and DDR should be pulled low to GND for proper operation.

4.3.3 *Memory Card Interface*

Pin Name	Default	Alt. Func. 1						SPI Flash	Pull H/L Config.
		CF (Memory mode)	SD_0	MMC	NAND	XD	MS		
FSD_CLK	FGPIO[0]		CLK	CLK			CLK	SCLK	H
FSD_CMD	FGPIO[1]	OE#	CMD	CMD	RE#	RE#			H
FSD_DAT[3:0]	FGPIO[5:2]	DAT[3:0]	DAT[3:0]	DAT[3:0]	DAT[3:0]	DAT[3:0]			H
FSD_DAT[7:4]	FGPIO[9:6]	DAT[7:4]		DAT[7:4]	DAT[7:4]	DAT[7:4]	DAT[7:4]	{HOLD#, WP#, -, SI}}	H
FWE	FGPIO[10]	WE#			WE#	WE#			H
FCLE	FGPIO[11]	A0			CLE	CLE			L
FALE	FGPIO[12]	A1			ALE	ALE	BS		L
FCF_A2	FGPIO[13]	A2							L
FCF_A3	FGPIO[14]	A3							L
FCF_RESET	FGPIO[15]	RESET							L
FMS_DAT[3:0]	FGPIO[19:16]						DAT[3:0]		L
FCF_WAIT	FGPIO[20]	WAIT#							H
FNAND_RB	FGPIO[21]				R/B#				H
FNAND_CE0	FGPIO[22]				CE0#			SCS#	H
FNAND_CE1	FGPIO[23]				CE1#				H
FXD_CE	FGPIO[24]					CE#			H
FCF_CE1	FGPIO[25]	CE1#							H
FCF_CD1	FGPIO[26]	CD1#							H
FXD_CD	FGPIO[27]					CD#			H
FSD_CD	FGPIO[28]		CD#	CD#					H
FMS_INS	FGPIO[29]						INS#		H
FSD_WP	FGPIO[30]		WP_IN#	WP_IN#					H
FXD_WP	FGPIO[31]					WP_OUT#		SO	L
FCF_WP	FGPIO[32]	WP_IN							H
FCF_REG	FGPIO[33]	REG#							H
FCF_IOWR	FGPIO[34]								H
FCF_IORD	FGPIO[35]								H
FCF_READY	FGPIO[42]	READY							H
FXD_RB	FGPIO[45]					R/B#			H

The built-in pull high/low for each pin is configurable and can be turned on or off by software.

The pin configuration of the secondary SD interface is summarized as below.

Pin Name	Default	Alt. Func. 1	Pull H/L Config.
FSDIO_CLK	FGPIO[36]	CLK	H
FSDIO_CMD	FGPIO[37]	CMD	H
FSDIO_DAT[3:0]	FGPIO[41:38]	DAT[3:0]	H
FSDIO_CD	FGPIO[43]	CD#	H
FSDIO_WP	FGPIO[44]	WP	H

4.3.4 *Display Interface*

Pin Name	Default	Alt. Func. 1				Alt. Func. 2	Alt. Func. 3
		CCIR-656	CCIR-601	RGB 24-bit	Serial RGB 8-bit	TCON + RGB-666	TCON
VD0	VGPIO[0]	YC[0]	YC[0]	VR0	D0	R0	
VD1	VGPIO[1]	YC[1]	YC[1]	VR1	D1	R1	
VD2	VGPIO[2]	YC[2]	YC[2]	VR2	D2	R2	
VD3	VGPIO[3]	YC[3]	YC[3]	VR3	D3	R3	
VD4	VGPIO[4]	YC[4]	YC[4]	VR4	D4	R4	
VD5	VGPIO[5]	YC[5]	YC[5]	VR5	D5	R5	
VD6	VGPIO[6]	YC[6]	YC[6]	VR6	D6	G0	
VD7	VGPIO[7]	YC[7]	YC[7]	VR7	D7	G1	
VD8	VGPIO[8]		VCCIR_C[0]	VG0		G2	
VD9	VGPIO[9]		VCCIR_C[1]	VG1		G3	
VD10	VGPIO[10]		VCCIR_C[2]	VG2		G4	
VD11	VGPIO[11]		VCCIR_C[3]	VG3		G5	
VD12	VGPIO[12]		VCCIR_C[4]	VG4		B0	
VD13	VGPIO[13]		VCCIR_C[5]	VG5		B1	
VD14	VGPIO[14]		VCCIR_C[6]	VG6		B2	
VD15	VGPIO[15]		VCCIR_C[7]	VG7		B3	
VD16	VGPIO[16]			VB0		B4	
VD17	VGPIO[17]			VB1		B5	
VD18	VGPIO[18]			VB2		GPOL (GPO3)	ckh2
VDCK	VGPIO[19]	VDCK	VDCK	VPXCK	VPXCK	SCKH	ckh1
VHSYNC	VGPIO[20]	VHSYNC	VHSYNC	DVHSYNC	DVHSYNC	SSTH (GPO9)	sth
VDVALID	VGPIO[21]	VDVALID	VDVALID	DVDVALID	DVDVALID	GSTV (GPO4)	stv
VVSYNC	VGPIO[22]	VVSYNC	VVSYNC	DVVSYNC	DVVSYNC	GCKV (GPO5)	ckv
VSPOL	VGPIO[23]			VB3		SPOL (GPO2)	com
VSREV	VGPIO[24]			VB4		SREV (GPO0)	q1h_ctr
VSLD	VGPIO[25]			VB5		SLD (GPO7)	oev1_mod2
VGOEV	VGPIO[26]			VB6		GOEV (GPO6)	oeh_mod1
VDRVPDN	VGPIO[27]			VB7		PWRDN (GPO8)	ckh3
CLKIN_IDU	VGPIO[28] / CLKIN_IDU						

4.3.5 *Panel Power PWM Interface*

Pin Name	Default	Alt. Func. 1	Alt. Func. 2
VPWM0	VPWM0	PGPIO[0]	I2CM_CLK (O)
VPWM_FB0	VPWM_FB0	PGPIO[1]	I2CM_DAT (I/O)
VPWM2	VPWM2	PGPIO[2]	I2CS_CLK (I)
VPWM_FB2	VPWM_FB2	PGPIO[3]	I2CS_DAT (I/O)

4.3.6 *Secondary UART Interface*

Pin Name	Default	Alt. Func. 1	Pull H/L Config.
HURX_B	UGPIO[4]	HURX_B	H
HUTX_B	UGPIO[5]	HUTX_B	
HUCTS_B	UGPIO[6]	HUCTS_B	
HURTS_B	UGPIO[7]	HURTS_B	

4.3.7 *USBOTG Interface*

Pin Name	Default	Alt. Func. 1
USBOTG0_VRES	USBOTG0_VRES	
USBOTG0_VBUS	USBOTG0_VBUS	
USBOTG0_DM	USBOTG0_DM	
USBOTG0_DP	USBOTG0_DP	
USBOTG0_ID	USBOTG0_ID	
USBOTG0_DRVVBUS	USBOTG0_DRVVBUS	OGPIO[0]
USBOTG1_VRES	USBOTG1_VRES	
USBOTG1_VBUS	USBOTG1_VBUS	
USBOTG1_DM	USBOTG1_DM	
USBOTG1_DP	USBOTG1_DP	
USBOTG1_ID	USBOTG1_ID	
USBOTG1_DRVVBUS	USBOTG1_DRVVBUS	OGPIO[1]

4.3.8 *I2S Digital Audio Interface*

Pin Name	Default	Alt. Func. 1
ACLK	AGPIO[0]	ACLK
AMCLK	AGPIO[1]	AMCLK
AFSYNC	AGPIO[2]	AFSYNC
ADIO	AGPIO[3]	ADIN/ADOUT

4.3.9 *GPIO Interface*

Pin Name	Default	Alt. Func. 1	Alt. Func. 2	Alt. Func. 3
GP[0]	GP[0]	HURX_A (I)		I2CM_CLK (O)
GP[1]	GP[1]	HUTX_A (O)		I2CM_DAT (I/O)
GP[2]	GP[2]/IR_in	HUCTS_A (I)		TM2 (O)
GP[3]	GP[3]	HURTS_A (O)		TM3 (O)
GP[4]	GP[4]		CLKOUT_12M	
GP[5]	GP[5]			TM4 (O)
GP[6]	GP[6]			TM5 (O)

4.3.10 ADC Interface

Pin Name	Default	Alt. Func. 1	Alt. Func. 2
ADC_IN0	ADC_IN0	KGPIO[0]	
ADC_IN1	ADC_IN1	KGPIO[1]	HURX_A (I)
ADC_IN2	ADC_IN2	KGPIO[2]	HUTX_A (O)
ADC_IN3	ADC_IN3	KGPIO[3]	3D_CLK (O)

5 Functional Description

5.1 CPU

The MP650UCG embeds a 32-bit RISC CPU, with a 32-bit MAC unit and instruction extension for audio performance enhancement. It offers good performance for audio processing and other application extensions that require intensive signal processing.

The operating frequency of CPU can be dynamically adjusted. Lower frequency setting can be used to save power consumption. SLEEP instruction can also be used to put the CPU into sleep mode, which will reduce the power consumption of CPU to the minimum level. Any enabled interrupt can then be used to wake up the CPU to normal operation.

It supports complete tool chain, including firmware, driver and debug utilities to facilitate software development.

5.1.1 *Memory Mapping*

The CPU supports 4GB of virtual addressing. It is divided into 4 segments as the following table. The 4GB of virtual address space are mapped to 512MB of physical space by ignoring the 3 MSBs.

Virtual Address Space	Description	Mapped Physical Address
0xE000_0000 ~ 0xFFFF_FFFF	KSEG2. 1GB. Addressable in Kernel mode. Cached	0x0000_0000 ~ 0x1FFF_FFFF
0xC000_0000 ~ 0xDFFF_FFFF		0x0000_0000 ~ 0x1FFF_FFFF
0xA000_0000 ~ 0xBFFF_FFFF	KSEG1. 512MB. Addressable in Kernel mode. Uncached	0x0000_0000 ~ 0x1FFF_FFFF
0x8000_0000 ~ 0x9FFF_FFFF	KSEG0. 512MB. Addressable in Kernel mode. Cached	0x0000_0000 ~ 0x1FFF_FFFF
0x6000_0000 ~ 0x7FFF_FFFF	KUSEG. 2GB. Addressable in Kernel or User mode. Cached	0x0000_0000 ~ 0x1FFF_FFFF
0x4000_0000 ~ 0x5FFF_FFFF		0x0000_0000 ~ 0x1FFF_FFFF
0x2000_0000 ~ 0x3FFF_FFFF		0x0000_0000 ~ 0x1FFF_FFFF
0x0000_0000 ~ 0x1FFF_FFFF		0x0000_0000 ~ 0x1FFF_FFFF

The 512MB of physical space is further mapped as follows:

Physical Space	Range	Description
0x1C00_0000 ~ 0x1FFF_FFFF	448 ~ 512MB	External Code Flash/Internal Boot ROM
0x1800_6000 ~ 0x1BFF_FFFF	408 ~ 448MB	Reserved
0x1800_0000 ~ 0x1800_5FFF	384 ~ 408MB	Scratch Pad Data Memory
0x1400_0000 ~ 0x17FF_FFFF	320 ~ 384MB	Reserved
0x1000_0000 ~ 0x13FF_FFFF	256 ~ 320MB	Peripheral
0x0800_0000 ~ 0x0FFF_FFFF	128 ~ 256MB	Register File
0x0000_0000 ~ 0x07FF_FFFF	0 ~ 128MB	DRAM

The physical space 0x1c00_0000 to 0x1fff_ffff is mapped to either external Serial NOR Flash or internal boot ROM depends on the boot-up configuration.

The following table also summarizes the register file mapping.

Physical Space	Contents
0x0803_8000 ~ 0x0FBF_FFFF	Reserved
0x0803_4000 ~ 0x0803_7FFF	MMCP Registers
0x0803_0000 ~ 0x0803_3FFF	MPV Registers
0x0802_6000 ~ 0x0802_FFFF	Reserved
0x0802_4000 ~ 0x0802_5FFF	SPI Registers
0x0802_2000 ~ 0x0802_3FFF	CDU Registers
0x0802_0000 ~ 0x0802_1FFF	Memory Card Control Registers
0x0801_E000 ~ 0x0801_FFFF	IDU/OSD Registers
0x0801_C000 ~ 0x0801_DFFF	GPIO Registers
0x0801_A000 ~ 0x0801_BFFF	RTC Registers
0x0801_8000 ~ 0x0801_9FFF	USB Registers
0x0801_6000 ~ 0x0801_7FFF	Reserved
0x0801_4000 ~ 0x0801_5FFF	AIU Registers
0x0801_2000 ~ 0x0801_3FFF	UART & UARTH Registers
0x0801_0080 ~ 0x0801_01FF	I2C Registers
0x0801_0000 ~ 0x0801_007F	IR Registers
0x0800_E000 ~ 0x0800_FFFF	Timer Registers
0x0800_C000 ~ 0x0800_DFFF	DMA Control Registers
0x0800_B000 ~ 0x0800_BFFF	Interrupt Handler Control Registers
0x0800_A000 ~ 0x0800_AFFF	Clock Generator Registers
0x0800_8000 ~ 0x0800_9FFF	BIU/System Control Registers
0x0800_0000 ~ 0x0800_7FFF	IPU Registers

Table 5-1 Register File Mapping

5.1.2 *Boot-up Configuration*

MP650UCG supports 2 boot-up configurations, either from the embedded ROM or external Serial NOR Flash. It's controlled by the power-on strap inputs from pin VHSYNC. If VHSYNC is pulled high at reset, MP650UCG will boot up from the external Serial NOR Flash. Otherwise, it will boot up from the embedded ROM. In either case, the external Serial NOR Flash is accessible through proper software configuration after boot-up procedure is completed.

5.2 DMA Controller

The DMA controller controls the traffic between functional modules and SDRAM/DDR. An arbiter is included to arbitrate among various SDRAM/DDR read/write requests from different functional modules. It supports 3 levels of configurable data access priorities. Each DMA channel can be configured flexibly and dynamically.

To satisfy high memory bandwidth requirement demanded by real time application, the arbiter also supports 1 preemptive request which has the highest DMA priority. The request to be assigned with the highest priority is also configurable. This feature insures that the DMA bus ownership will be granted to the selected channel as soon as the request is asserted.

The accompanying DRAM controller can support up to 64Mbyte DDR DRAM or 32Mbyte SDRAM. Versatile DRAM timing parameters can be configured flexibly. A deep power down mode is also supported by the DRAM controller. When there is no pending request, the DRAM controller will force the DRAM into self refresh mode. The DRAM will then be woken up automatically when there is need of DRAM access.

5.3 Generic Memory Copy DMA

The MP650UCG embeds a one-channel generic DMA controller which can perform memory-to-memory data transfers without CPU intervention. Two kinds of operation mode are supported by this DMA, memory copy mode and write only mode. In the memory copy mode, data from the source memory are copied to the destination memory by this DMA controller. In the write only mode, the generic memory copy DMA controller can refill the destination memory with user-defined constant value. The generic memory copy DMA starts by software and the CPU can recognize when an operation has been completed by software polling or when it receives a generic memory copy DMA interrupt.

5.4 Image Processing Unit (IPU)

The Image Processing Unit supports versatile image operations including scaling, basic color operation, color manipulation, special effect, color transform and overlay.

Scaling: The scaling engine supports up to 3x scaling up and 16x scaling down. The input and output image size can be up to 16k by 16k. Besides the scaling function, the engine also support edge enhancement and blur function.

Basic color operation: The basic color operation includes 32-level Y curve, Y offset, Y gain, CbCr offset, CbCr gain and CbCr rotation. Window function is also included before the output of IPU.

Color manipulation: The IPU includes two different types of selective color manipulation in both YCbCr and RGB domains. In YCbCr domain, the color space is divided into 32x32 square areas evenly. The color offset of each 32x32 areas can be adjust individually. In RGB domain, the color space is divided into 24 coaxes fan-shape areas evenly. The color offset of each 24 areas can be adjusted individually. Color manipulation in both YCbCr and RGB domain can be used at the same time. This configuration can be used to explore the favorite of different color intention among different color spaces.

Special effect: In order to enrich the fun of image manifestation and release the burden of CPU, the IPU also supports several arithmetic operations for image retouch. That includes black-white (with configurable Y value), color merge, high color gain, edge sketch, bit-plane cut, and additive noise. These functions can be enabled individually. The order of pipeline can also be adjusted by register configuration.

Color transform: The IPU has two color transform matrix. Each matrix has 3x3 add-multiplication and 3 offsets. The chroma offset can also be adjusted individually at both input and output of the IPU. With this function, color transforms like RGB=>YUV, YUV=>RGB or RGB=>RGB can be achieved.

Overlay: The IPU support 24bit true color overlay function with color key and configurable multiplication factors for both main and overlay image on color key and non color key area. The role of main and overlay images can also be switched. Overlay window is controlled by the start position and the size of overlay image.

All the above functions listed can be enabled individually. The order of pipeline is also configurable.

The input format of IPU supports ARGB32bit, RGB888, YCbCr422, YCbCr444, and YCbCr420 (from video decoder). The output format of IPU supports RGB888, YCbCr422 and YCbCr444. The image size of both input and output can be up to 16k by 16k.

5.5 Image Display Unit (IDU)

The Image Display Unit supports variety of digital LCD interface. It supports several output formats, including CCIR-601/656/709, RGB-666/888 or serial RGB.

MP650UCG provides great flexibility in display timing settings. Typical display output timing is illustrated in Fig. 5-1 and 5-2. All the parameters shown in the figures are programmable.
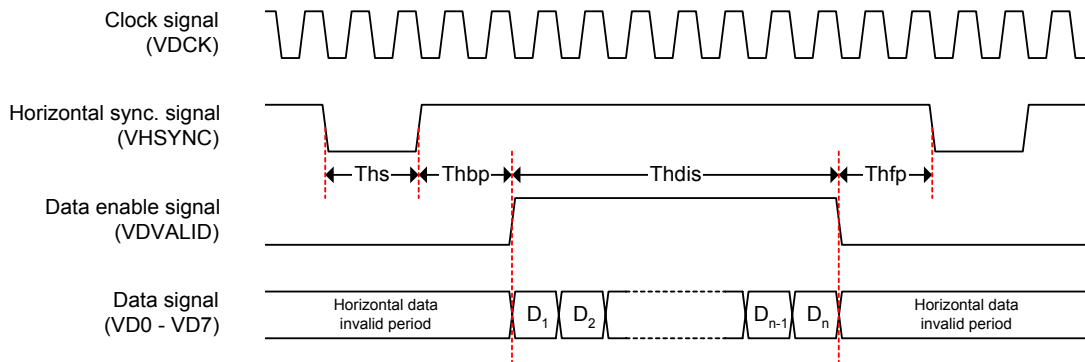
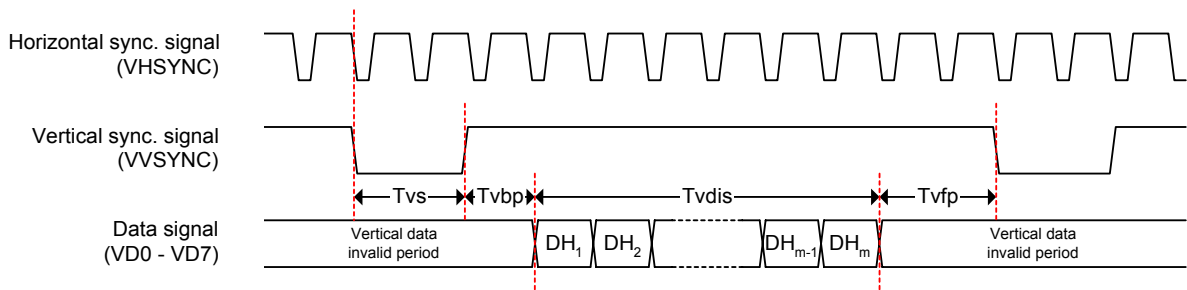**Fig. 5-1 Display output horizontal timing diagram**

Fig. 5-2 Display output vertical timing diagram

It accepts 4 input data formats: YCbCr-422, YCbCr-444, XRGB and packed RGB-888. A programmable Color Space Converter is included for YCbCr-to-RGB or vice versa conversion. A dithering unit is supported to minimize contour artifact if RGB-666 output is selected. It also supports independent RGB Gamma correction to cater different panel characteristics or customer requirement. The gamma correction of each color component is done with 32-step piecewise-linear programmable coefficients.

A digital TCON is also included to support glue-less connection with variety of panels. With most parameters programmable, it can support variety of panels with maximum flexibility.

5.6 JPEG CODEC

A standard JPEG Compression/Decompression engine is embedded. It is compliant to the Baseline JPEG Standard. JPEG Decoder accepts image data in YCbCr 4:2:2 h, YCbCr 4:2:2 v, YCbCr 4:2:0, and YCbCr 4:4:4 formats. Besides, it also supports Y only format and 1/2/3/4-component Raw Data with 2 Huffuman and 2 Quantization tables at max. JPEG Encoder only compresses photo in YCbCr 4:2:2 h format.

MCU size	16 × 16	16 × 8	8 × 16	8 × 8

Table 5-2. MCU types supported by CDU

It is capable of processing image with resolution up to 64Kx64K in decoding and 8Kx8K in encoding. The image source and compressed stream are both acquired from and delivered to DRAM through DMA. It needs no CPU intervention for data transfer. Single cycle throughput can be achieved to allow real-time capturing. It can always catch up and deliver high performance for continuous image or video capturing.

It supports two sets of Quantization and Huffman tables respectively. They are both programmable for better compression quality adjustment. The latter is usually fixed in factory, while the Quantization table can be adjusted with pre-determined values for image quality and compression ratio tradeoff controlled by the end users.

It also supports Restart Marker insertion and detection when enabled. Other markers or headers should be handled by the firmware instead.

The JPEG module consists of System Bus Interface, configuration registers, dedicated SRAM modules, system memory interface, Sub-sampling Unit and Control Unit.

CPU can configure and start/stop encoding/decoding process via the 32-bit System Bus Interface.

In encoding mode, it reads in images pixel data, from external system DRAM and outputs the encoded stream data back to DRAM.

While decoding, stream data is read from DRAM, with header information (Huffman tables, quantization tables, etc.) already peeled by CPU. Pixel data is output MCU by MCU.

An interrupt is triggered when encoding/decoding process is finished.

5.7 Multi-format Video Decoder

For the application which needs high quality video playback, the MP650UCG embeds a high performance pure hardware multi-format video decoder to accelerate the video decoding. The video decoder is capable of decoding H.264, MPEG-4/H.263, Sorenson Spark, MPEG-2 and MPEG-1 bitstreams that conform to the supported standards, profiles and levels are presented in Table 5-8-1 and Table 5-8-2.

Standard	Decoder supported profile and level
H.264	Baseline Profile, levels 1 – 3.1 Main Profile, levels 1 – 3.1 High Profile, levels 1 – 3.1
MPEG-2	Main Profile, low and medium levels
MPEG-4	Simple Profile, levels 0-6 Advanced Simple Profile, levels 0-5
H.263	Profile 0, levels 10-70
Sorenson Spark	Bitstream version 0 and 1

Table 5-3 Supported standards, profiles and levels

Standard	Tool	Decoder support
H.264	Slice group	Up to 8 supported. If more than 1 used, SW performs entropy decoding
H.264	Arbitrary slice order	Supported, SW performs entropy decoding
H.264	redundant slices	Supported, but not utilized; slices are skipped by SW
H.264	image cropping	Not performed by the decoder, cropping parameters are returned to the application
MPEG-4	data partitioning	supported, SW performs entropy decoding
MPEG-4	global motion compensation	Not supported

Table 5-4 Deviations from supported profiles and levels

The features of the decoder for each supported standards are shown in Table 5-8-3 ~ Table 5-8-5.

Feature	Decoder support
Input data format	H.264 byte or NAL unit stream
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48x48 to 1280x720, step size 16 pixels
Maximum frame rate	30fps @ 1280x720
Maximum bit rate	As specified by H.264 HP level 3.1
Error detection and concealment	supported

Table 5-5 H.264 Features

Feature	Decoder support
Input data format	MPEG-4/H.263/Sorenson Spark elementary video stream
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48x48 to 1280x720, step size 16 pixels
Maximum frame rate	30fps @ 1280x720
Maximum bit rate	As specified by MPEG-4 ASP level 5
Error detection and concealment	supported

Table 5-6 MPEG-4/H.263/Sorenson Spark features

Feature	Decoder support
Input data format	MPEG-2/MPEG-1 elementary video stream
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48x48 to 1280x720, step size 16 pixels
Maximum frame rate	30fps @ 1280x720
Maximum bit rate	As specified by MPEG-2 MP, medium level
Error detection and concealment	supported

Table 5-7 MPEG-2/MPEG-1 features

There is also a post-processor built in MP650UCG to cooperate with the video decoder. It is possible to run the post-processor combined with the decoder, or as a stand-alone function, when it can process data from

an external source such as from IPU or JPEG decoder. The features of this post-processor are listed as following: user definable color conversion, image contrast/brightness/saturation adjustment, image up-scaling with bicubic polynomial interpolation, image down scaling with averaging filter, deinterlacing, de-blocking filter, image 90/180/270 degree rotation and image horizontal/vertical flip.

5.8 Memory Card Controller

The Memory Card Controller is responsible of controlling the data accesses with external image storage media. It supports Compact Flash, Secure Digital Memory Card (SD), Multi Media Card (MMC), xD , Memory Stick, Memory Stick Pro and Memory Stick Pro HG. Coexist with the memory cards, on-board NAND Flash is also supported.

For Compact Flash interface, only Memory mode can be supported. Hardware ECC and CRC are implemented for MMC/SD support respectively.

Data transfer with Compact Flash can be accomplished through DMA or CPU. For MMC or SD, however, it allows only through DMA. The bus interface timing is programmable for maximum compatibility.

5.9 SPI Serial Flash Controller

MP650UCG includes a Serial Flash Controller that supports transfer to/from SPI Flash in SPI protocols.

5.10   USB OTG Controller 0 and 1

The built-in USB OTG Controller supports device, host and OTG functions, the transceiver interface is UTMI+level2, which support HS/FS/LS transfers without a hub.
All transfers are accomplished with DMA for optimal performance. The host function supported includes:

> Control Read/Write transfer
>
> Interrupt Transfer
>
> Downstream Bulk Transfer from Host
>
> Upstream Bulk Transfer to Host

The upstream bulk or isochronous transfer is accomplished with DMA operation.

The software we provided includes the protocol of MSDC (Mass Storage Device Class) which is compatible

with the OSs Microsoft Windows 2000, Windows XP, Windows Vista, Mac OS X 10.2.4 or later.

5.11   Digital Audio Interface Unit (AIU)

The Digital Audio Interface Unit (AIU) handles data communication between MP650UCG and internal/external audio DAC. Only audio playback is supported. It implements a quite flexible interface for standard I2S or generic audio DAC. It supports both Master and Slave clocking. It also supports variety of audio data format, 8 or 16-bit, mono or stereo, and sampling rate for playback.

5.12   Peripheral Controller

5.12.1 GPIO

The MP650UCG provides 7 dedicated GPIO pins. There are also additional pins can be configured as

GPIO if the associated function is not used. Most of the pins can be programmed for alternative functions by setting corresponding configuration register. Those dedicated GPIO pins can be enabled to generate interrupt with level or edge trigger. The polarity of level or edge interrupt is programmable to fit variety of application requirement.

The GPIO input pins with interrupt capability, when enabled, can also be used to wake up the chip from deep power down mode.

5.12.2 *I2C Master*

MP650UCG support I2C Master Interface .I2C interface acts as a bus master and is fully programmable by the CPU. It supports 8bit and 16bit modes with or without device acknowledge check. It also supports loop write/read which can transfer unlimited bytes continuously in a packet.

5.12.3 *I2C Slave*

MP650UCG support I2C slave interface which can connect to external I2C Master.

5.12.4 *UART Controller A and B*

The MP650UCG support Dual UART ports. The secondary UART(UART_B) supports flow control with max baud rate 8Mbps.

5.12.5 *IR Controller*

MP650UCG has built-in IR decoder that supports NEC and Remote Point Mouse Protocol. Signal delay time and data bits number are programmable to support specific protocols.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Units
VPP, VPPM	Digital I/O Supply Voltage(including VPP, VPPM, VPP_OSC)	-1.0 to 4.6	V
VPP_RTC	RTC I/O Supply Voltage	-1.0 to 4.6	
VPPA	Analog I/O Supply Voltage (including USBOTG0_VDDA, USBOTG1_VDDA, VPPA_AUD_1, VPPA_AUD_2, VPPA_ADC_PWM)	-0.5 to 4.6	V
VDD	Digital Core Supply Voltage (VDD_OSC, VDD_RTC)	TBD	V
VDDA	Analog Core Supply Voltage (USBOTG0_VDDL, USBOTG1_VDDL, VDD_PLL1, VDD_PLL23, VDDA_PLL_IDU)	TBD	
TSTG	Storage Temperature	-40 to 125	°C
ESD	ESD Rating (Rzap = 1.5K Ω, Czap = 100pf)	TBD	V

Note:

1. Permanent device damage may occurs if the specification for the Absolute Maximum Ratings are exceeded.

2. All voltages are defined with respect to ground.

6.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VPP	Digital I/O Supply Voltage(including VPP, VPP_OSC)	3.0	3.3	3.6	V
VPPM-SDRAM	VPPM supply voltage for SDRAM	3.0	3.3	3.6	V
VPPM-DDR	VPPM supply voltage for DDR	2.25	2.5	2.75	V
VPP_RTC	RTC I/O Supply Voltage	TBD		3.6	
VPPA	Analog I/O Supply Voltage (including USBOTG0_VDDA, USBOTG1_VDDA, VPPA_AUD_1, VPPA_AUD_2, VPPA_ADC_PWM)	3.0	3.3	3.6	V
VDD	Digital Core Supply Voltage (VDD_OSC, VDD_RTC)	1.08	1.2	1.32	V
VDDA	Analog Core Supply Voltage (USBOTG0_VDDL, USBOTG1_VDDL, VDD_PLL1, VDD_PLL23, VDDA_PLL_IDU)	1.08	1.2	1.32	V
TA	Ambient Operating Temperature	0	-	70	°C

6.3 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	TTL	-0.5		0.8	V
V_{IH}	Input High Voltage	TTL	2.0		5.0	V
V_{OL}	Output Low Voltage	I_{OL} = -2, -4, -8, -12, -16, -24mA	0		0.4	V
V_{OH}	Output High Voltage	I_{OH} = 2, 4, 8, 12, 16, 24mA	2.4			V
I_i	Input Leakage Current	VPP = MIN V_{IN} = GND or 3.6V	TBD		TBD	
Ioz	Tri-state Output Leakage Current	VPP = MIN V_{IN} = GND or 5V	-100uA		100µA	

Note: 1. The I/O with Schmitt-trigger: RESETx.

6.4 Capacitance

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{IN}	Input pin capacitance		5		pF
C_{BI}	Bidirectional pin capacitance		5		pF
C_{OUT}	Output pin capacitance		5		pF

6.5 AC Characteristics

6.5.1 *Reset Timing*
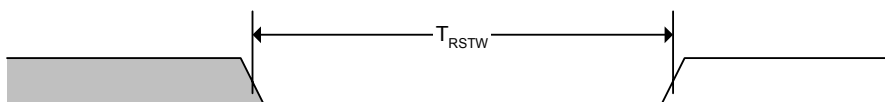
Fig. 6-1 Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{RSTW}	Reset Pulse Width	1			ms

6.5.2 *Input Clock*
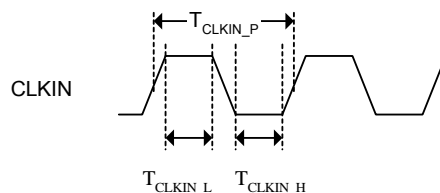
Fig. 6-2 CLKIN AC Characteristic

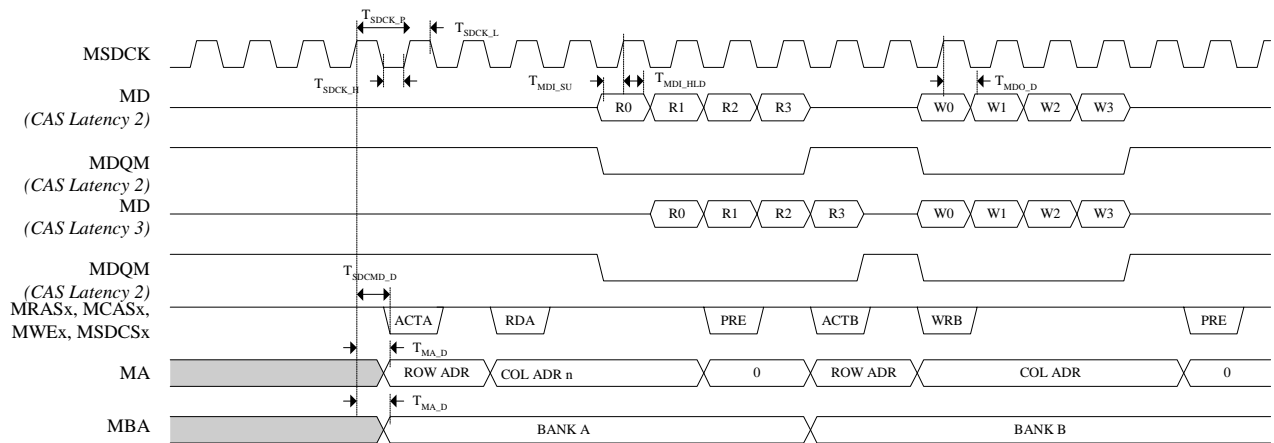| Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{CLKIN}	CLKIN Master Clock Input Frequency		12		MHZ
T_{CLKIN_P}	CLKIN Master Clock Input Period		83.3		ns
T_{CLKIN_L}	CLKIN Master Clock Input Low Width	37.5		45.8	ns
T_{CLKIN_H}	CLKIN Master Clock Input High Width	37.5		45.8	ns
DT_{CLKIN}	CLKIN Duty Cycle	45		55	%

6.5.3 *SDRAM/DDR Interface Timing*

Fig. 6-3 Basic SDRAM Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{SDCK_P}	SDRAM Clock Output Period	6			ns
T_{SDCK_H}	SDRAM Clock Output High Pulse Width	3			ns
T_{SDCK_L}	SDRAM Clock Output Low Pulse Width	3			ns
T_{MDI_SU}	SDRAM Data Input Setup Time	1.2			ns
T_{MDI_HLD}	SDRAM Data Input Hold Time	0			ns
T_{MA_D}	SDRAM Address Valid Delay			4.4	ns
T_{MDO_D}	SDRAM Data Output Valid Delay			4.4	ns
T_{SDCMD_D}	SDRAM Command Valid Delay			4.4	ns

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{SDCK_P}	DDR Clock Output Period	6			ns
T_{SDCK_H}	DDR Clock Output High Pulse Width	3			ns
T_{SDCK_L}	DDR Clock Output Low Pulse Width	3			ns
T_{MDI_SU}	DDR Data Input Setup Time (to DQS)	0.8			ns
T_{MDI_HLD}	DDR Data Input Hold Time (to DQS)	0			ns
T_{MA_D}	DDR Address Valid Delay			4.4	ns
T_{MDO_D}	DDR Data Output Valid Delay (to DQS)			0.5	ns
T_{SDCMD_D}	DDR Command Valid Delay			4.4	ns

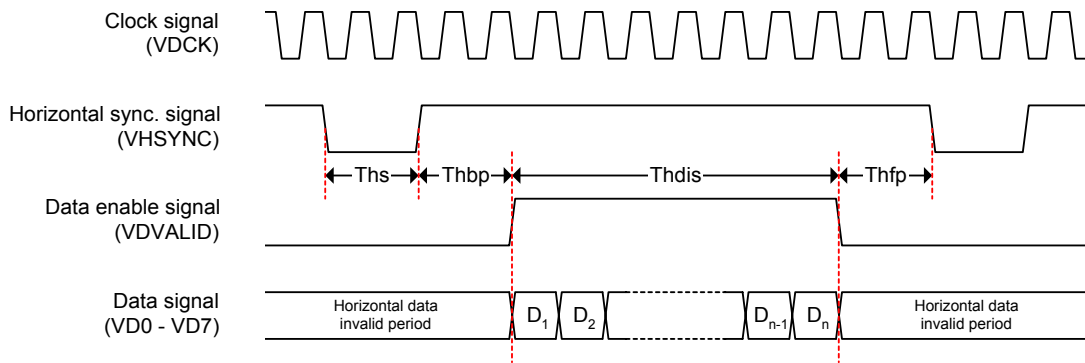### 6.5.4 *RGB-888 Display Output, W/O TCON*

Fig. 6-4 Display/CCIR-601 Output Horizontal Timing
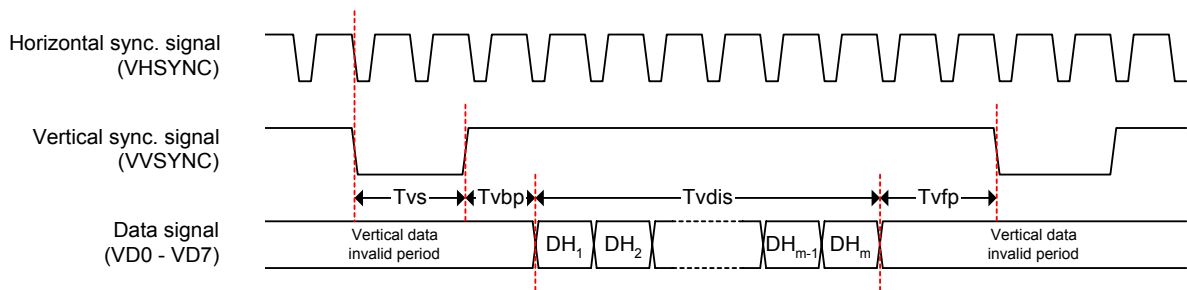

Fig. 6-5 Progressive Display Output Vertical Timing
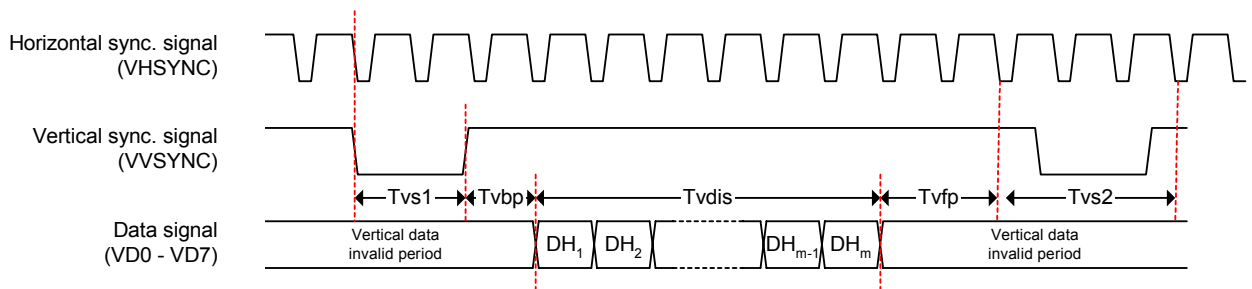

Fig. 6-6 Progressive Display Output Vertical Timing
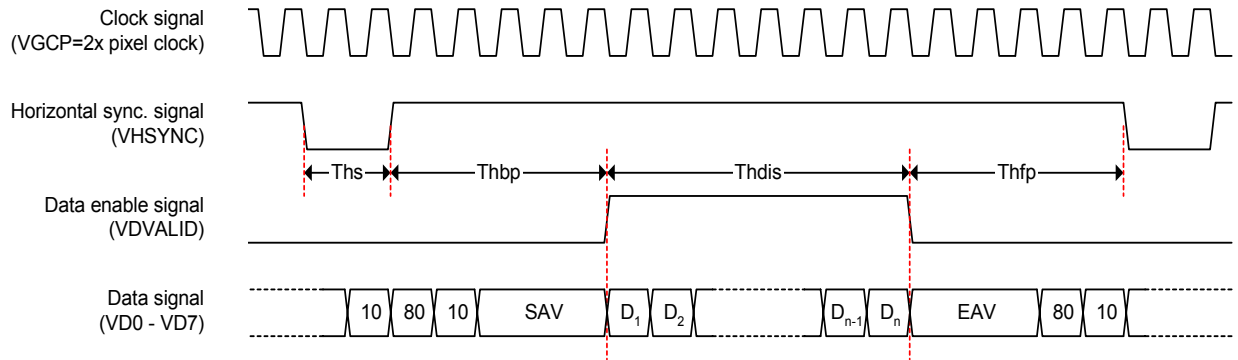
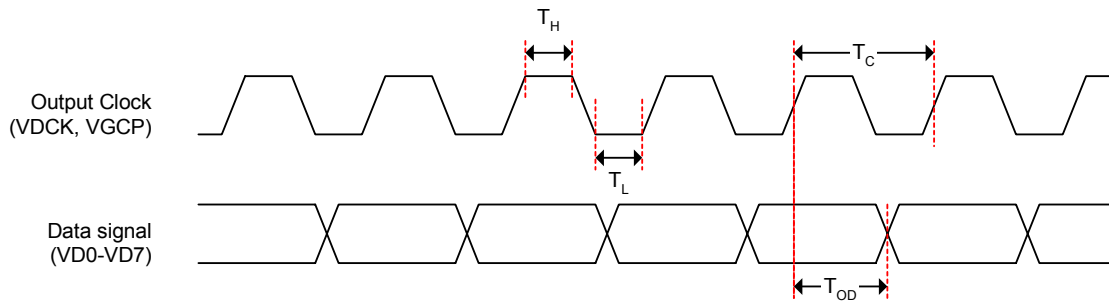**Fig. 6-7 CCIR-656 Output Horizontal Timing**

Fig. 6-8 Display Output Clock, and Data Sample Timing

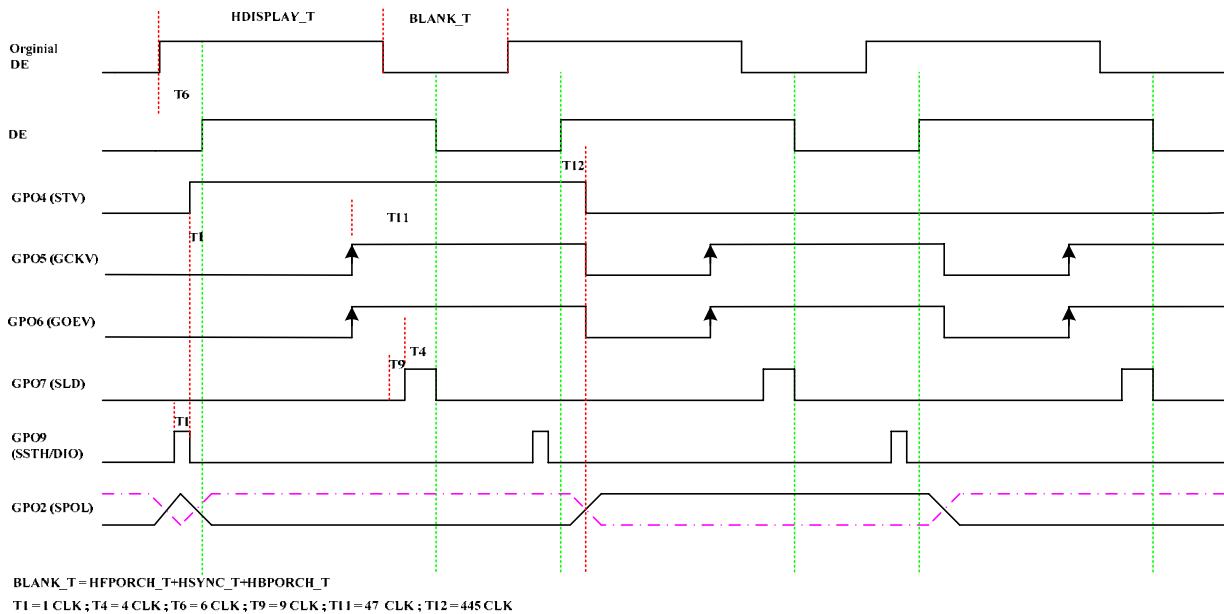| Symbol		Parameter	Min.	Typ.	Max.	Unit
T_{hs}		Horizontal Sync. Pulse Width	1		256	VDCK
T_{hbp}		Display Horizontal Back Porch Width	1		256	VDCK
T_{hdis}		Horizontal Display Enable Width	1		2048	VDCK
T_{hfp}		Display Horizontal Front Porch Width	1		256	VDCK
T_{vs}		Vertical Sync. Pulse Width	1		256	line
T_{vbp}		Display Vertical Back Porch Width	1		256	line
T_{vdis}		Vertical Display Enable Width	1		2048	line
T_{vfp}		Display Vertical Back Porch Width	1		256	line
T_C	VDCK	VDCK Clock Cycle Time	65			Ns
	VGCP	VGCP (2x of VDCK) Clock Cycle Time	33			Ns
T_H	VDCK	VDCK Clock High Pulse Width	20			Ns
	VGCP	VGCP (2x of VDCK) Clock High Pulse Width	11			Ns
T_L	VDCK	VDCK Clock Low Pulse Width	20			Ns
	VGCP	VGCP (2x of VDCK) Clock Low Pulse Width	11			Ns
T_{OD}	VDCK	Display Data Output delay time relative to the rising edge of VDCK			TBD	Ns
	VGCP	Display Data Output delay time relative to the rising edge of VGCP			TBD	Ns

6.5.5 *Display TCON Output Timing*

Fig. 6-9 TCON Control Timing

6.5.6 *NAND Flash Interface Timing*

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{CLS}	CLE Setup Time	0		-	ns
T_{CLH}	CLE Hold Time	10		-	ns
T_{WP}	Write Pulse Width *1	40		-	ns
T_{ALS}	ALE Setup Time	10		-	ns
T_{ALH}	ALE Hold Time	0		-	ns
T_{DS}	Data Setup Time *1	40		-	ns
T_{DH}	Data Hold Time *1	20		-	ns
T_{WC}	Write Cycle Time	60		-	ns
T_{RP}	Read Pulse Width *2	30		-	ns
T_{RC}	Read Cycle Time *2	50		-	ns
T_{REA}	Read Access Time (depends on Flash data output) *3	20		-	ns
T_{CR}	CE Low to RE Low	10		-	ns
T_{CLR}	CLE Low to RE Low	10		-	ns
T_{AR}	ALE Low to RE Low	10		-	ns
T_{REH}	RE High Hold Time	10		-	ns
T_{tR}	Write Cycle Time	20		-	ns

Note:

*1:Write cycle time length can be programmed by software & the minimum cycle count is 2 + 4 (2 high + 4 low) or 1+5 (1high + 5 low).

*2.Read cycle time length can be programmed by software & the minimum cycle length is "TREA + 1MCARD clock + RE high (2 MCARD clock)"
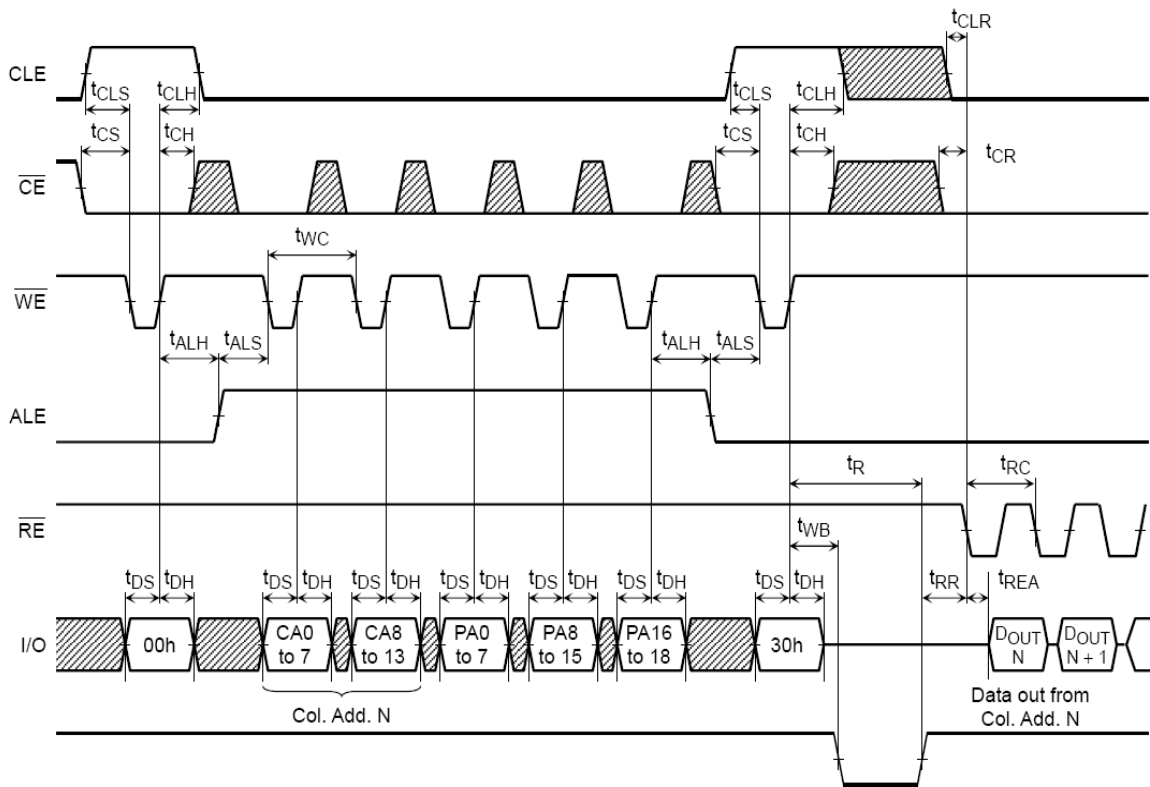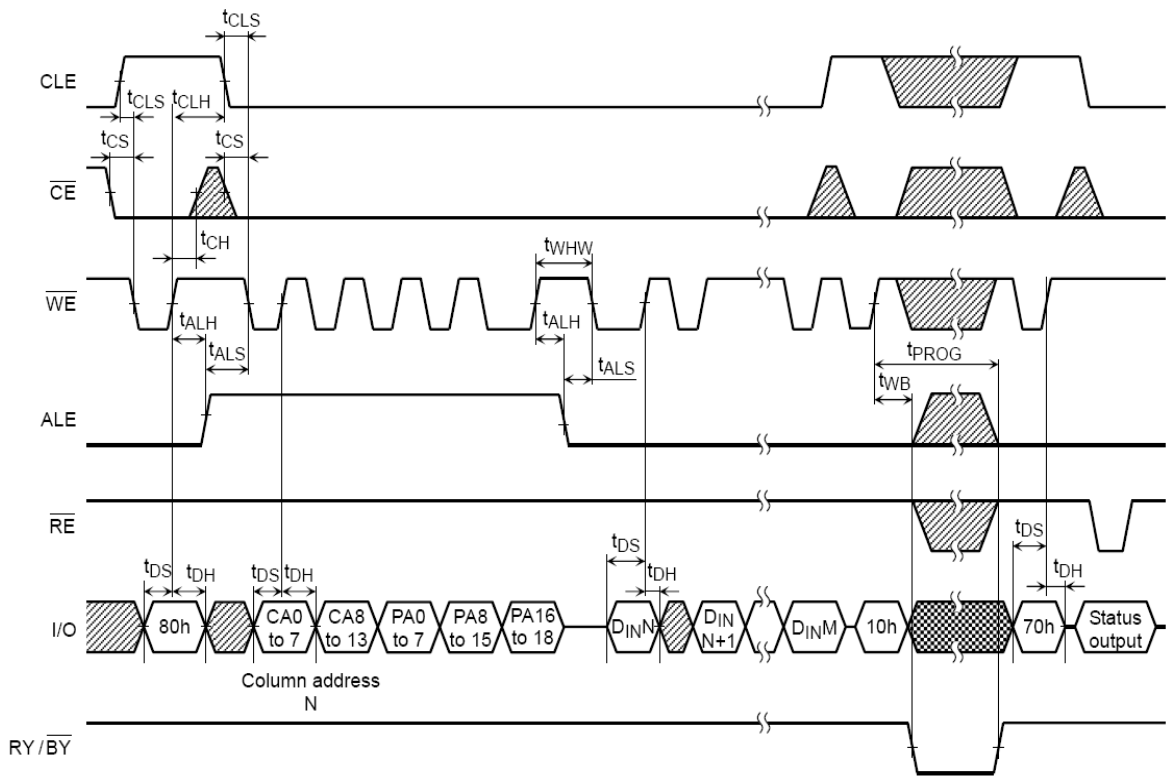
Fig. 6-10 NAND Flash Read Timing

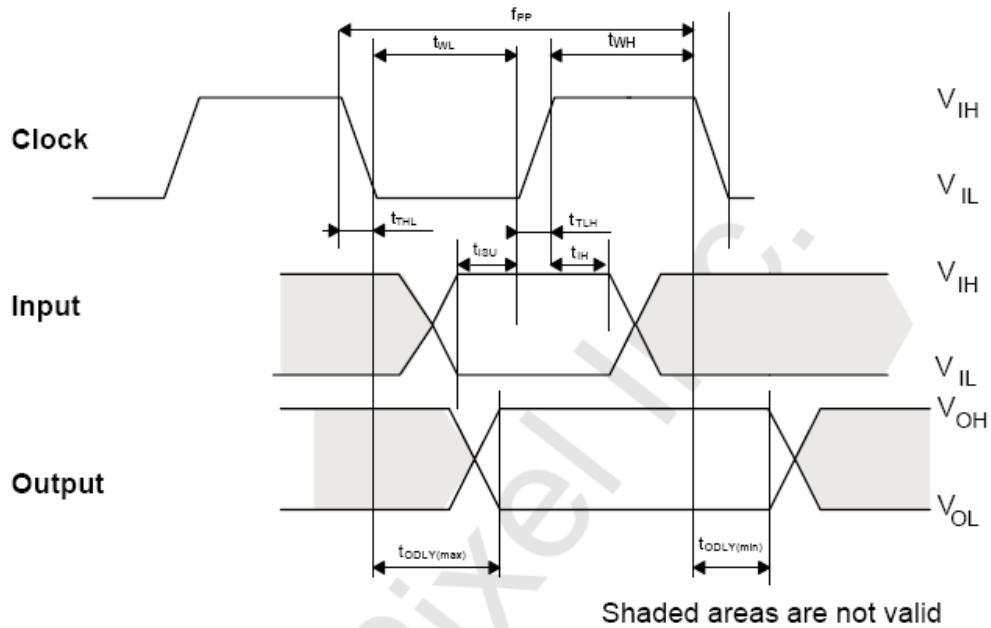**Fig. 6-11 NAND Flash Programming Timing**

6.5.7 SD Card Interface Timing

Fig. 6.12 SD Card Bus Timing (Defaults)

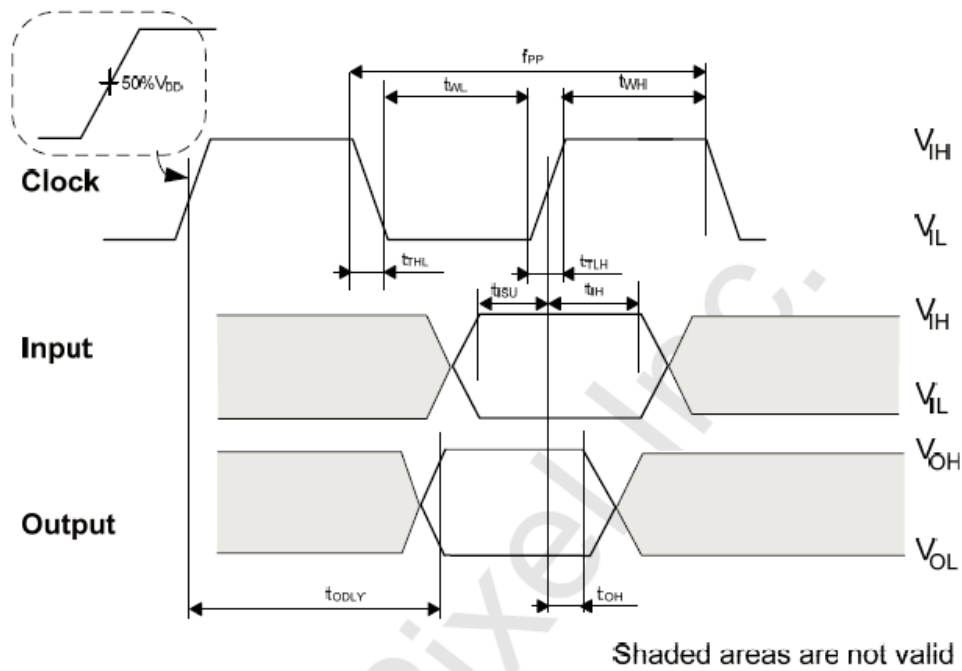| Parameter	Symbol	Min	Max.	Unit
Clock CLK (All values are referred to min (VIH) and max (VIL),				
Clock frequency Data Transfer Mode	fPP	0	25	MHz
Clock frequency Identification Mode	fOD	0(1)/100	400	kHz
Clock low time	tWL	10		ns
Clock high time	tWH	10		ns
Clock rise time	tTLH		10	ns
Clock fall time	tTHL		10	ns
Inputs CMD, DAT (referenced to CLK)				
Parameter	Symbol	Min	Max.	Unit
Input set-up time	tISU	5		ns
Input hold time	tIH	5		ns
Outputs CMD, DAT (referenced to CLK)				
Output Delay time during Data Transfer Mode	tODLY	0	14	ns
Output Delay time during Identification Mode	tODLY	0	50	ns

Bus Timing - Parameters Values (Default)

Fig. 6.13 SD Card Bus Timing (High Speed)

Parameter	Symbol	Min	Max.	Unit
Clock CLK (All values are referred to min (VIH) and max (VIL),				
Clock frequency Data Transfer Mode	fPP	0	50	MHz
Clock low time	tWL	7		ns
Clock high time	tWH	7		ns
Clock rise time	tTLH		3	ns
Clock fall time	tTHL		3	ns
Inputs CMD, DAT (referenced to CLK)				
Input set-up time	tISU	6		ns
Input hold time	tIH	2		ns
Parameter	Symbol	Min	Max.	Unit
Outputs CMD, DAT (referenced to CLK)				
Output Delay time during Data Transfer Mode	tODLY		14	ns
Output Hold time	tOH	2.5		ns

Bus Timing - Parameters Values (High Speed)

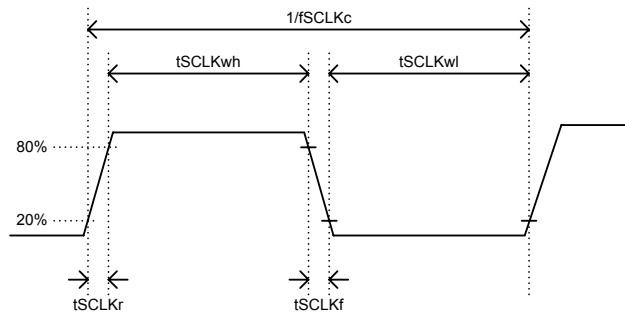### 6.5.8 *Memory Stick Card Interface Timing*
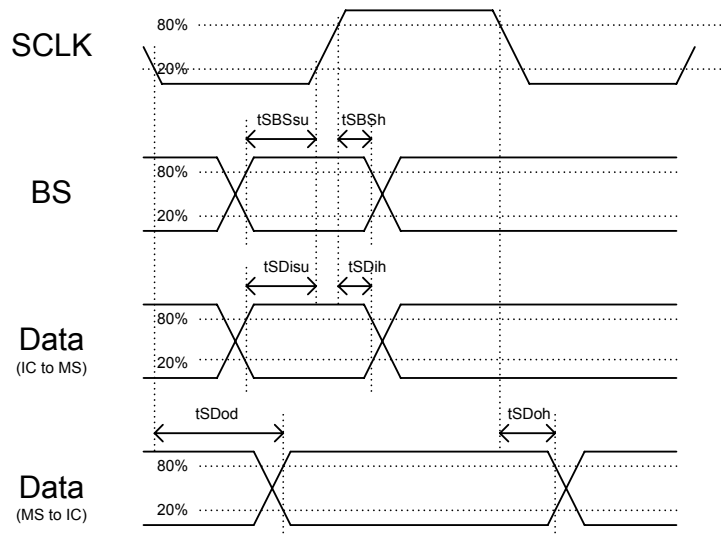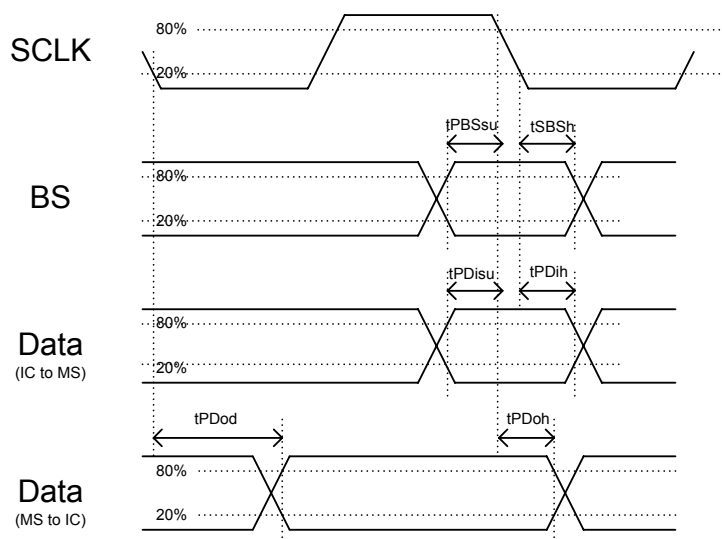
Fig. 6.14 SCLK Timing

Fig. 6.15 Transfer Operation Timing (Serial Interface)

Signal	Parameter	Symbol	Rating		Unit
			Min.	Max	
SCLK	Frequency	fSCLK	-	20	MHz
	H pules width	tSCLKwh	15	-	nsec
	L pulse width	tSCLKwl	15	-	nsec
	Rising time	tSCLKr	-	7.5	nsec
	Falling time	tSCLKf	-	7.5	nsec
BS	Setup time	tSBSsu	5	-	nsec
	Hold time	tSBSh	5	-	nsec
DATA	Setup time	tSDisu	5	-	nsec
	Hold time	tSDih	5	-	nsec
	Output delay time	tSDod	-	15	nsec
	Output hold time	tSDoh	1.5	-	nsec

Serial I/F

Fig. 6.16 Transfer Operation Timing (Parallel Interface)

Signal	Parameter	Symbol	Rating		Unit
			Min.	Max	
SCLK	Frequency	fSCLK	-	40	MHz
	H pules width	tSCLKwh	5	-	nsec
	L pulse width	tSCLKwl	5	-	nsec
	Rising time	tSCLKr	-	7.5	nsec
	Falling time	tSCLKf	-	7.5	nsec
BS	Setup time	tPBSsu	7	-	nsec
	Hold time	tPBSh	0	-	nsec
DATA	Setup time	tPDisu	7	-	nsec
	Hold time	tPDih	0	-	nsec
	Output delay time	tPDod	-	15	nsec
	Output hold time	tPDoh	1.5	-	nsec

4-bit Parallel I/F

Signal	Parameter	Symbol	Rating		Unit
			Min.	Max	
SCLK	Frequency	fSCLK	20	60	MHz
	H pules width	tSCLKwh	5	-	nsec
	L pulse width	tSCLKwl	5	-	nsec
	Rising time	tSCLKr	-	7.5	nsec
	Falling time	tSCLKf	-	7.5	nsec
BS	Setup time	tSBSsu	7	-	nsec
	Hold time	tSBSh	0	-	nsec
DATA	Setup time	tSDisu	7	-	nsec
	Hold time	tSDih	0	-	nsec
	Output delay time	tSDod	-	10	nsec
	Output hold time	tSDoh	1.5	-	nsec

8-bit Parallel I/F

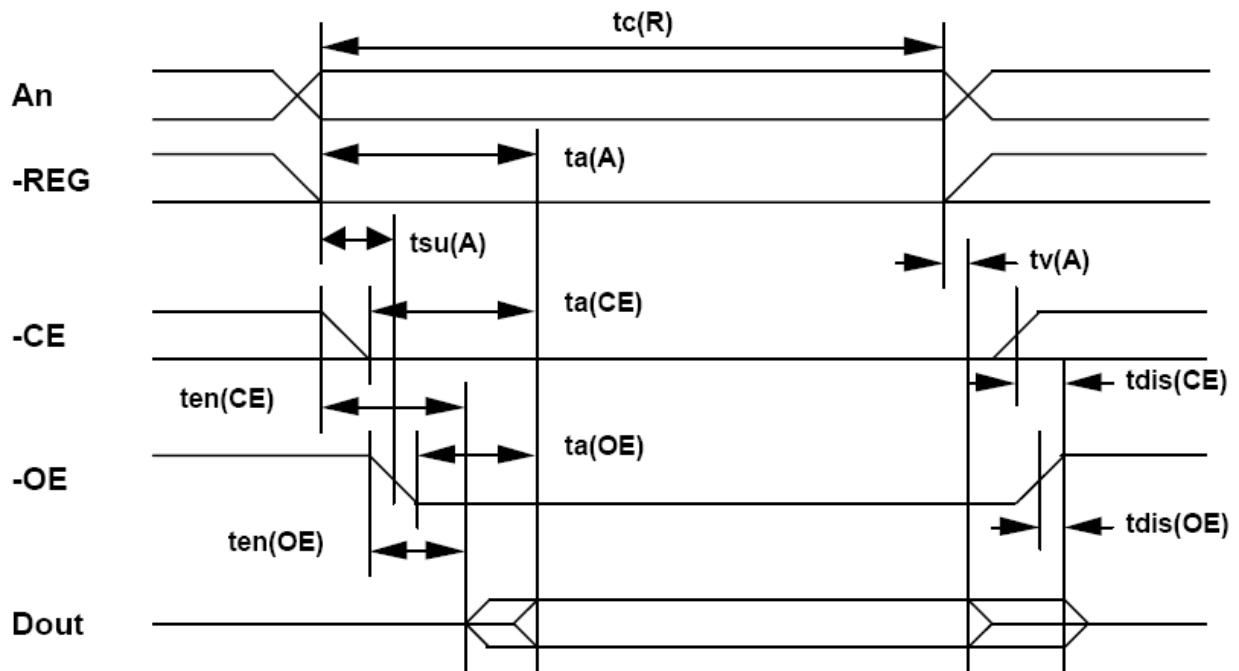### 6.5.9 *Compact Flash Card Interface Timing*

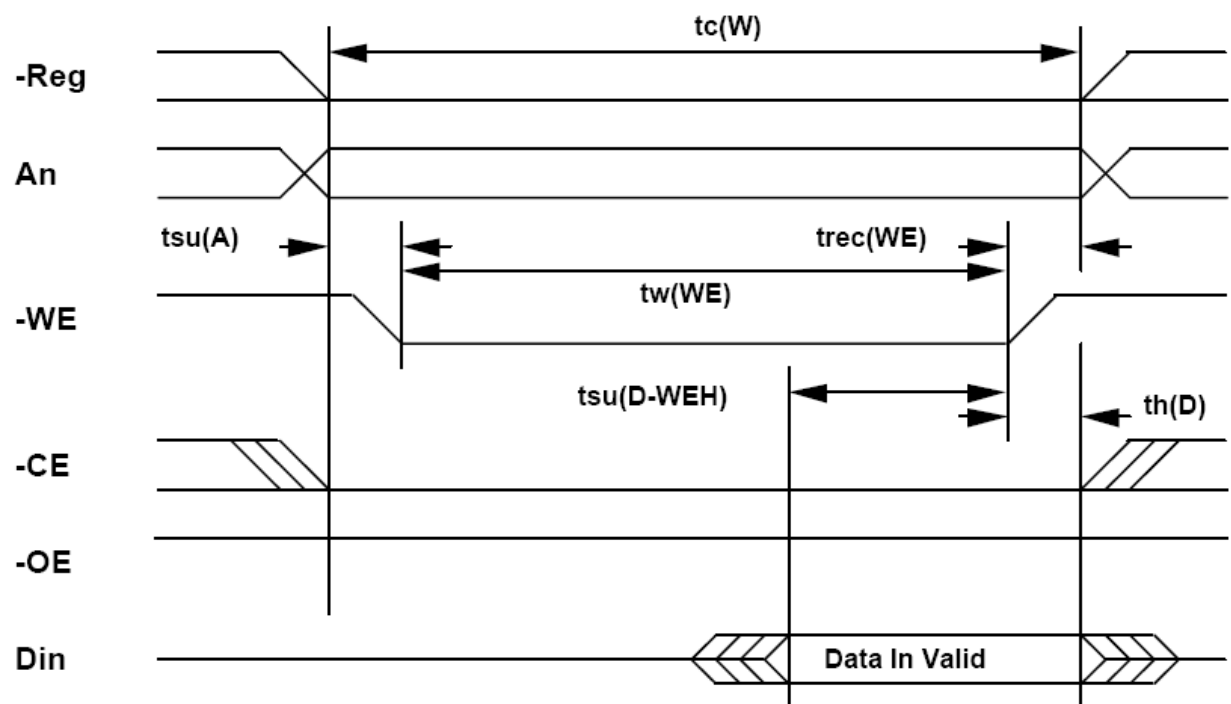**Fig. 6.17 Attribute Memory Read Timing Diagram**
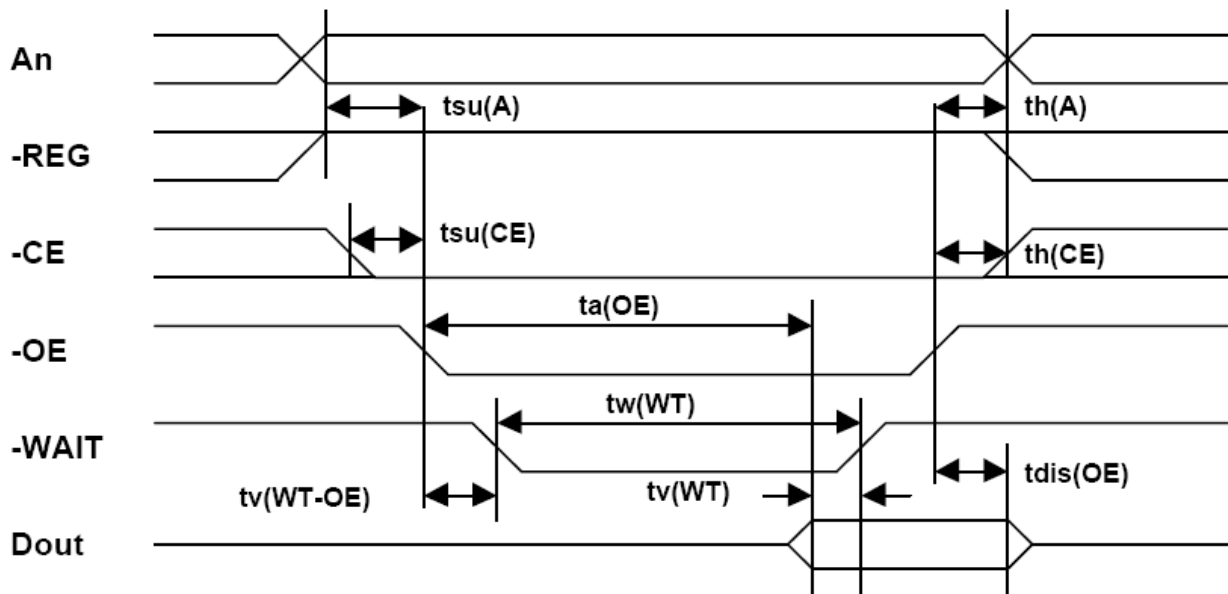

Fig. 6.18 Attribute Memory Write Timing Diagram
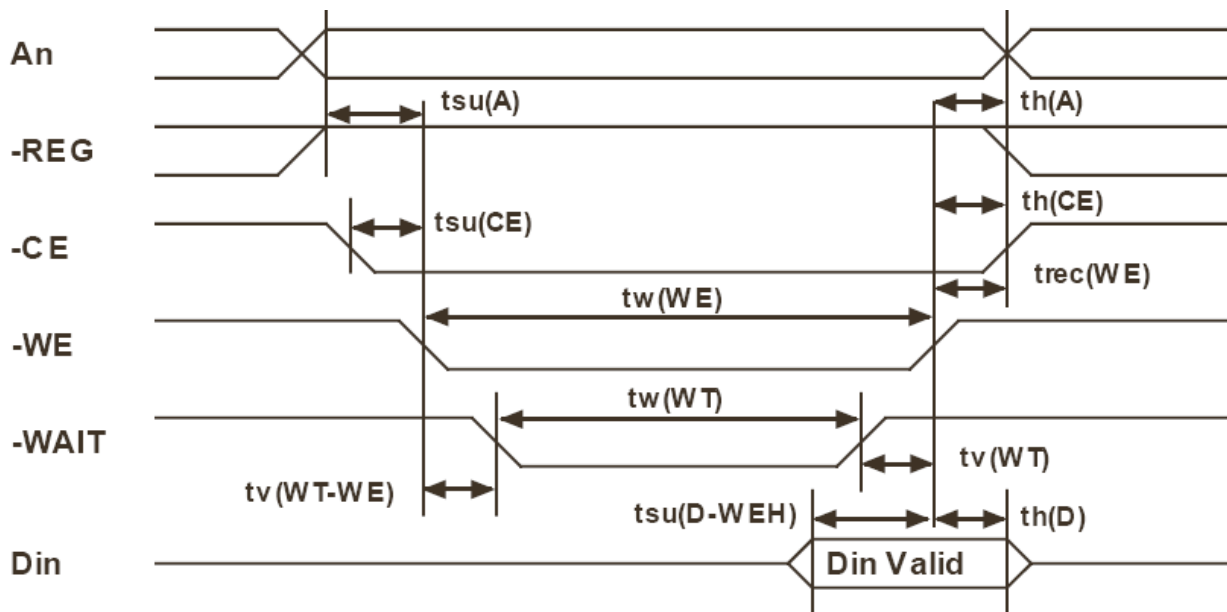
Fig. 6.19 Common Memory Read Timing Diagram

Fig. 6.20 Common Memory Write Timing Diagram

6.6 Analog Electrical Characterisitcs

6.6.1 *ADC*

Name	Max.	Min.	Unit
Input clock frequency	20	----	MHz
Power dissipation current	4 (at 3.3V)	3.1 (at 3.3V)	mA
Power current	100	----	nA
Sampling Rate	150	----	KHz
Signal-to-noise-ratio (SNR)	25.2	23.5	dB
Signal-to-noise/distortion-ratio (SNDR)	24.8	22	dB
Differential Nonlinearity Error (DNL)	0.7	0.3	1LSB
Integral Nonlinearity Error (INL)	0.5	0.2	1LSB
Effective Number of Bit (ENOB)	3.85	3.5	bit
S/H circuit sampling jitter check	100	----	mV

7 Package Dimension

MP650UCG Package Outline for LQFP 216 Pin (24mm x 24mm x 1.4mm, Pin Pitch = 0.4mm)

NOTE :
1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 .

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D_1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E_1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°