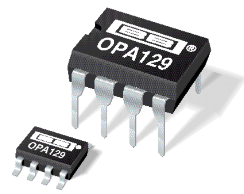
BURR - BROWN®

OPA129



Ultra-Low Bias Current *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- **ULTRA-LOW BIAS CURRENT: 100fA max**
- **LOW OFFSET: 2mV max**
- **LOW DRIFT: 10μV/°C max**
- **HIGH OPEN-LOOP GAIN: 94dB min**
- **LOW NOISE: 15nV/√Hz at 10kHz**
- **PLASTIC DIP and SOIC PACKAGE**

APPLICATIONS

- **PHOTODETECTOR PREAMP**
- **CHROMATOGRAPHY**
- **ELECTROMETER AMPLIFIERS**
- **MASS SPECTROMETER**
- **pH PROBE AMPLIFIER**
- **ION GAGE MEASUREMENT**

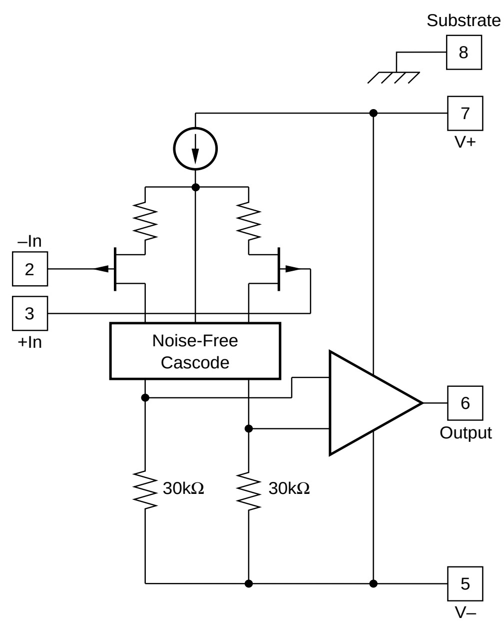
DESCRIPTION

The OPA129 is an ultra-low bias current monolithic operational amplifier offered in an 8-pin PDIP and SO-8 package. Using advanced geometry dielectrically-isolated FET (***Difet***®) inputs, this monolithic amplifier achieves a high performance level.

Difet fabrication eliminates isolation-junction leakage current—the main contributor to input bias current with conventional monolithic FETs. This reduces input bias current by a factor of 10 to 100. Very low input bias current can be achieved without resorting to small-geometry FETs or CMOS designs which can suffer from much larger offset voltage, voltage noise, drift, and poor power supply rejection.

The OPA129's special pinout eliminates leakage current that occurs with other op amps. Pins 1 and 4 have no internal connection, allowing circuit board guard traces—even with the surface-mount package version.

OPA129 is available in 8-pin DIP and SO-8 packages, specified for operation from –40°C to +85°C.



Simplified Circuit

Difet® Burr-Brown Corp.

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SBOS026

SPECIFICATIONS

ELECTRICAL

At V_S = ±15V and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

		OPA129PB, UB			OPA129P, U			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT BIAS CURRENT[1]	V_{CM} = 0V		±30	±100		*	±250	fA
vs Temperature			Doubles every 10°C			*		
INPUT OFFSET CURRENT	V_{CM} = 0V		±30			*		fA
OFFSET VOLTAGE								
Input Offset Voltage	V_{CM} = 0V		±0.5	±2		±1	±5	mV
vs Temperature			±3	±10		±5		µV/°C
Supply Rejection	V_S = ±5V to ±18V		±3	±100		*	*	µV/V
NOISE								
Voltage	f = 10Hz		85			*		nV/√Hz
	f = 100Hz		28			*		nV/√Hz
	f = 1kHz		17			*		nV/√Hz
	f = 10kHz		15			*		nV/√Hz
	f_B = 0.1Hz to 10Hz		4			*		µVp-p
Current	f = 10kHz		0.1			*		fA/√Hz
INPUT IMPEDANCE								
Differential			10^{13} || 1			*		Ω || pF
Common-Mode			10^{15} || 2			*		Ω || pF
VOLTAGE RANGE								
Common-Mode Input Range		±10	±12		*	*		V
Common-Mode Rejection	V_{IN} = ±10V	80	118		*	*		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	R_L ≥ 2kΩ	94	120		*	*		dB
FREQUENCY RESPONSE								
Unity Gain, Small Signal			1			*		MHz
Full Power Response	20Vp-p, R_L = 2kΩ		47			*		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2.5		*	*		V/µs
Settling Time:	G = –1, R_L = 2kΩ, 10V Step							
0.1%			5			*		µs
0.01%			10			*		µs
Overload Recovery, 50% Overdrive[2]	G = –1		5			*		µs
RATED OUTPUT								
Voltage Output	R_L = 2kΩ	±12	±13		*	*		V
Current Output	V_O = ±12V	±6	±10		*	*		mA
Load Capacitance Stability	Gain = +1		1000			*		pF
Short-Circuit Current			±35	±55		*	*	mA
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range, Derated Performance		±5		±18	*		*	V
Current, Quiescent	I_O = 0mA		1.2	1.8		*	*	mA
TEMPERATURE								
Specification	Ambient Temperature	–40		+85	*		*	°C
Operating	Ambient Temperature	–40		+125	*		*	°C
Storage		–40		+125	*		*	°C
Thermal Resistance	θ_{JA}, Junction-to-Ambient							
PDIP—"P"			90			*		°C/W
SOIC—"U"			100			*		°C/W

NOTES: (1) High-speed automated test. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Differential Input Voltage	V– to V+
Input Voltage Range	V– to V+
Storage Temperature Range	–40°C to +125°C
Operating Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 10s; SOIC 3s)	+300°C
Output Short Circuit Duration[1]	Continuous
Junction Temperature (T_J)	+150°C

NOTE: (1) Short circuit may be to power supply common at +25°C ambient.

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

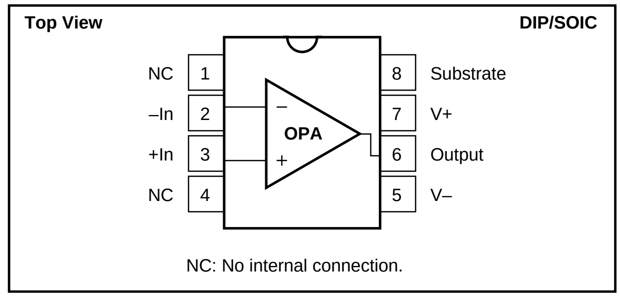
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA129P	8-pin Plastic DIP	006
OPA129PB	8-pin Plastic DIP	006
OPA129U	8-pin SOIC	182
OPA129UB	8-pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

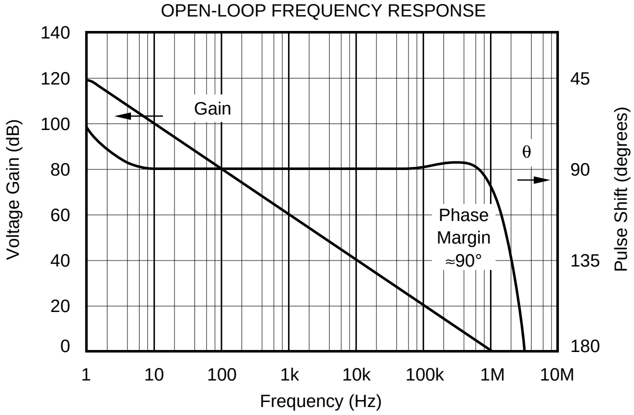
CONNECTION DIAGRAM



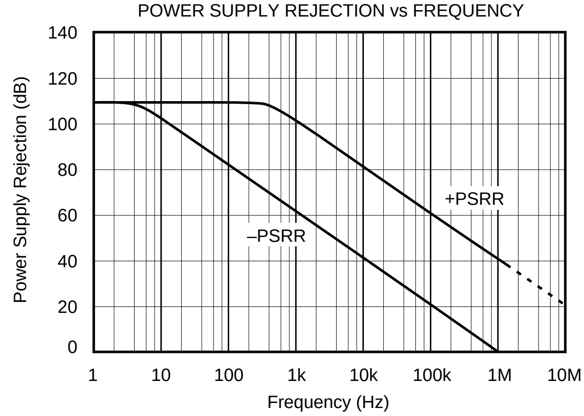
TYPICAL PERFORMANCE CURVES

T_A = +25°C, +15VDC, unless otherwise noted.

OPEN-LOOP FREQUENCY RESPONSE

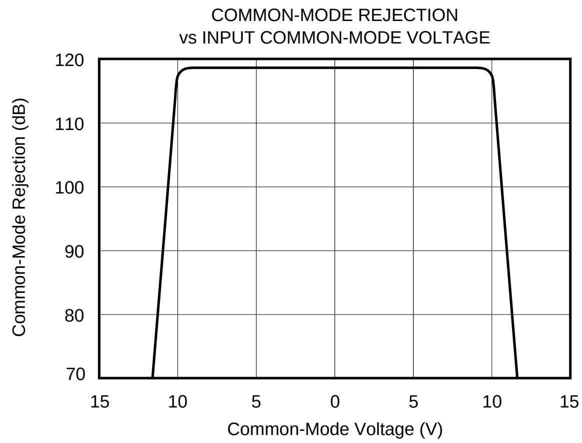


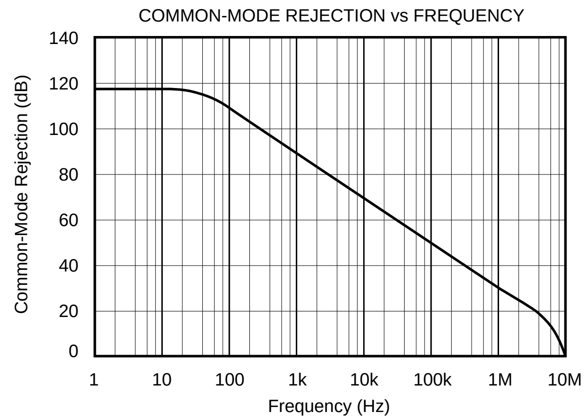
POWER SUPPLY REJECTION vs FREQUENCY

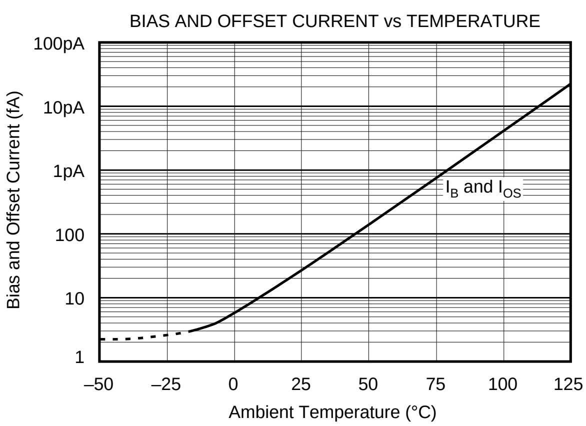


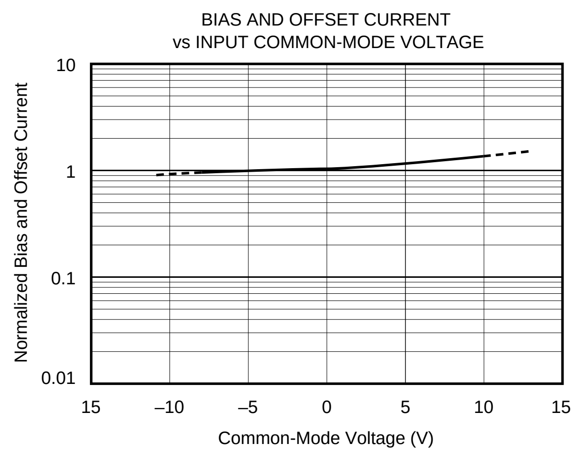
TYPICAL PERFORMANCE CURVES (CONT)

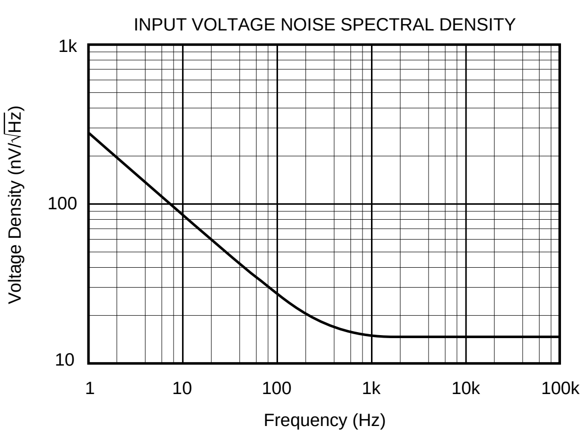
T_A = +25°C, +15VDC, unless otherwise noted.

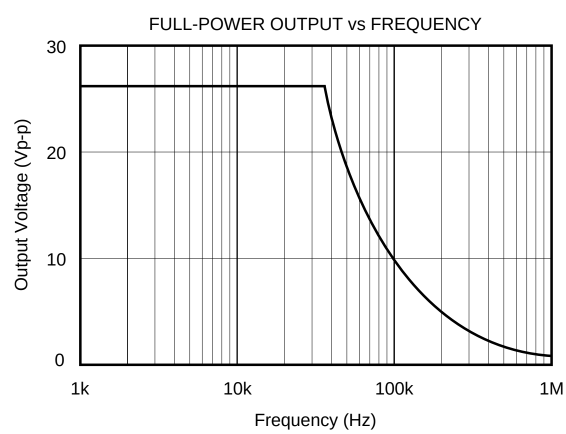






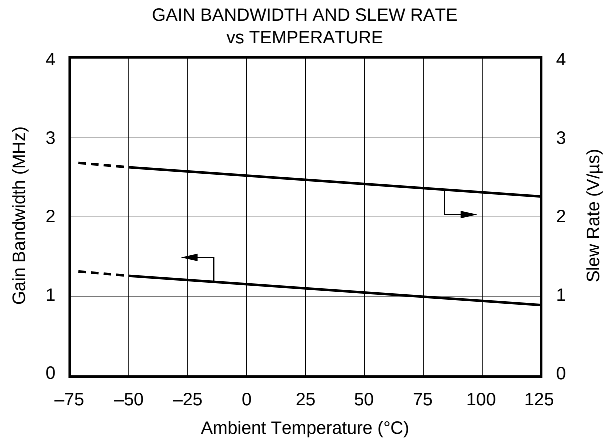


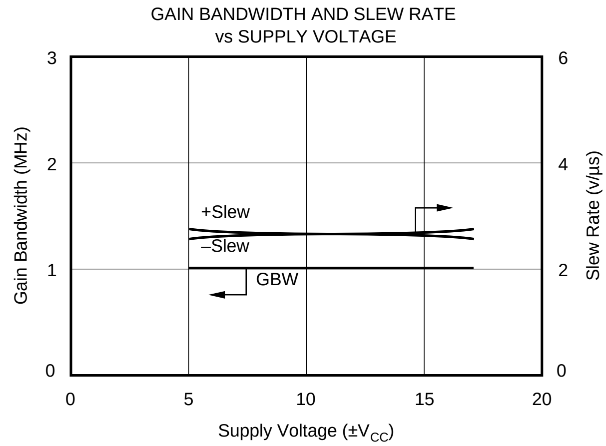


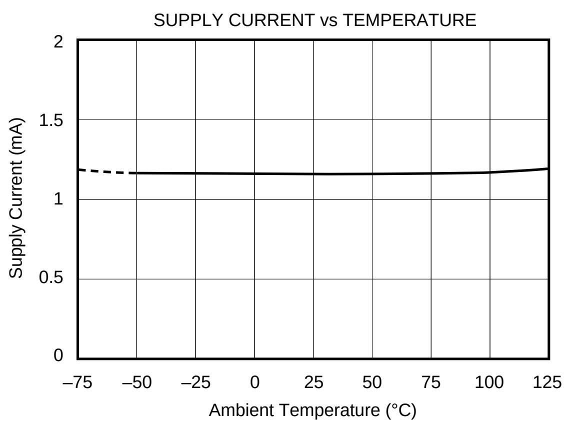


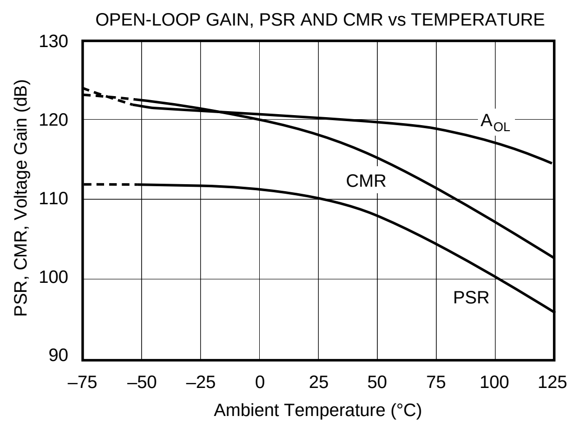
TYPICAL PERFORMANCE CURVES (CONT)

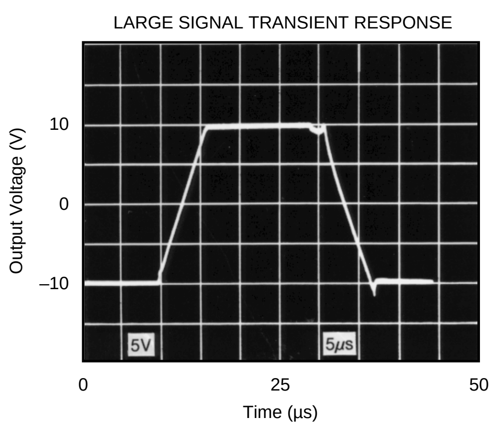
T_A = +25°C, +15VDC, unless otherwise noted.

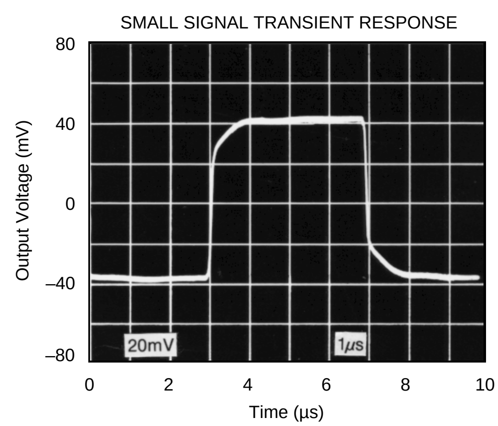






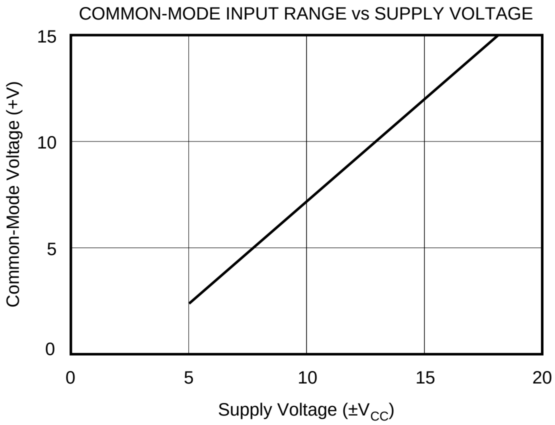


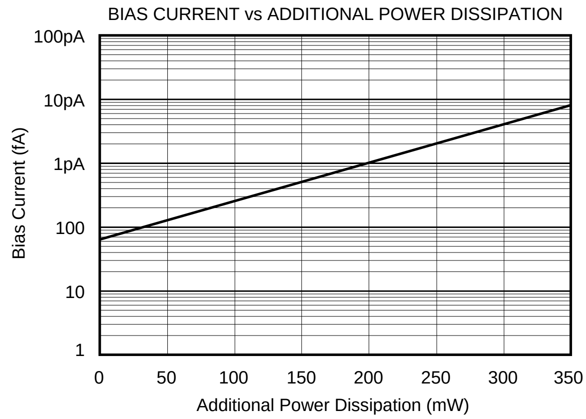




TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, +15VDC, unless otherwise noted.





APPLICATIONS INFORMATION

NON-STANDARD PINOUT

The OPA129 uses a non-standard pinout to achieve lowest possible input bias current. The negative power supply is connected to pin 5—see Figure 1. This is done to reduce the leakage current from the V- supply (pin 4 on conventional op amps) to the op amp input terminals. With this new pinout, sensitive inputs are separated from both power supply pins.

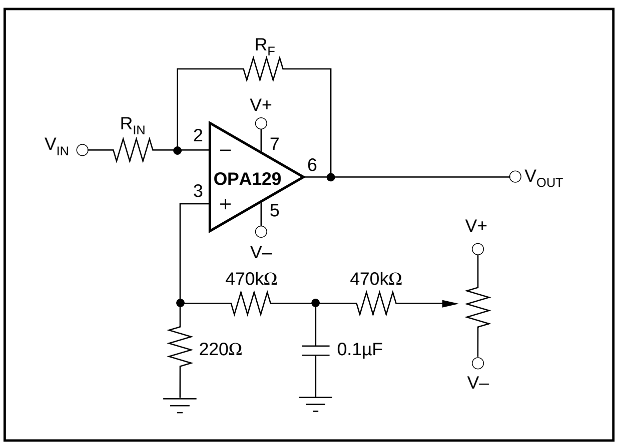


FIGURE 1. Offset Adjust Circuit.

OFFSET VOLTAGE TRIM

The OPA129 has no conventional offset trim connections. Pin 1, next to the critical inverting input, has no internal connection. This eliminates a source of leakage current and allows guarding of the input terminals. Pin 1 and pin 4, next to the two input pins, have no internal connection. This allows an optimized circuit board layout with guarding—see "circuit board layout."

Due to its laser-trimmed input stage, most applications do not require external offset voltage trimming. If trimming is required, the circuit shown in Figure 1 can be used. Power supply voltages are divided down, filtered and applied to the non-inverting input. The circuit shown is sensitive to variation in the supply voltages. Regulation can be added, if needed.

GUARDING AND SHIELDING

Ultra-low input bias current op amps require precautions to achieve best performance. Leakage current on the surface of circuit board can exceed the input bias current of the amplifier. For example, a circuit board resistance of $10^{12}\Omega$ from a power supply pin to an input pin produces a current of 15pA—more than one-hundred times the input bias current of the op amp.

To minimize surface leakage, a guard trace should completely surround the input terminals and other circuitry connecting to the inputs of the op amp. The DIP package should have a guard trace on both sides of the circuit board. The guard ring should be driven by a circuit node equal in potential to the op amp inputs—see Figure 2. The substrate, pin 8, should also be connected to the circuit board guard to assure that the amplifier is fully surrounded by the guard potential. This minimizes leakage current and noise pick-up.

Careful shielding is required to reduce noise pickup. Shielding near feedback components may also help reduce noise pick-up.

Triboelectric effects (friction-generated charge) can be a troublesome source of errors. Vibration of the circuit board, input connectors and input cables can cause noise and drift. Make the assembly as rigid as possible. Attach cables to avoid motion and vibration. Special low noise or low leakage cables may help reduce noise and leakage current. Keep all input connections as short possible. Surface-mount components may reduce circuit board size and allow a more rigid assembly.

CIRCUIT BOARD LAYOUT

The OPA129 uses a new pinout for ultra low input bias current. Pin 1 and pin 4 have no internal connection. This allows ample circuit board space for a guard ring surrounding the op amp input pins—even with the tiny SO-8 surface-mount package. Figure 3 shows suggested circuit board layouts. The guard ring should be connected to pin 8 (substrate) as shown. It should be driven by a circuit node equal in potential to the input terminals of the op amp—see Figure 2 for common circuit configurations.

TESTING

Accurately testing the OPA129 is extremely difficult due to its high performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current.

Inaccurate bias current measurements can be due to:

1. Test socket leakage,
2. Unclean package,
3. Humidity or dew point condensations,
4. Circuit contamination from fingerprints or anti-static treatment chemicals,
5. Test ambient temperature,
6. Load power dissipation,
7. Mechanical stress,
8. Electrostatic and electromagnetic interference.

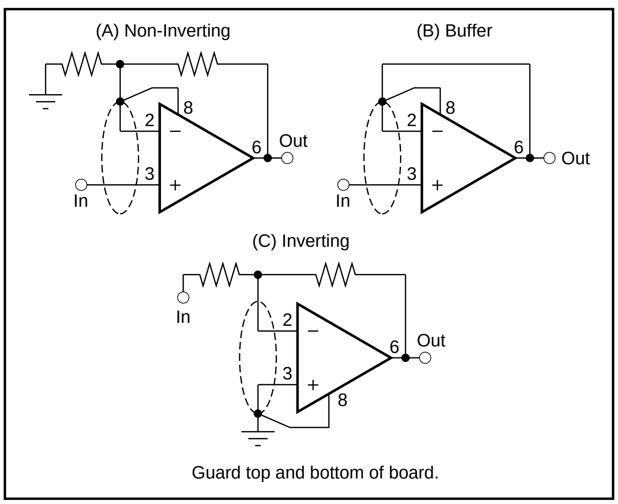


FIGURE 2. Connection of Input Guard.

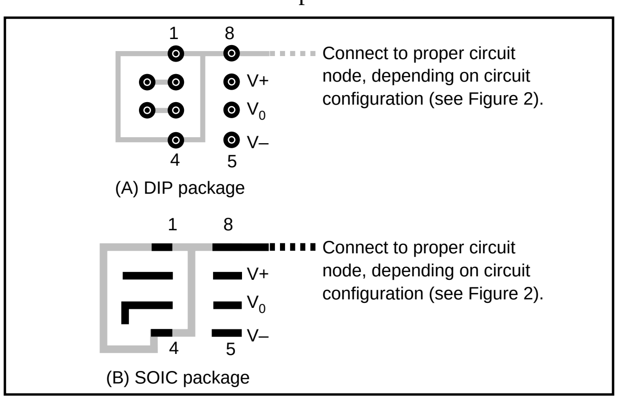


FIGURE 3. Suggested Board Layout for Input Guard.

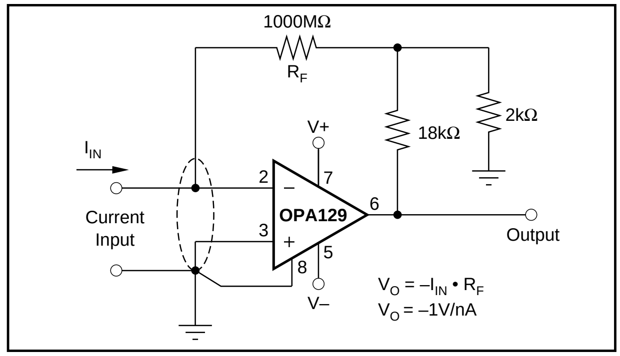


FIGURE 4. Current-to-Voltage Converter.

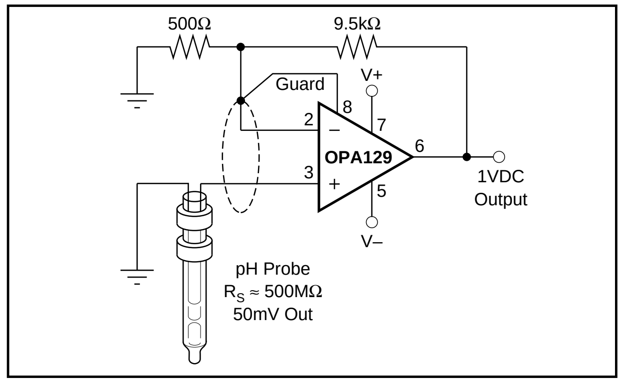


FIGURE 5. High Impedance ($10^{15}\Omega$) Amplifier.

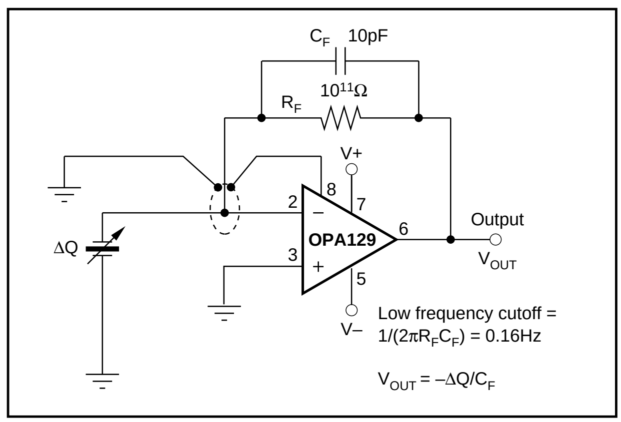


FIGURE 6. Piezoelectric Transducer Charge Amplifier.

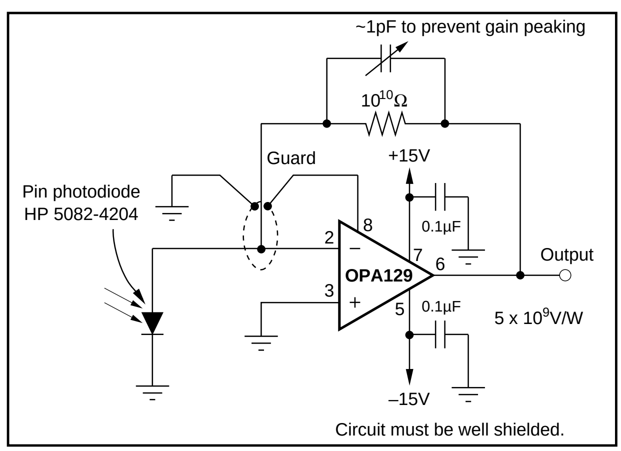


FIGURE 7. Sensitive Photodiode Amplifier.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA129P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA129PB	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA129U	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA129UB	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA129UB/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA129UB/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA129UBE4	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA129UE4	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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