Product *Specification*

Customer: _____

Product No.: TMT035DNAFWU18-1

Date: 2007/7/20

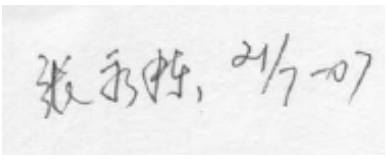
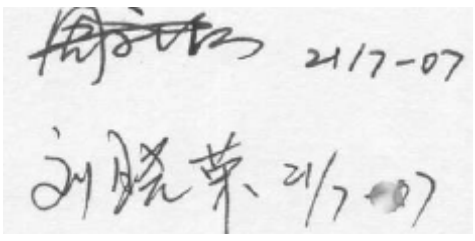
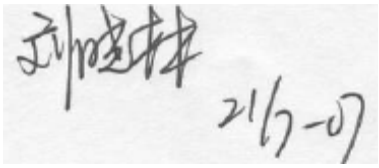
Version: 0.0

■ **Preliminary Specification**

□ **Final Specification**

For Customer's Comment

Approved	Customer's Comment

Approved By	Checked By	Prepared By
		

This specification is subject to change without notice.

Please contact Tianma or its representative before designing your product based on this specification.

Revision Record

Date	Rev. No.	Page	Revision Items
2007/7/20	0.0		Initial Release

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1. Description

TMT035DNAFWU18-1 is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, FPC and a back light unit. The resolution of a 3.5″ contains 320 x 240 pixels and can display up to 16.7M colors. This product accords with RoHS environmental criterion.

2. Applications

- Visible telephone
- Digital Still Camera (DSC)
- Portable Multimedia Player (PMP)
- Global Position System (GPS)

3. Features

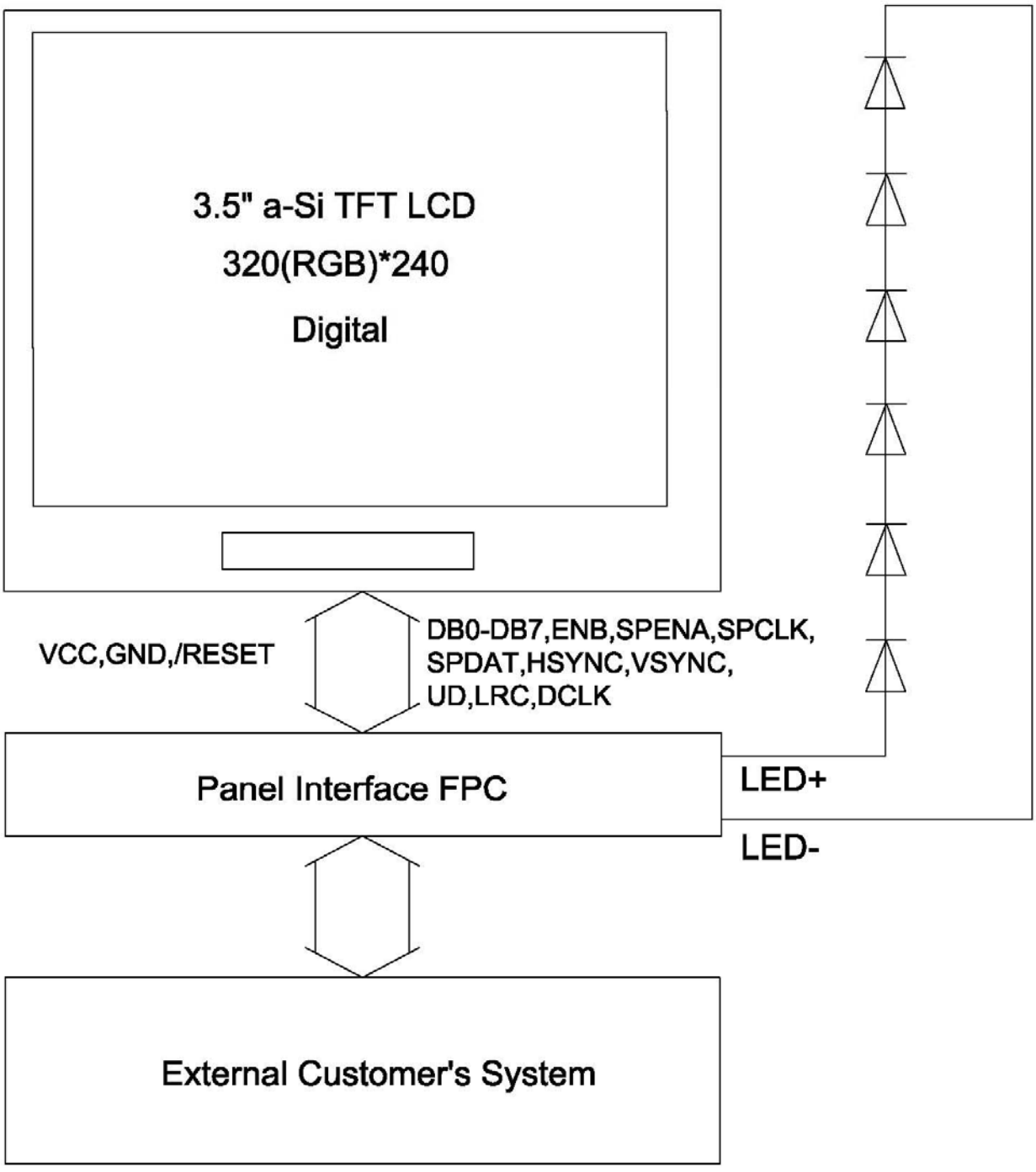
- 8 bits color depth
- Signal Interface is selectable: S-RGB/CCIR656/601
- Built-in charge-pump circuits (including VGH,VGL,VCOM set-up circuits)

4. General Specifications

Item	Specification	Unit	Remark
Display Mode	Transmissive / Normally White	-	-
Display Technology	α-Si TFT active matrix	-	-
Outline Dimension	76.9(H)×63.9(V)×3.15(T)	mm	Note 4-1
Active Area	70.08(H)X52.56(V)	mm	-
Resolution	320X(RGB)X240	dots	-
Pixel Pitch	219X219	μm	-
Pixel Configuration	RGB Stripe	-	-
Weight	TBD	g	-
Backlight	6*LED	-	-
Luminance	250(Typ.)	cd/m^2	-
Surface Treatment	Anti-Glare	-	-
Signal Interface	S-RGB/CCIR656/601	-	-
Viewing Direction	12	o'clock	Note 4-2
Power consumption	409(Typ.)	mW	Note 4-3

Note 4-1: Refer to the mechanical drawing on page25.
Note 4-2: Refer the definition of the viewing direction on page22.
Note 4-3: The Power Consumption is a calculated reference value (P_{LCD}+P_{LED}).

5. Block Diagram



6. Interface

(Recommended connector: OMRON XF2M-3615-1A)

Pin No.	Symbol	I/O	Description	Remark
1	LED-	-	Backlight LED Ground	-
2	LED+	-	Backlight LED Power	-
3	NC	-	No Connection	-
4	NC	-	No Connection	-
5	NC	-	No Connection	-
6	/REST	I	Hardware Reset	-
7	SPENA	I	SPI Interface Data Enable Signal	Note 6-1
8	SPCLK	I	SPI Interface Data Clock	Note 6-1
9	SPDAT	I	SPI Interface Data	Note 6-1
10	DB0	I	Data Bit 0	-
11	DB1	I	Data Bit 1	-
12	DB2	I	Data Bit 2	-
13	DB3	I	Data Bit 3	-
14	DB4	I	Data Bit 4	-
15	DB5	I	Data Bit 5	-
16	DB6	I	Data Bit 6	-
17	DB7	I	Data Bit 7	-
18	HSYNC	I	Horizontal Sync Input	-
19	VSYNC	I	Vertical Sync Input	-
20	DCLK	I	Dot Data Clock	-
21	UD	I	Up/Down scan direction setting	Note 6-2
22	NC	-	No Connection	-
23	VCC	I	Supply Voltage for Source Driver	VCC=3.3V
24	LRC	I	Left/Right scan direction setting	Note 6-2
25	NC	-	No Connection	-
26	NC	-	No Connection	-
27	NC	-	No Connection	-
28	NC	-	No Connection	-
29	NC	-	No Connection	-
30	NC	-	No Connection	-
31	NC	-	No Connection	-
32	NC	-	No Connection	-
33	NC	-	No Connection	-
34	ENB	I	Data Enable Input	-
35	GND	I	Power Ground(0V)	-
36	GND	I	Power Ground(0V)	-

Note 6-1: SPENA, SPCLK, SPDAT must be connected to referenced control pins to enable the SPI initialization, to let the LCD give a good display (reference to Page14~16).

Note 6-2: Select the output shift direction of the gate driver and source driver. These pins can be adjusted by software commands (reference to Page16~17), the hardware provides default setting only.

7. Absolute Maximum Ratings

(GND=0V, Ta=25°C)

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VCC	-0.3	+4.0	V	-
Signal Input Voltage	V_{SIG}	-0.3	+3.6	V	-
Operation Temperature(Ambient)	T_{OPR}	-20	+70	°C	Note 7-1,2
Storage Temperature(Ambient)	T_{STG}	-30	+80	°C	Note 7-1,2,3,4

Note 7-1: No parameter is allowed to exceed to the temperature range.
Note 7-2: 95% RH Max. (40 °C ≥ Ta)
Maximum wet-bulb temperature at 39°C or less. (Ta >40 °C) No dew condensation.
Note 7-3: Only operation is guarantied at operating temperature. Contrast, response time and another display quality are evaluated at +25°C.
Note 7-4: The ambient temperature, when backlight is on. (Reference)

8. Electrical Conditions

8.1. TFT- LCD Panel Driving Section

(Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for VCC	VCC	2.5	3.3	3.6	V	-
VCC Operation Current	IVCC	-	7.5	-	mA	Note 8-1
Signal Input Voltage	V_{SIG}	0	-	VCC	V	-
Signal Voltage High	V_{SIG-H}	0.8VCC	-	VCC	V	-
Signal Voltage Low	V_{SIG-L}	0	-	0.2VCC	V	-
Power Consumption	P_{LCD}	-	25	-	mW	Note 8-2

Note 8-1: The current IVCC is tested under the condition of VCC=3.3V, displaying a 16-grayscale graphic.
TNote 8-2: The P_{LCD} is calculated by a reference value of VCC×IVCC.

8.2. Backlight Driving Section

Fig. 8-2 LED Circuit

(Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Voltage	V_L	-	19.2	-	V	-
LED Current	I_L	-	20	-	mA	-
Power Consumption	P_{LED}	-	384	-	mW	Note 8-3
Life Time	-	-	(50,000)	-	hr	Note 8-4

Note 8-3: P_{LED} is a calculated reference value ($I_L \times V_L$)

Note 8-4: The “lamp life time” is defined as the module luminance decrease to 50% original luminance at Ta=25℃, I_L=20 mA (This is the reference value).

9. Timing Characteristics and waveform

9.1. Timing Conditions

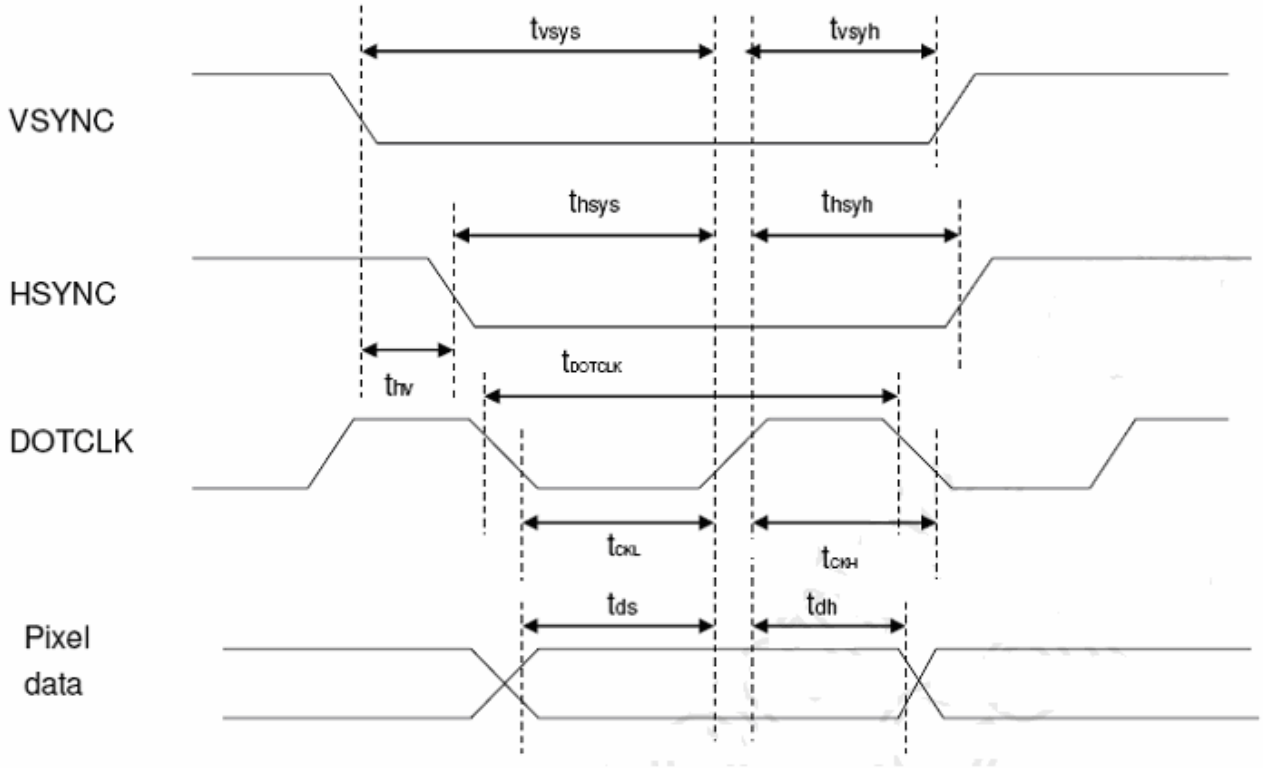


Fig 9.1 Pixel timing

Characteristics	Symbol	Min		Typ		Max		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	fDOTCLK	-		6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-		ns
Vertical Sync Setup Time	tvsys	20	10	-		-		ns
Vertical Sync Hold Time	tvsyh	20	10	-		-		ns
Horizontal Sync Setup Time	thsys	20	10	-		-		ns
Horizontal Sync Hold Time	thsyh	20	10	-		-		ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-		-		ns
DOTCLK High Period	tCKH	50	15	-		-		ns
Data Setup Time	tds	12	10	-		-		ns
Data hold Time	tdh	12	10	-		-		ns
Reset pulse width	tRES	10		-		-		us

Note: External clock source must be provided to DOTCLK pin of HX8238-A. The driver will not operate if absent of the clocking signal.

Table 9.1 Pixel timing

9.2. CCIR601 Interface

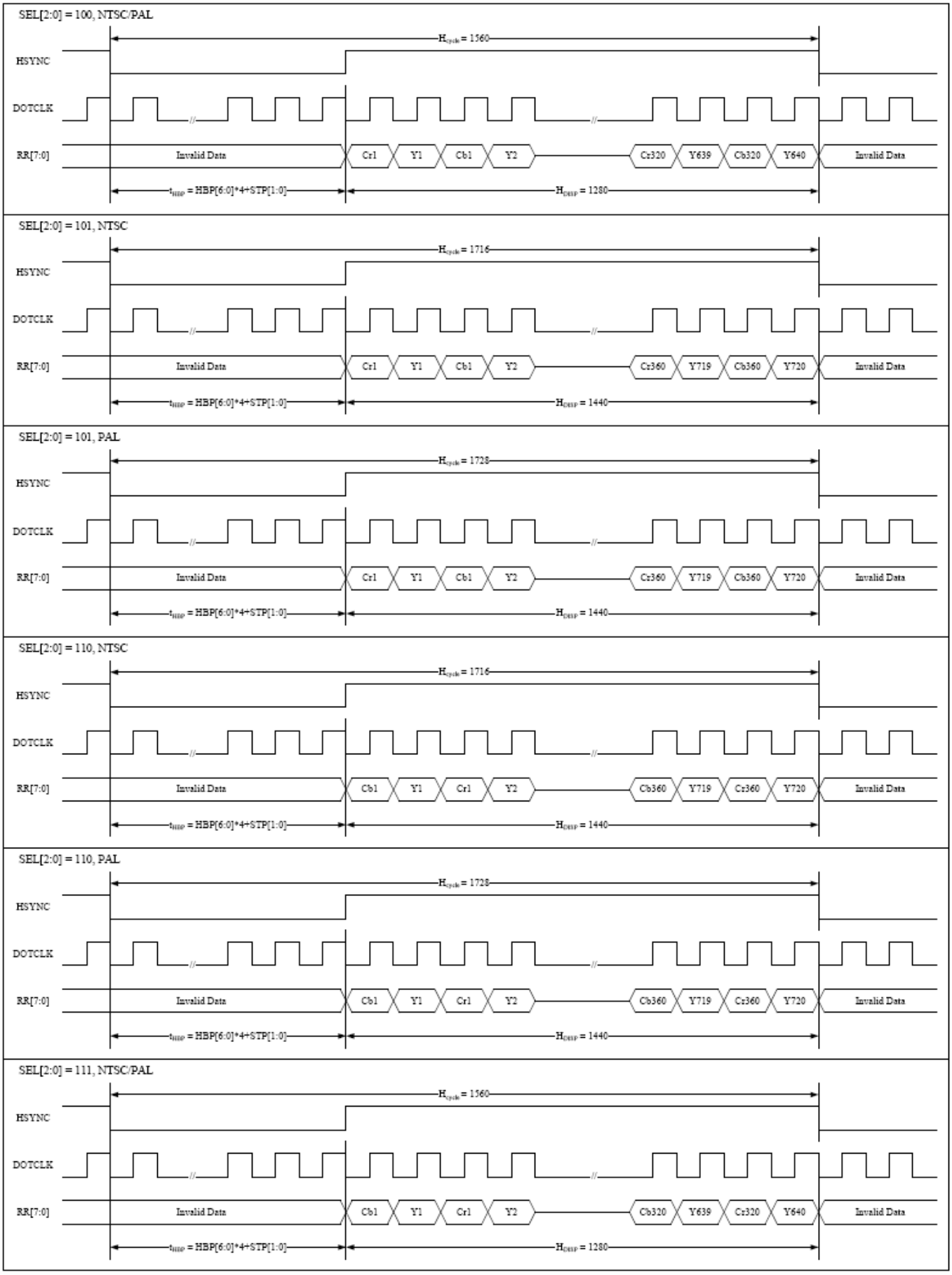


Fig 9.2 CCIR601 horizontal timing

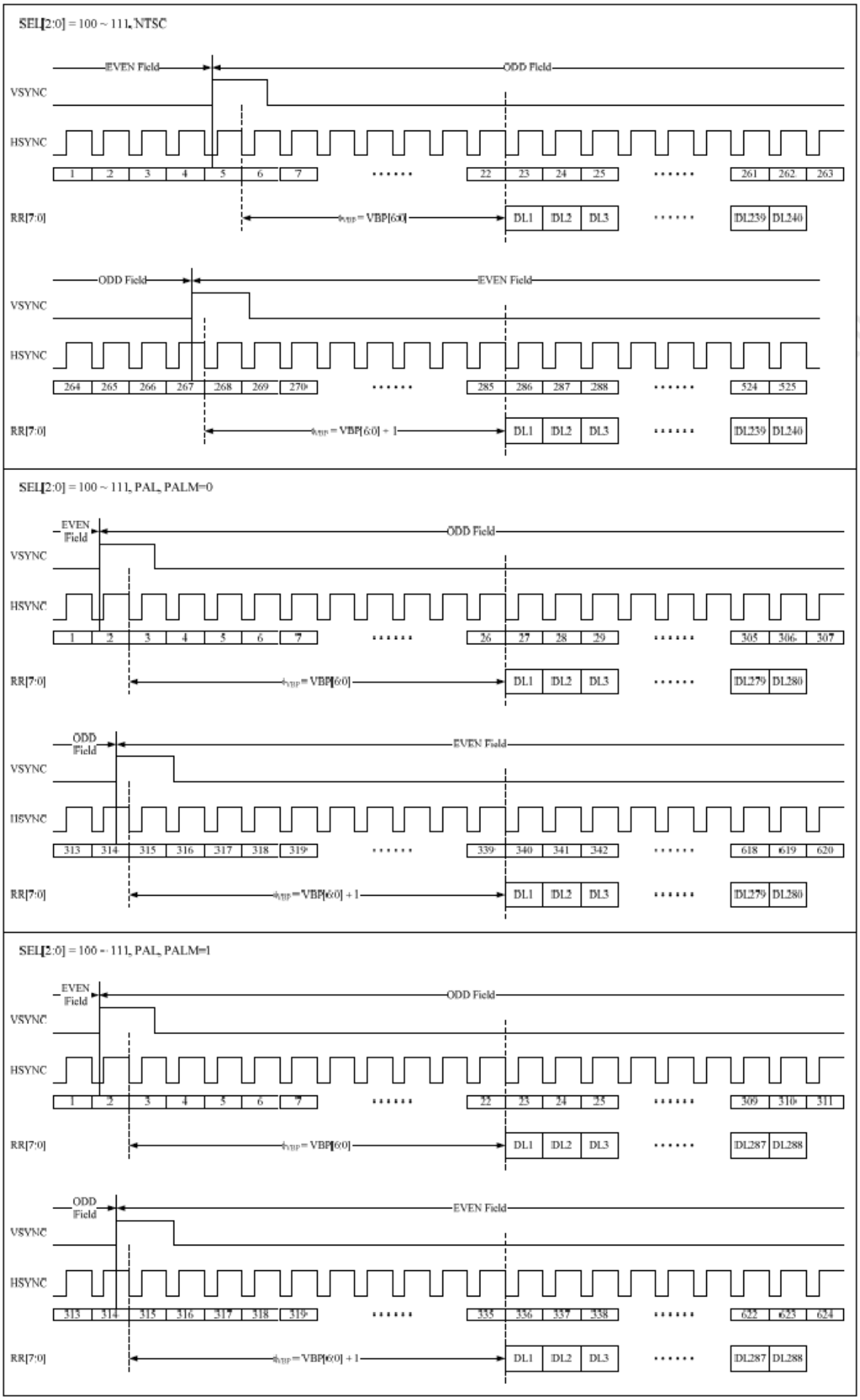


Fig 9.3 CCIR601 vertical timing

9.3. CCIR656 Interface

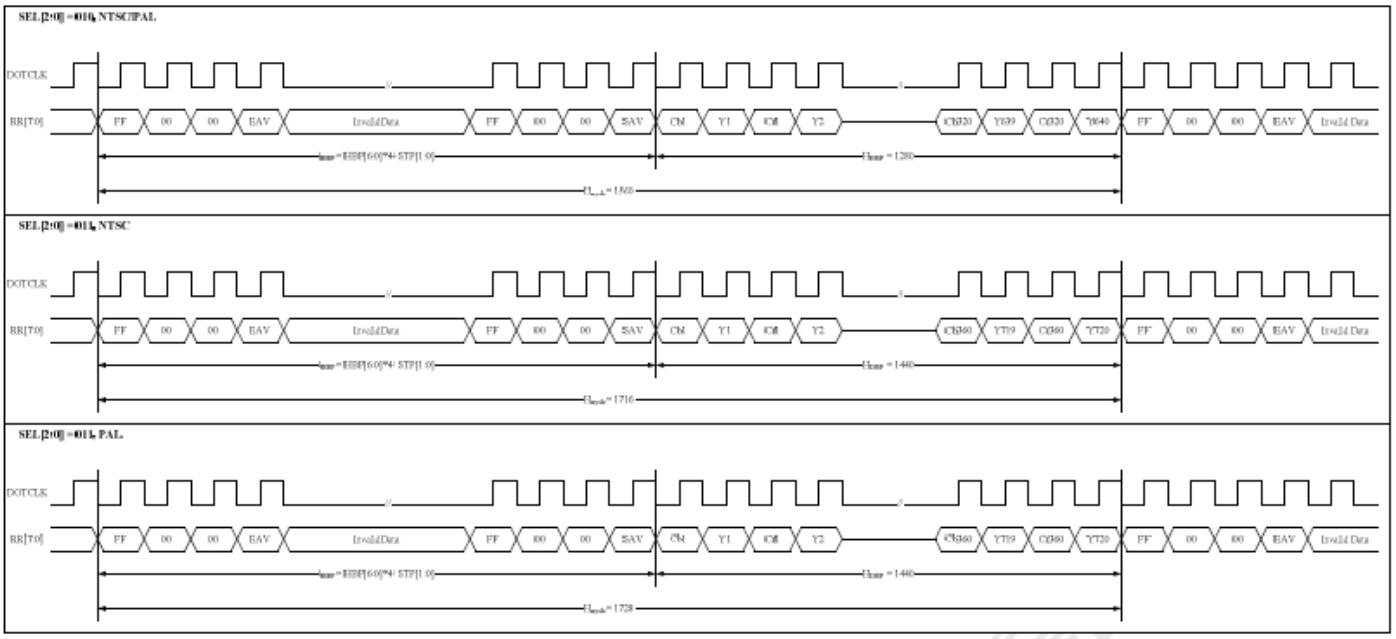
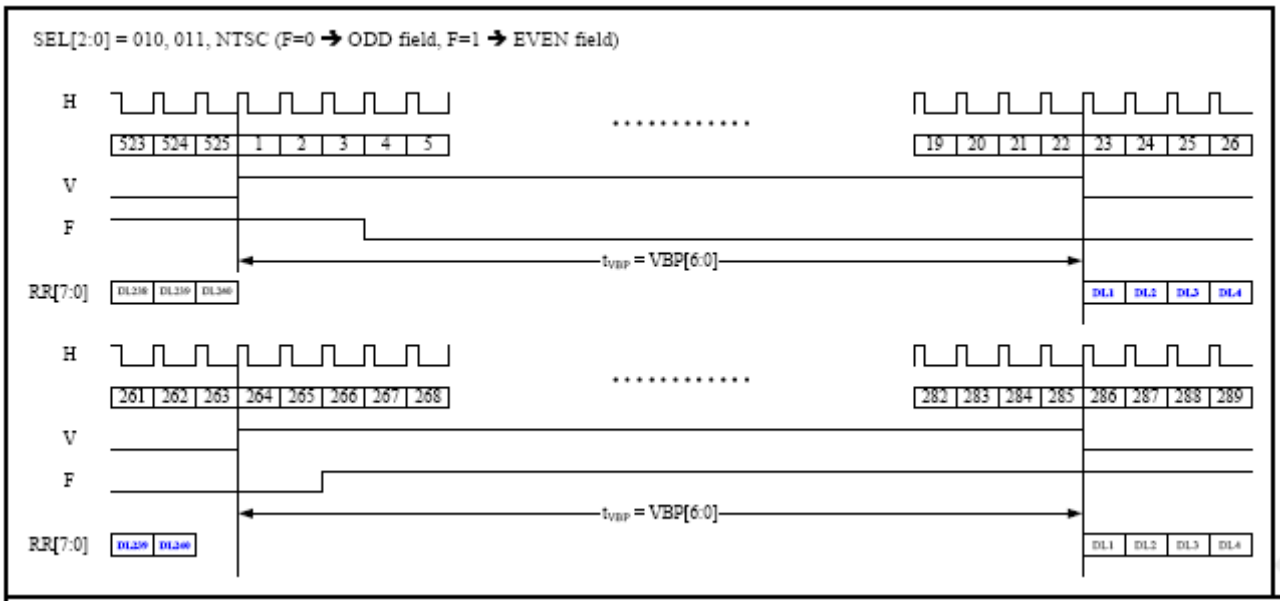


Fig 9.4 CCIR656 horizontal timing



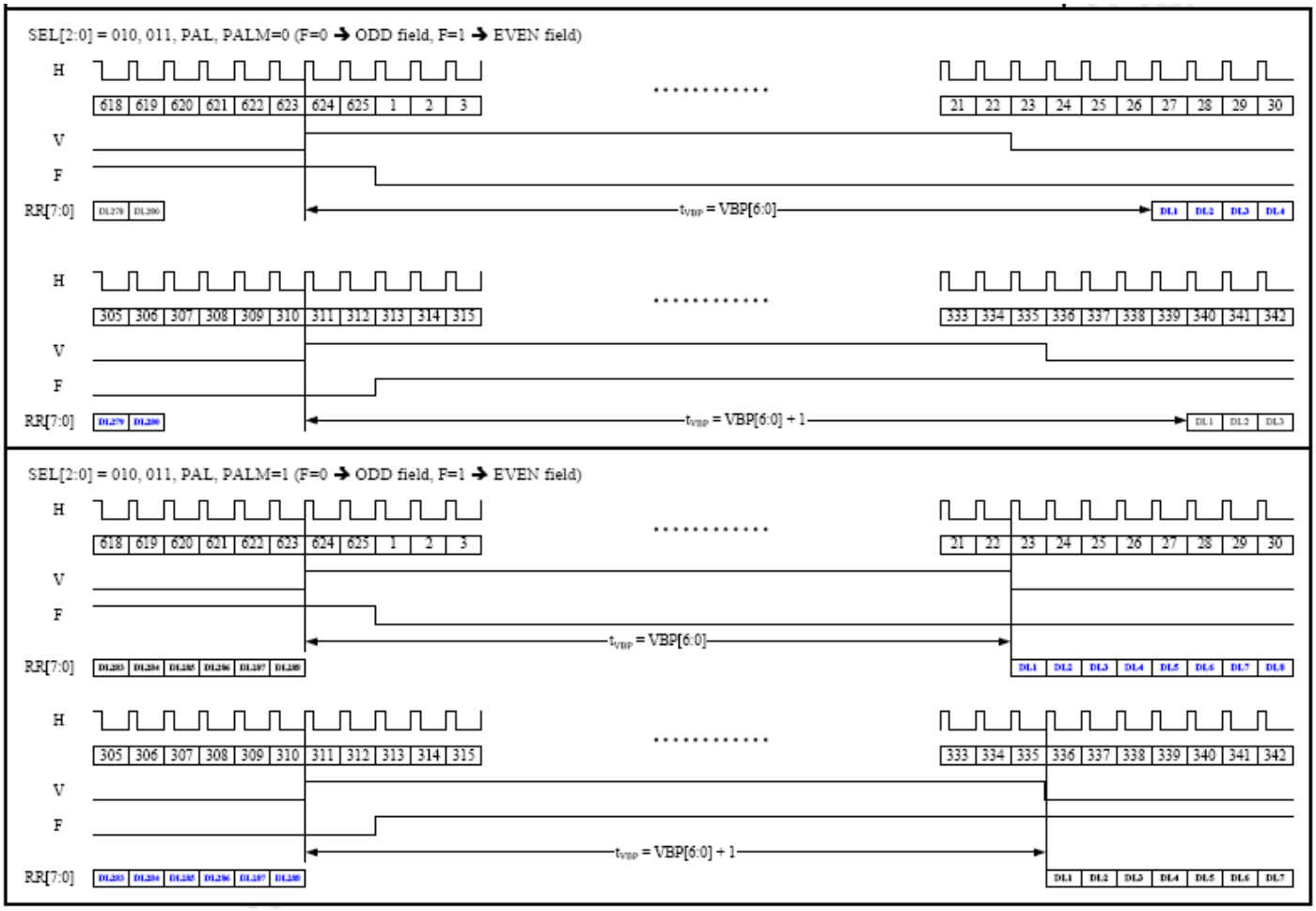


Fig 9.5 CCIR656 vertical timing

9.4. SPI Interface

The SPI is available through the SPENA, SPCLK, SPDAT. The LCD driver recognizes the start of data transfer at the falling edge of SPENA input to initiate the transfer of start byte, and the end of data transfer at the rising edge of SPENA input.

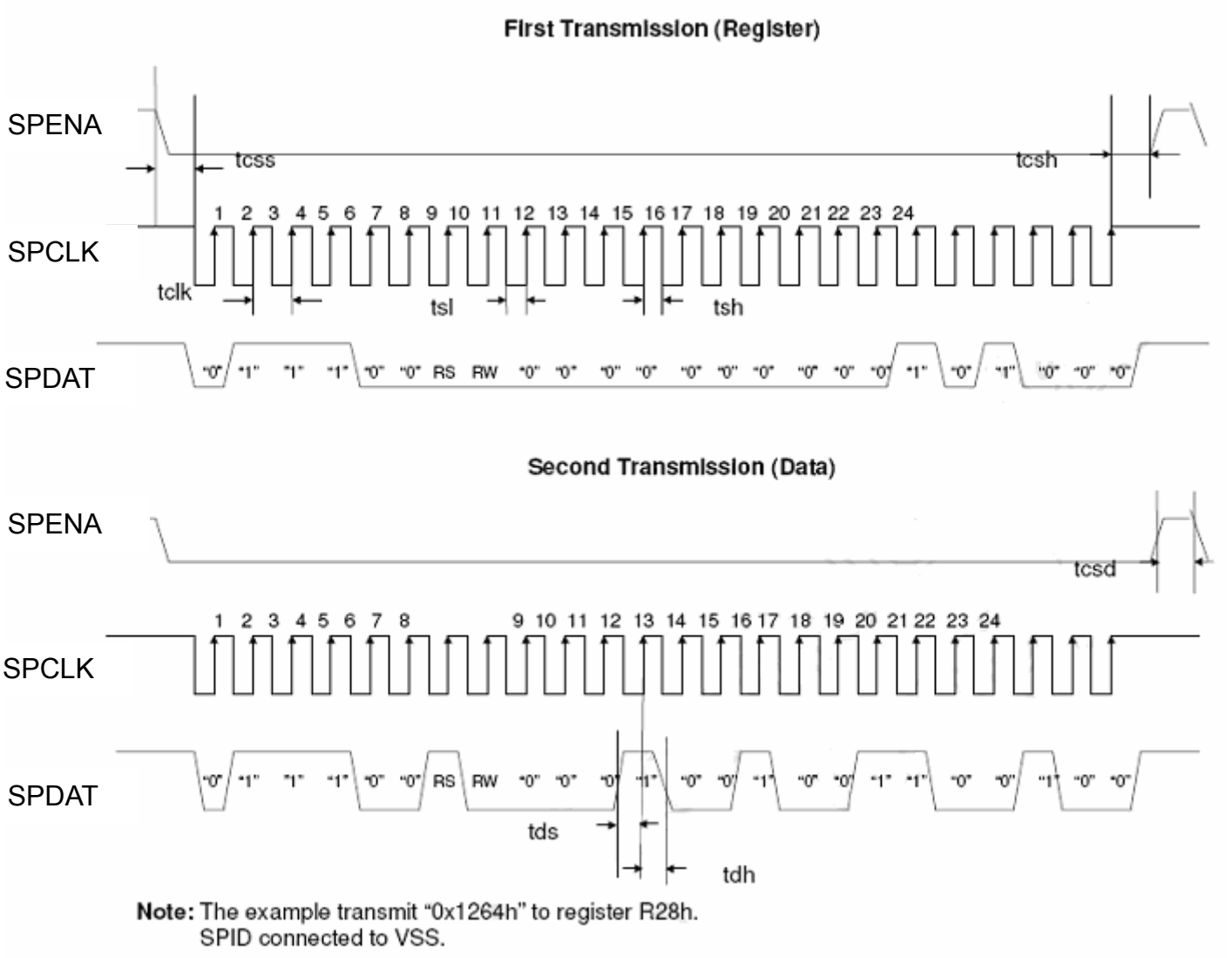


Fig 9.6 SPI interface timing diagram & transaction example

Characteristics	Symbol	Min	Typ	Max	Unit
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Chip Select Setup Time	tcss	0	-	-	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

Table 9.2 SPI timing

Reg#	Hex Code	Register Bit Value
R01h	XX00	RL = X REV = X PINV = X BGR = X SM = "0" TB = X CPE = X
R02h	0200	B/C = "1" NW = "00000000"
R03h	6364	DCT = "0110" BT = "011" BTF = "0" DC = "0110" AP = "010"
R04h	04XX	PALM = "1" BLT = "00" OEA = note 2 SEL = X SWD = X
R05h		GHN="1" XDK="0" GDIS="1" LPF="1" DEP="0" CKP="1" VSP= note 2 HSP="0" DEO="1" DIT="1" PWM="0" FB="100"
R0Ah	4008	BR = "1000000" CON = "01000"
R0Bh	D400	NO = "11" SDT = "01" EQ = "100"
R0Dh	3229	VRC = "011" VDS = "10" VRH = "101001"
R0Eh	3200	VCOMG = "1" VDV = "1001000"
R0Fh	0000	SCN = "00000000"
R16h	9F80	XLIM = "100111111"
R17h		STH = "00" HBP = note 2 VBP = note 2
R1Eh	0052	nOTP = "0" VCM = "1010010"
R30h	0000	PKP1 = "000" PKP0 = "000"
R31h	0407	PKP3 = "100" PKP2 = "111"
R32h	0202	PKP5 = "010" PKP4 = "010"
R33h	0000	PRP1 = "000" PRP0 = "000"
R34h	0505	PKN1 = "101" PKN0 = "101"
R35h	0003	PKN3 = "000" PKN2 = "011"
R36h	0707	PKN5 = "111" PKN4 = "111"
R37h	0000	PRN1 = "000" PRN0 = "000"
R3Ah	0904	VRP1 = "01001" VRP0 = "0100"
R3Bh	0904	VRN1 = "01001" VRN0 = "0100"

Note 1 : X means the bit is refer to the logic stage of the corresponding hardware pin.
Note 2 : The default values of the VSP、OEA、HBP、VBP are automatically set by SEL.

Note 3: RL=LRC; TB=UD.

Default Value auto setting			VSP	OEA[1:0]	HBP[6:0]	VBP[6:0]
SEL[2:0] = 000	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 001	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 010	NTSC		0	01	1000101	0010110
	PAL	PALM=0	0	10	1000101	0011100
		PALM=1				0011000
SEL[2:0] = 011	NTSC		0	01	1000100	0010110
	PAL	PALM=0	0	10	1000111	0011100
		PALM=1				0011000
SEL[2:0] = 100	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100
SEL[2:0] = 101	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 110	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 111	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100

Table 9.3 Registers default value

The interface can be modified by changing the value of R04:

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0

SEL2-0: Define the input interface mode.

SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	Parallel-RGB data format (only support stripe type color filter)	6.5MHz
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Table 9.4 interface type

The scan direction and display can be modified by changing the value of R01:

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	R_L	REV	PINV	BGR	S_M	T_B	CPE	0	0	1	1	1	1	1	1

Note: RL=LRC; TB=UD.

Table 9.5 Scan direction & Display

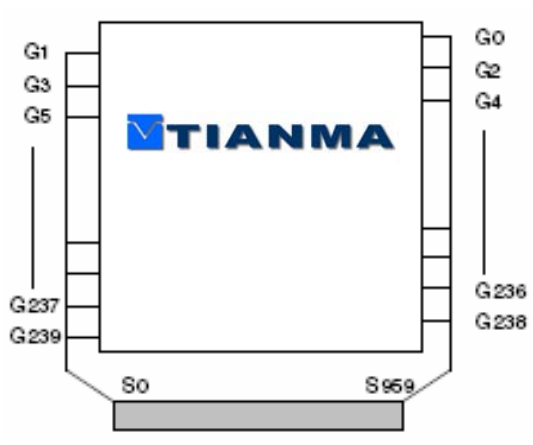
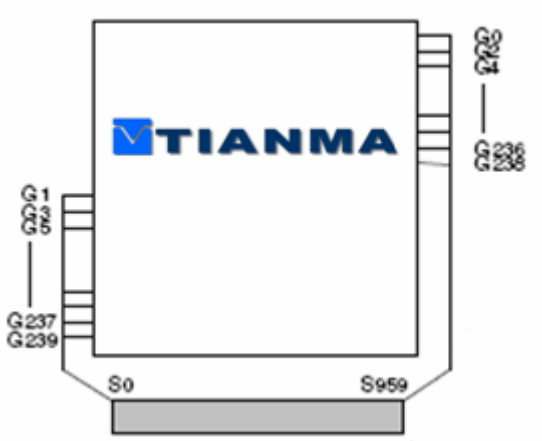
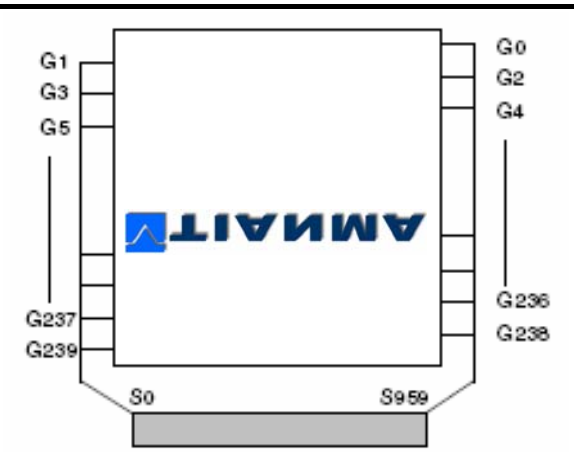
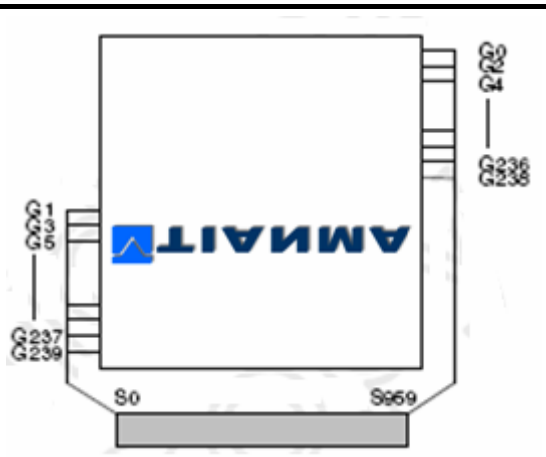
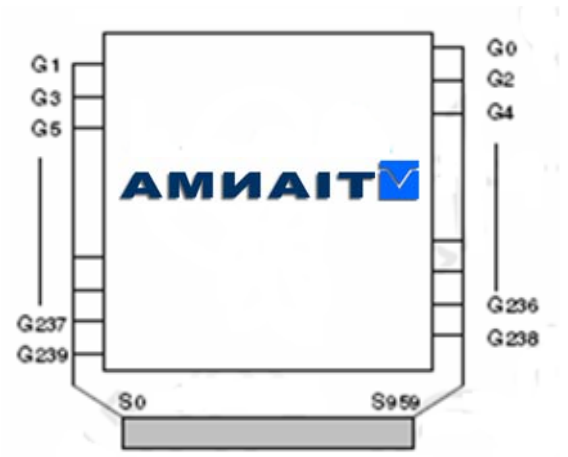
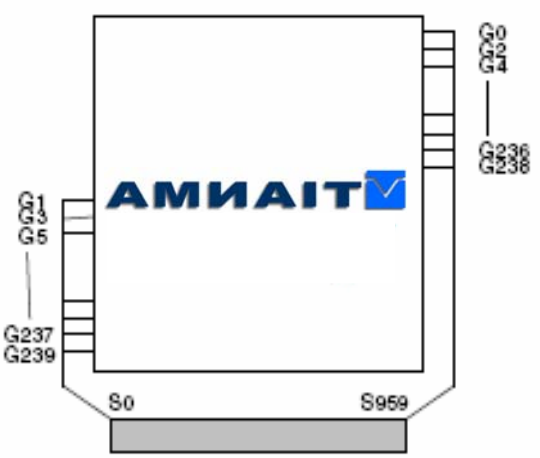
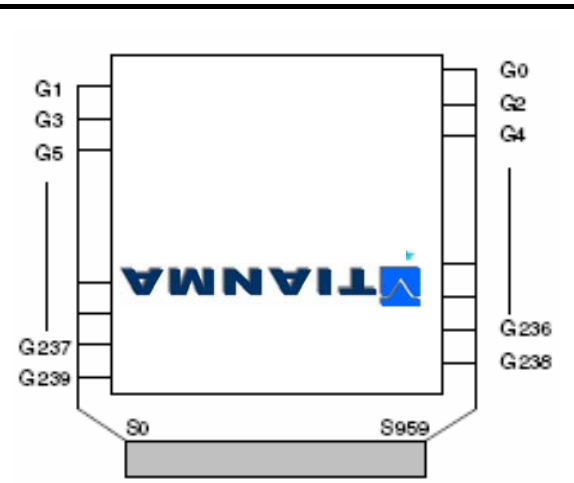
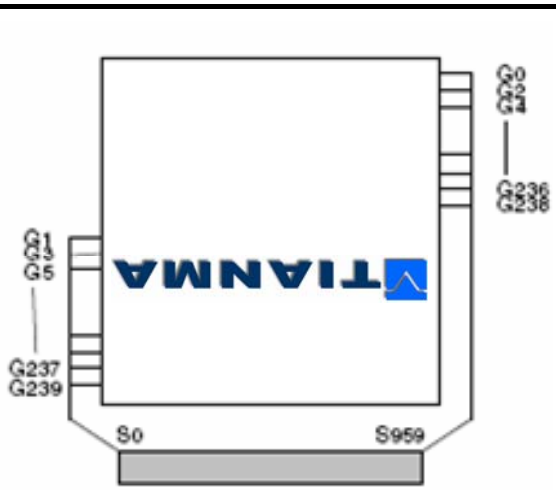
	SM=0	SM=1
UD=1 LRC=1		
UD=0 LRC=1		
UD=1 LRC=0		
UD=0 LRC=0		

Fig 9.7 Scan direction & Display

9.5. Power up/down Sequence

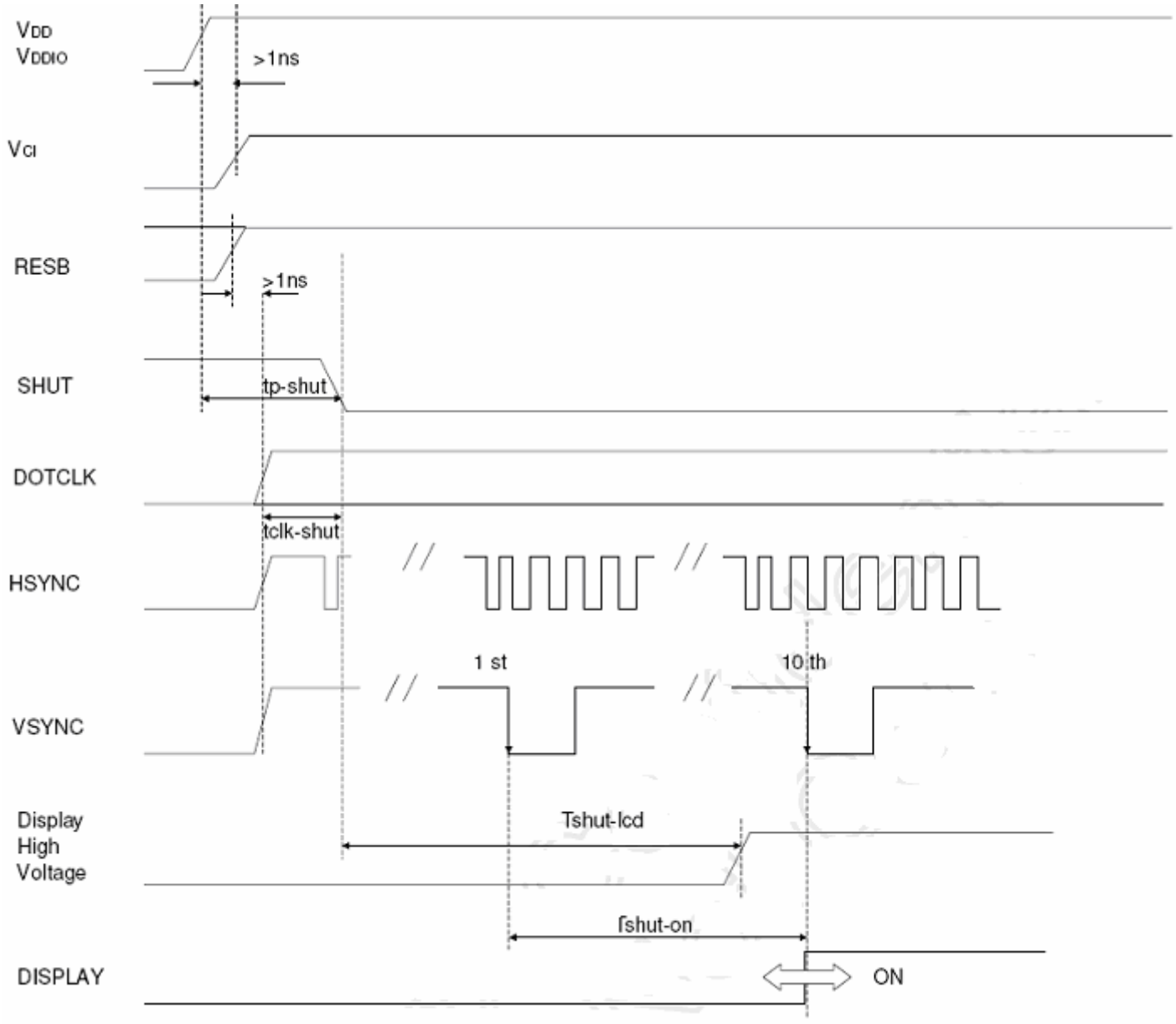


Fig 9.8 Power up sequence

Characteristics	Symbol	Min	Typ	Max	Units
VDDD / VDDIO on to falling edge of SHUT	tp-shut	1	-	-	us
DOTCLK	tclk-shut	1	-	-	clk
Falling edge of SHUT to LCD power on	tshut-lcd	-	-	128	ms
Falling edge of SHUT to display start - 1 line: 408 clk - 1 frame: 262 line -DOTCLK = 6.5MHz	tshut-on	-	-	10	frame
		-	166	-	ms

Note: It is necessary to input DOTCLK before the falling edge of SHUT.
Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

Table 9.5 Power up sequence

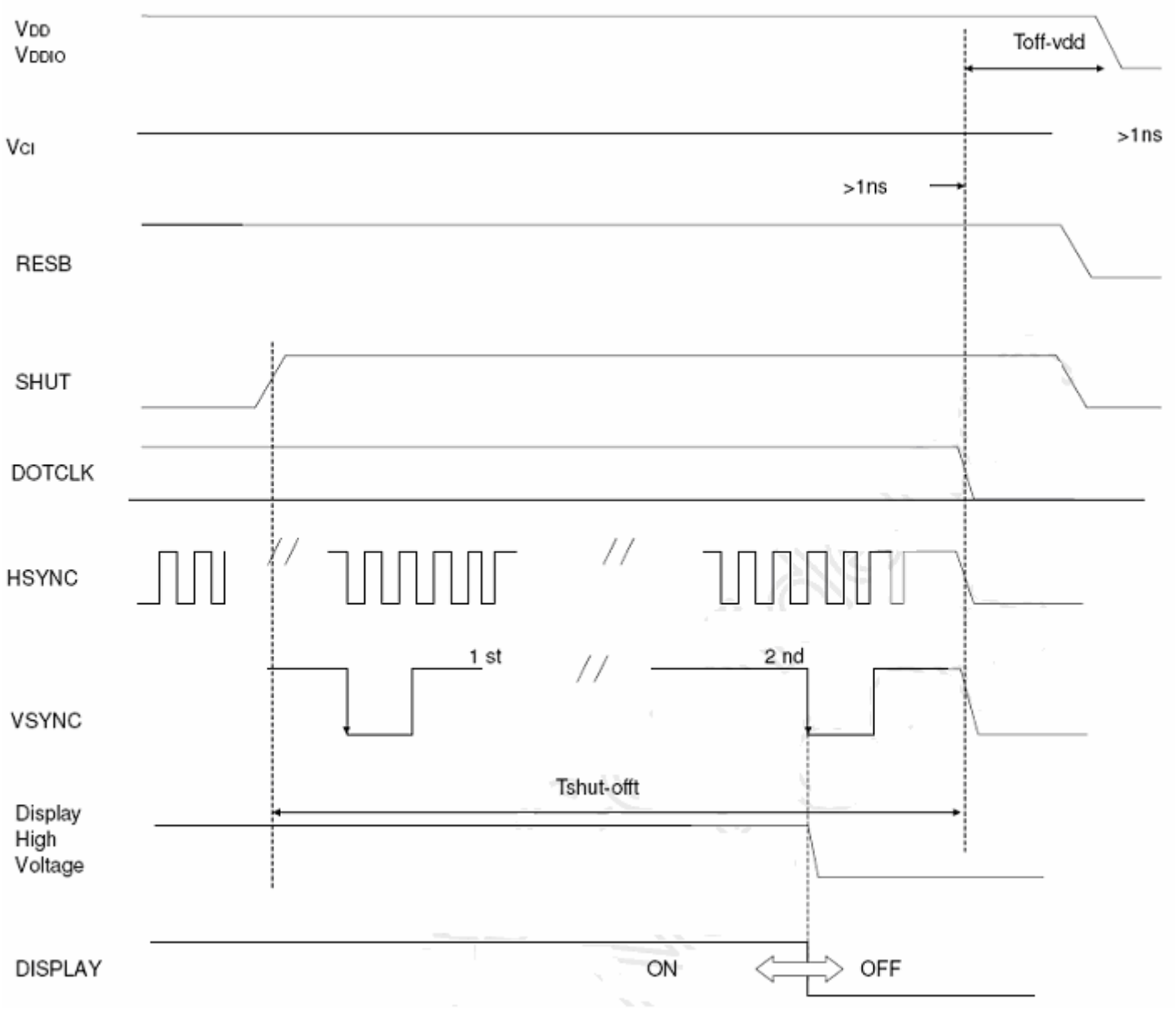


Fig 9.9 Power down sequence

Characteristics	Symbol	Min	Typ	Max	Unl
Rising edge of SHUT to display off - 1 line: 408 clk - 1 frame: 262 line - DOTCLK = 6.5MHz	tshut-off	2	-	-	frame
		33.4	-	-	ms
Input-signal-off to VDDD / VDDIO off	toff-vdd	1	-	-	us

Note: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.
Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.
If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

Table 9.6 Power down sequence

10. Optical Characteristics

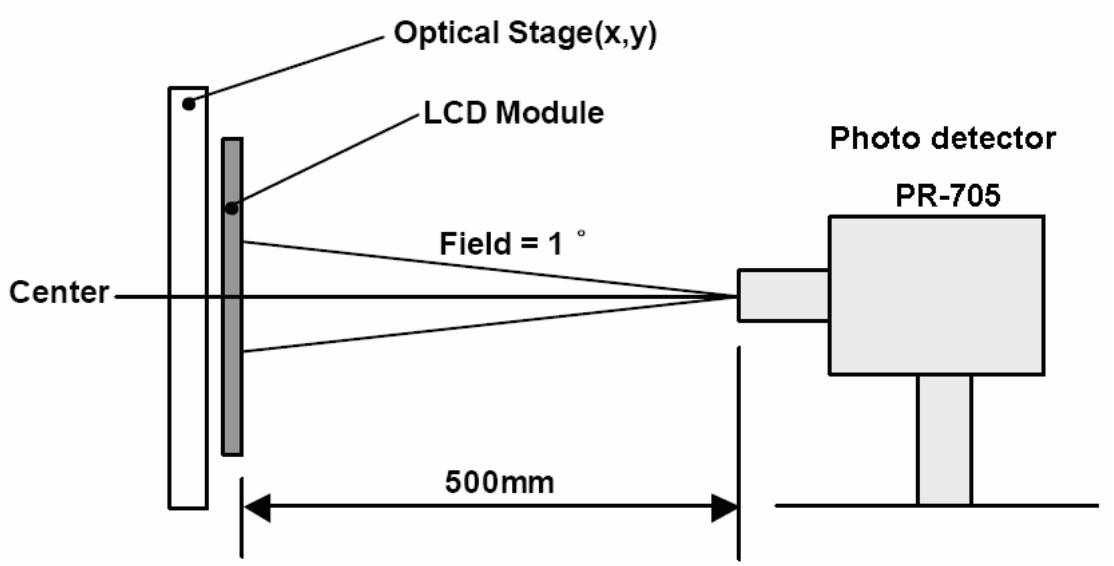
(Ta = 25 °C, I_f = 20 mA, V_L= 19.2 V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle	Horizontal	Θ_L	Center CR≥10	50	60	-	Deg.	Note 10-2
		Θ_R		50	60	-		
	Vertical	Θ_U		40	50	-		
		Θ_D		50	60	-		
Contrast Ratio		CR	At optimized View Angle	(250)	(300)	-	-	Note 10-1,3
Luminance		Y_L	Θ=0°	(200)	(250)	-	cd/m^2	Note 10-4
Uniformity		L_U		(70)	(75)	-	%	Note 10-1,5
Response Time		T_r	Θ=0°	-	(15)	(30)	ms	Note 10-6
		T_f		-	(30)	(50)	ms	
Color Chromaticity	White	X	Θ=0°	0.282	0.312	0.342	-	-
		Y		0.319	0.349	0.379		
	Red	X		0.610	0.640	0.670		
		Y		0.314	0.344	0.374		
	Green	X		0.268	0.298	0.328		
		Y		0.553	0.583	0.613		
	Blue	X		0.102	0.132	0.162		
		Y		0.107	0.137	0.167		

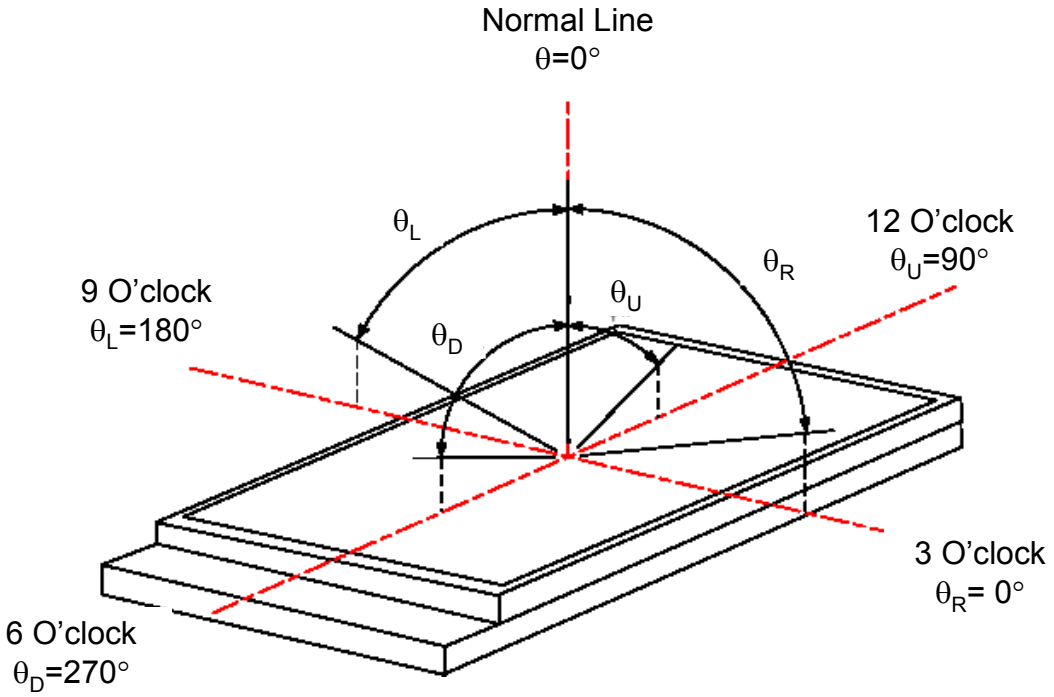
Note 10-1: Measuring equipments: DMS-501, PR-705.

Measuring condition:

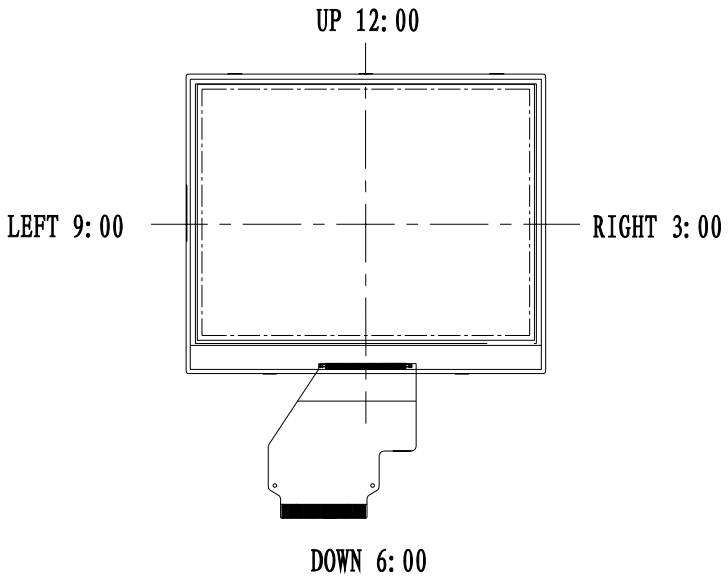
- After stabilizing and leaving the panel alone at a given temperature for 30 min, the measurement should be executed,
- Measuring surroundings: a stable, windless and dark room,
- Measuring temperature: Ta=25°C,
- 30 min after lighting the back-light.



Note 10-2: The definition of viewing angle:



Note 10-3: The definition of viewing direction:



*** The definition of viewing direction is for good image quality, which is 12 O'clock. View Direction for Largest Contrast Ratio is 6 O'clock.

Note 10-4: The contrast ratio (CR) is defined as follows:

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Measure the luminance at the center of the screen.

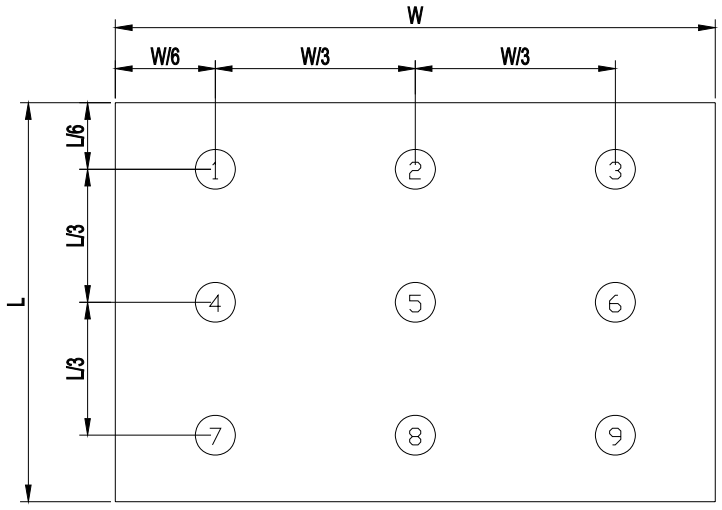
Note 10-5: Definition luminance of White: measure the luminance of White at the center of the screen.

Note 10-6: The definition of luminance uniformity:

The luminance uniformity is calculated by using following formula.

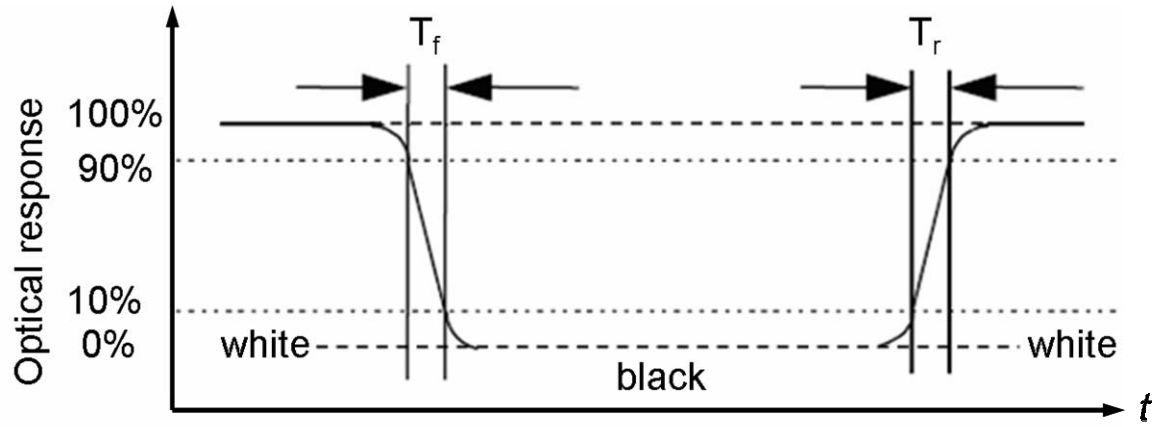
$$\text{Luminance uniformity (Lu)} = \frac{\text{Minimum luminance from ① to ⑨}}{\text{Maximum luminance from ① to ⑨}}$$

The luminance is measured at near the 9 points shown below.



Note 10-7: The definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (falling time) and from “white” to “black” (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below:



11. Reliability Test

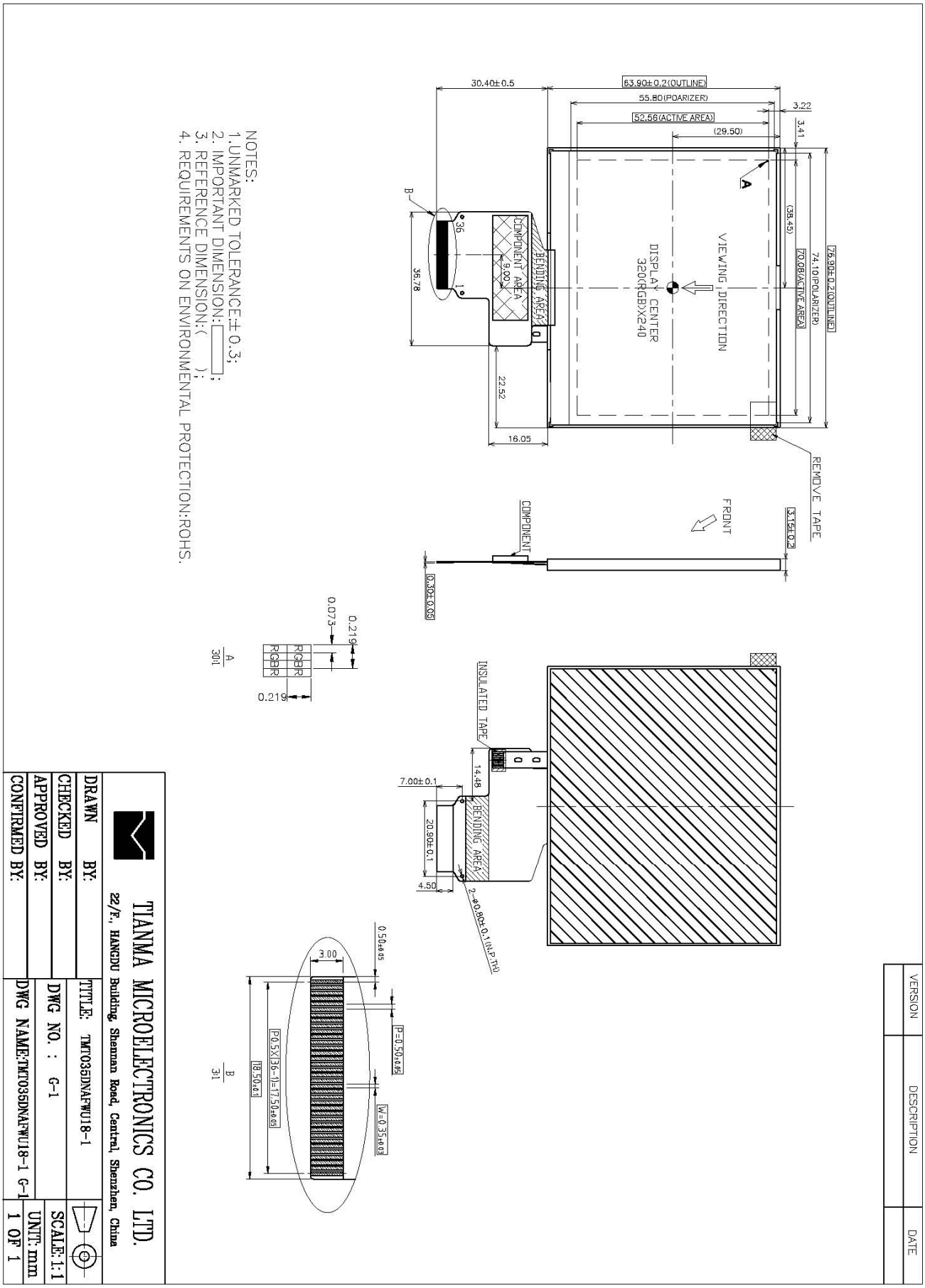
No.	Test Item	Test Condition
1	High Temperature Storage	Ta=+80 °C, 240 hrs
2	Low Temperature Storage	Ta=-30 °C, 240 hrs
3	High Temperature Operation Test	Ta=+70 °C, 240 hrs
4	Low Temperature Operation Test	Ta=-20 °C, 240 hrs
5	High Temperature &High Humidity Operation Test	Ta=+60 °C, 90% RH, 240 hrs
6	Temperature Cycle Test (Non-Operating)	-30 °C↔+25 °C↔+80 °C,100 Cycles 30min 5min 30min
7	Vibration Test (Non-Operating)	Frequency: 10 ~150 Hz, Stroke: 1.5mm Sweep time: 11 min Test Period: 6 Cycles for each direction of X,Y,Z,120 min every direction
8	Shock Test (Non-Operating)	Waveform : Half Sinusoidal Wave Shock Level:30 G, Pulse Width:18 ms, Direction: ±X, ±Y, ±Z, Cycle:3 times
9	Electrical Static Discharge HBM (Operating)	Air : ± 8 kV, 150 pF/ 330 Ω (10 times/point)

Note: 1. Ta=Ambient Temperature.

2. The tested samples have recovery time for 2hrs at room temperature before estimating these appearance and display effect.

3. Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

12. Mechanical Drawing



13. Package

TBD

14. Precautions for Use of LCD Modules

14.1. Handling Precautions

14.1.1. The display panel is made of glass. **Do not** subject it to a mechanical shock by dropping it from a high place, etc.

14.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

14.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

14.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

14.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol
— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, **do not** use the following:

— Water
— Ketone
— Aromatic solvents

14.1.6. Do not attempt to disassemble the LCD Module.

14.1.7. If the logic circuit power is off, **do not** apply the input signals.

14.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, **do not** conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

14.2. Storage precautions

14.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

14.2.2. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃
Relatively humidity: ≤80%

14.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

14.3. Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.