

承 认 书

SPECIFICATION FOR APPROVAL

(一) 顾 客:

CUSTOMER: _____

(二) 品 名:

DESCRIPTION: _____

(三) 型 号:

PART NO: 模组 V035QN02-A06

新玻璃 A035QN02 V6(601)

(四) 日 期:

DATE: _____

承认签名

APPROVED SIGNATURES

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A. General Description

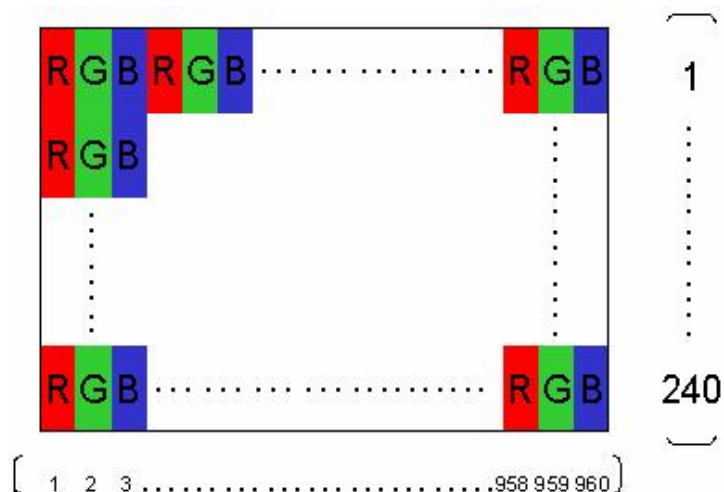
A035QN01 V6 is an amorphous transmissive type Thin Film Transistor Liquid crystal Display (TFT-LCD). This model is composed of a TFT-LCD, drive and gate IC's, an FPC (flexible printed circuit) and a backlight unit.

B. Features

- QVGA resolution in RGB stripe dot arrangement
- High brightness
- 3-wire register setting
- Interfaces: parallel RGB 24-bit
- 2-in-1 FPC for LCD signals and backlight LED power
- Wide viewing angle
- Green design

C. Physical specifications

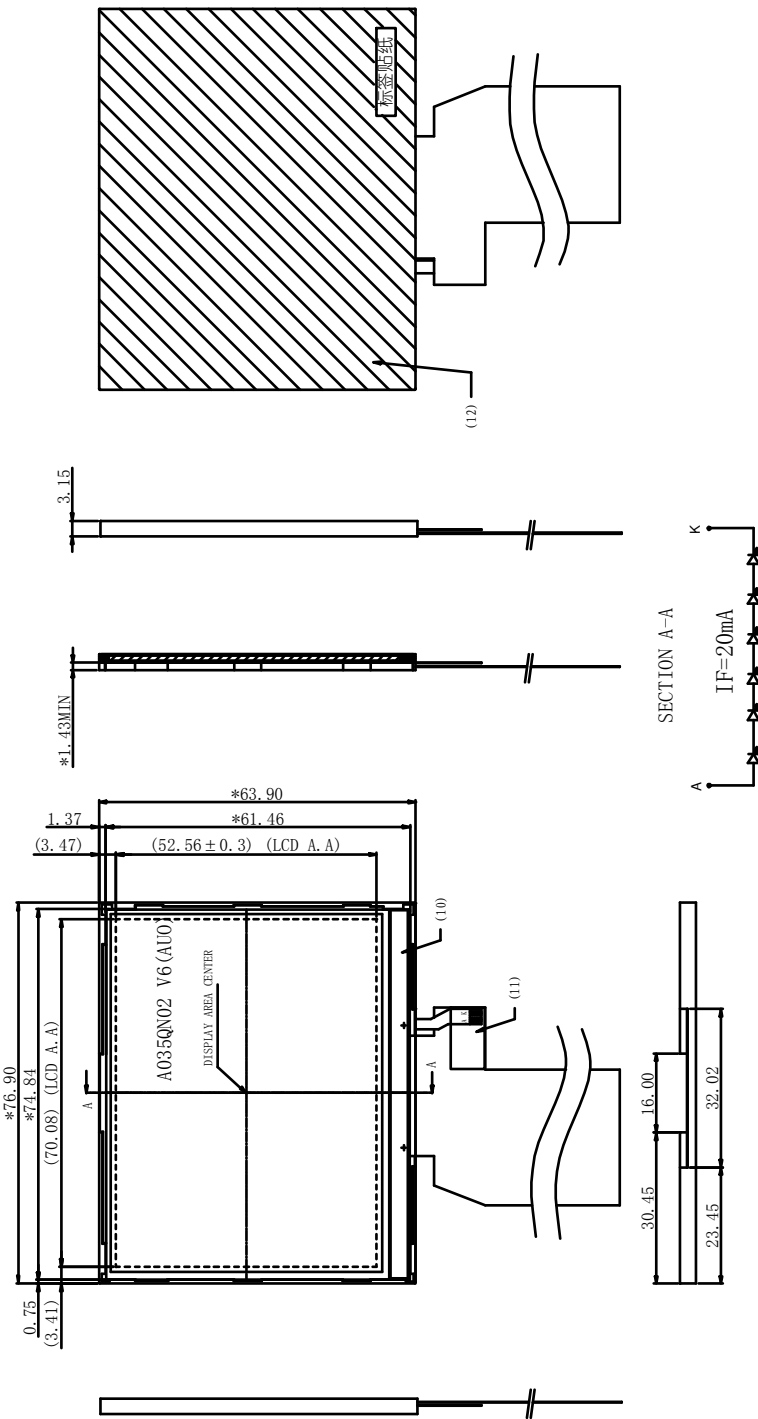
NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	320 RGB (H)×240(V)	
2	Active Area	mm	70.08(H)×52.56(V)	
3	Screen Size	inch	3.5(Diagonal)	
4	Dot Pitch	mm	0.073(H)×0.219(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	Note 2
7	Overall Dimension	mm	76.9(H) × 63.9(V) × 3.15(T)	Note 3
8	Weight	g	33.2	
9	Panel surface treatment	--	Hard coating 3H	
10	Display Mode	--	Normally White	



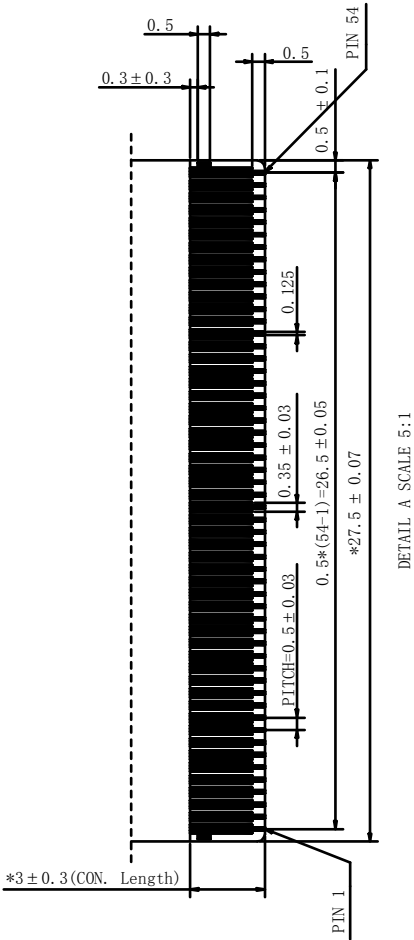
Note 2: The full color display depends on 8-bit data signal (pin12~35). Note 3:

Not include FPC. Refer to the next page for further information.

D. Outline Dimension



- NOTE:
1. Unit:mm
 2. General tolerance ± 0.2
 3. The bending radius of FPC should be larger than 0.6mm
 4. Luminous intensity (9 points average): 320cd/m^2 (min)
 5. * The thickness of solder area



E. Electrical Specifications

1 Pin Assignment

NO.	Pin name	I/O	Description	Remarks
1	LED_Cathode	I	Backlight LED Cathode	
2	LED_Cathode	I	Backlight LED Cathode	
3	LED_Anode	I	Backlight LED Anode	
4	LED_Anode	I	Backlight LED Anode	
5	NC	--	Not Connected	
6	NC	--	Not Connected	
7	NC	--	NC	
8	RESET	--	Reset	
9	SPENA	I	SPI Interface Data Enable Signal	
10	SPCLK	I	SPI Interface Clock	
11	SPDAT	I	SPI Interface Data	
12	NC	--	Not Connected	
13	NC	--	Not Connected	
14	B0	I	Blue Data Bit 0	
15	B1	I	Blue Data Bit 1	
16	B2	I	Blue Data Bit 2	
17	B3	I	Blue Data Bit 3	
18	B4	I	Blue Data Bit 4	
19	B5	I	Blue Data Bit 5	
20	NC	--	Not Connected	
21	NC	--	Not Connected	
22	G0	I	Greene Data Bit 0	
23	G1	I	Greene Data Bit 1	
24	G2	I	Greene Data Bit 2	
25	G3	I	Greene Data Bit 3	
26	G4	I	Greene Data Bit 4	
27	G5	I	Greene Data Bit 5	
28	NC	--	Not Connected	
29	NC	--	Not Connected	
30	R0	I	Red Data Bit 0	
31	R1	I	Red Data Bit 1	
32	R2	I	Red Data Bit 2	
33	R3	I	Red Data Bit 3	
34	R4	I	Red Data Bit 4	

35	R5	I	Red Data Bit 5	
36	HSYNC	I	Horizontal Sync Input	
37	VSYNC	I	Vertical Sync Input	
38	DCLK	I	Dot Data Clock	
39	NC	--	NC	
40	NC	--	NC	
41	VDD	I	Digital Power	
42	VDD	I	Digital Power	
43	NC	I	Not Connected	
44	NC	--	Not Connected	
45	NC	--	Not Connected	
46	NC	--	Not Connected	
47	NC	--	Not Connected	
48	NC	--	Not Connected	
49	NC	--	Not Connected	
50	NC	--	Not Connected	
51	NC	--	Not Connected	
52	ENB	I	Data Enable Input	VDD/GND
53	GND	I	Ground	
54	GND	I	Ground	

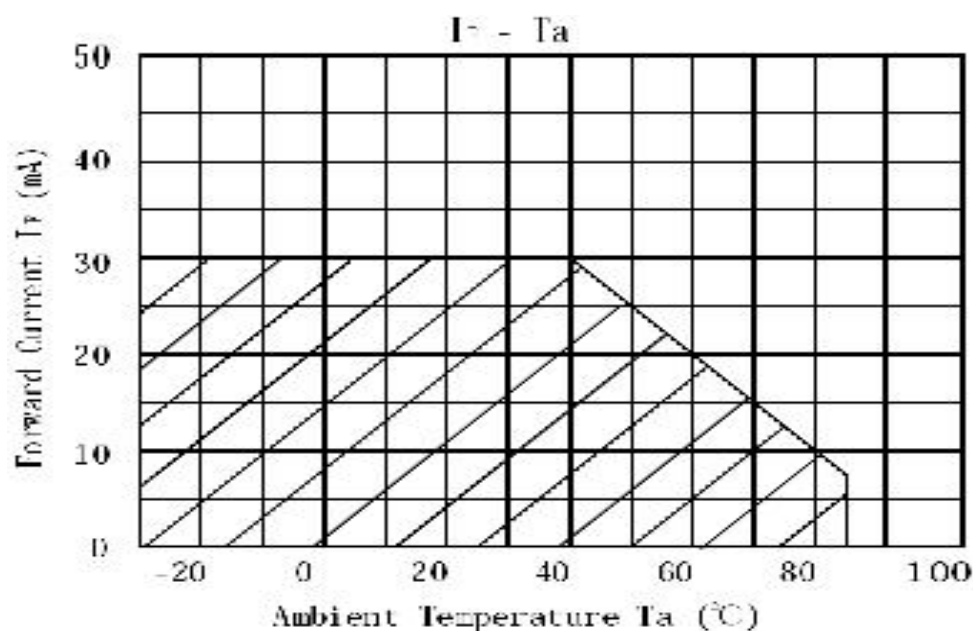
I: Input pin; O: Output pin

Note 1. For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported. If ENB signal is fixed low, SYNC mode is used. Otherwise, DE+SYNC mode is used.

Note 2. SPENA、SPCLK are usually pulled high.

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Typ.		
Power Voltage	AVDD	-0.3	7.0	V	AVSS=0
	VDD	-0.3	7.0	V	GND=0
	VGH	-0.3	32.0	V	GND=0
	VGL	-22.0	+0.3	V	GND=0
	VGH-VGL	-0.3	+45	V	GND=0
Input Signal Voltage	Vi	-0.3	AVDD+0.3	V	
	Vl	-0.3	VDD+0.3	V	
Storage Temperature	Tst	-10	70	°C	Note 2
Operating Temperature(Ta)	Top	-0	60	°C	Note 2, Note 3



- Note 1. If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.
- Note 2. Temp. ≤ 60°C. 90% RH MAX
Temp. > 60°C, Absolute humidity shall be less than 90% RH at 60°C
- Note 3. The LCD module operating temperature, excluding touch panel, is from -10 to 70°C
- Note 4. If LED current exceeds the limit curve, the lifetime will drop dramatically

3. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

a. TFT- LCD Panel (GND=0V)

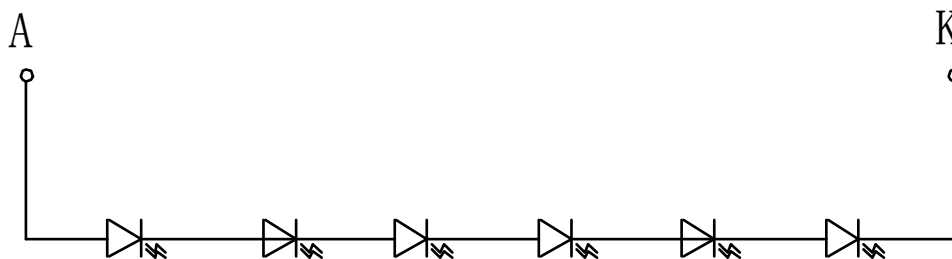
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Digital Power Supply	VDD	3	3.3	3.6	V	
Gate On Voltage	VGH	14	16	18	V	
Gate Off Voltage	V _{GL}	-11	-10	-8	V	
Frame Frequency	f _{Frame}	55	60	70	Hz	
Dot Data Clock	DCLK	-	6.4	-	MHz	

Note 1. Panel surface temperature should be kept less than content of section 3.2. "Absolute maximum ratings"

b. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ	Max.	Unit	Remark
LED Current	I _L	--	20	28	mA	single serial
LED Voltage	V _L	--	19.2	20.4	V	single serial
LED Life Time	LL	10,000	--	--	Hr	Note 2, 3

Note 1: LED backlight is six LEDs serial type.



Note 2: The "LED Supply Voltage" is defined by the number of LED at Ta=25°C, If=20mA. In the case of 6 pcs LED, V_{LED}=3.2*6=19.2V

Note 3: The "LED life time" is defined as the time for the module brightness to decrease to 50% of the initial value at Ta=25°C, If=20mA

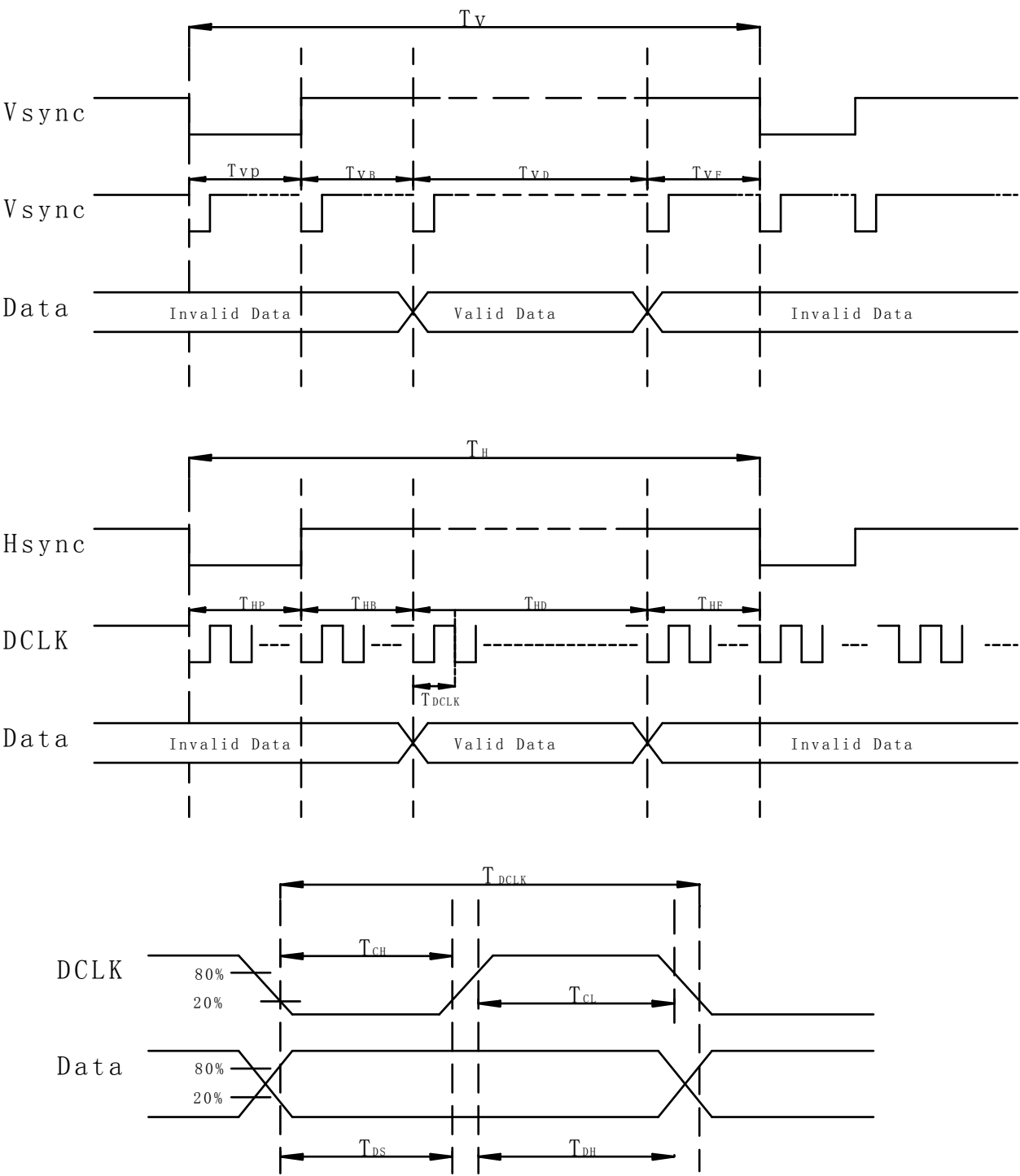
Note 4: The LED lifetime could be decreased if operating I_L is larger than 25mA.

4. AC Timing

a. Timing Condition

Signal	Item		Symbol	Min	Typ	Max	Unit
DCLK	Frequency		Dclk	6	6.4		MHz
	High Time		Tch		78	80	ns
	Low Time		Tcl		78	80	ns
Data	Setup Time		Tds	12			ns
	Hold Time		Tdh	12			ns
HSYNC	Period		TH		408	432	DCLK
	Pulse Width		Thp	5	30		DCLK
	Back-Porch		Thb		38		DCLK
	Display Period		Thd		320		DCLK
	Front-Porch		Thf		20		DCLK
VSYNC	Period	NTSC	Tv		262.5		TH
		PAL			312.5		
	Pulse Width		Tvp	1	3	5	TH
	Back-Porch	NTSC	Tvb		15		TH
		PAL			26		
	Display Period		Tvd		240		TH
	Front-Porch	NTSC	Tvf		4.5		TH
		PAL			46.5		
	VSYNC-ENB Time		NTSC	TVSE		18	
PAL			TVSE		26		TH
HSYNC-ENB Time			THE		68		DCLK
ENB Pulse Width			TEP		320		DCLK

b. Timing Diagram



5. Command register map

a. Command timing : Serial Peripheral Interface

PARAMETER	Symbol	Min	Typ	Max	Unit
SPCK period	T_{CK}	60	—	—	ns
SPCK high width	T_{CKH}	30	—	—	ns
SPCK low width	T_{CKL}	30	—	—	ns
Data setup time	T_{SU1}	12	—	—	ns
Data hold time	T_{HD1}	12	—	—	ns
SPENA to SPCK setup time	T_{CS}	20	—	—	ns
SPENA to SPDA hold time	T_{CE}	20	—	—	ns
SPENA high pulse time	T_{CD}	50	—	—	ns

b. COMMAND TABLE

Command Table and POR (Power On Reset) values

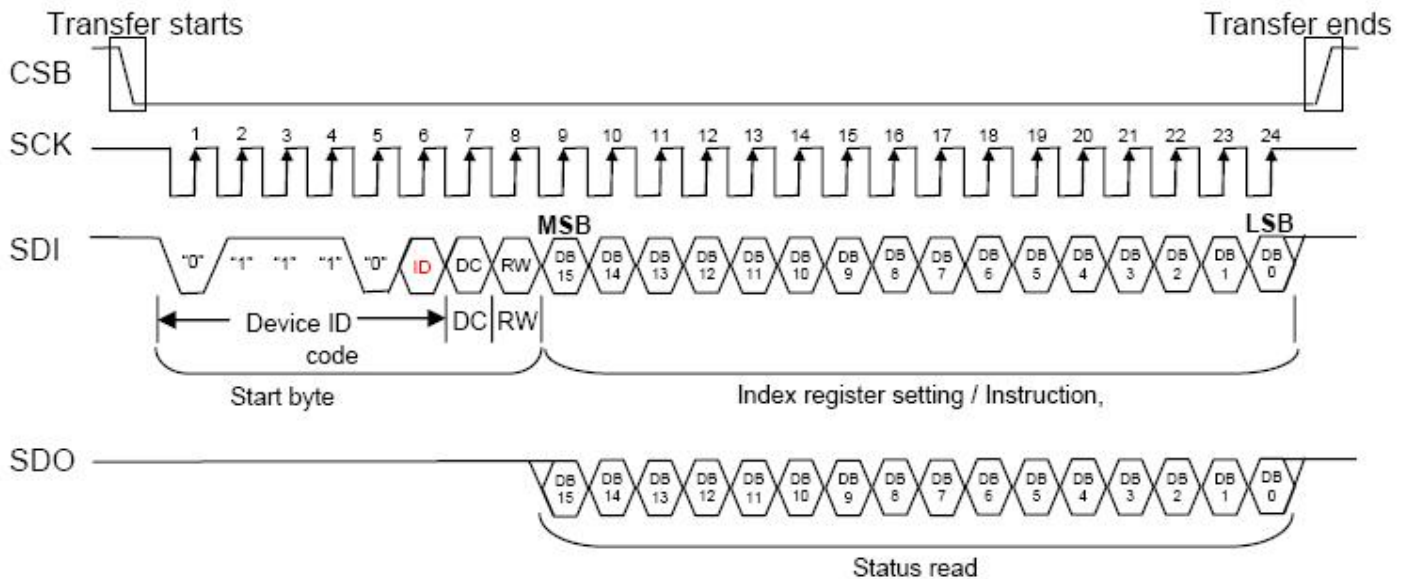
Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R01h	Driver output control [00XX][X0XX]EF	0	1	0	0	REV	CAD	BGR	SM	TB	RL	1	1	1	0	1	1	1	1
R02h	LCD drive AC control (0300h)	0	1	0	0	0	0	0	0	B/C	EOR	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0
R03h	Power control (1) (7272h)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
R0Bh	Frame cycle control (DC00h)	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	0	0	0	0	0	0	0	0	0	0
R0Ch	Power control (2) (0002h)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
R0Dh	Power control (3) (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4) (3200h)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	VCOMAS
R0Fh	Gate scan starting Position (0000h)	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R16h	Horizontal Porch (9F86h)	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
R17h	Vertical Porch (0002h)	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R1Eh	Power control (5) (002Dh)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCMS5	VCMS4	VCMS3	VCMS2	VCMS1	VCMS0
R30h	γ control (1) (0000h)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	γ control (1) (0200h)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20

R31h	γ control (1)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
	(0200h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R32h	γ control (1)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R33h	γ control (1)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R34h	γ control (1)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
	(0405h)			0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R35h	γ control (1)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
	(0202h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
R36h	γ control (1)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
	(0707h)			0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R37h	γ control (1)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
	(0006h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R3Ah	γ control (2)	0	1	0	0	0		VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R3Bh	γ control (2)	0	1	0	0	0		VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R40h	γ control (3)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R41h	γ control (3)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
	(0200h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R42h	γ control (3)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R43h	γ control (3)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R44h	γ control (3)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
	(0405h)			0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R45h	γ control (3)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
	(0202h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
R46h	γ control (3)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
	(0707h)			0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R47h	γ control (3)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
	(0006h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R4Ah	γ control (4)	0	1	0	0	0		VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R4Bh	γ control (4)	0	1	0	0	0		VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R50h	γ control (5)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51h	γ control (5)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
	(0200h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R52h	γ control (5)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R53h	γ control (5)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R54h	γ control (5)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
	(0405h)			0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R55h	γ control (5)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
	(0202h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

R56h	γ control (5)	0	1	0	0	0	0	0	PRN 52	PRN 51	PRN 50	0	0	0	0	0	PRN 42	PRN 41	PRN 40
	(0707h)			0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R57h	γ control (5)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
	(0006h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R5Ah	γ control (6)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R5Bh	γ control (6)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R27h	VCOM bias current	0	1	0	0	0	0	0	0	0	0	0	1	IU2	IU1	IU0	0	0	0
	(0058h)			0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0
R28h	VCOM OTP	0	1	0	0	0	0	0	0	0	0	0	0	0	0	CCB3	CCB2	CCB1	CCB0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R2Ch	VCOM Charge sharing	0	1	1	1	VCOM SH	0	1	0	0	0	1	0	0	0	1	1	0	0
	(E88Ch)			1	1	1	0	1	0	0	0	1	0	0	0	1	1	0	0
R2Dh	Software Shut	0	1	0	1	1	1	1	1	1	1	0	1	0	0	0	SS1	SS0	0
	(7F40)			0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
R2Eh	3 Gamma	0	1	1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	OLO
	(B945h)			1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	1

c. Serial Interface – 3-wires (24 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCK), serial input data (SDI), and serial output data (SDO). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB. DC bit determinate the data of SDI which is register or data. RW bit determinate the read / write operation.



d.Recommand Register Settings

Register	Setting
R01	"2AEF"h
R03	"920E"h
R0C	"0005"h
R0D	"000C"h
R0E	"3100"h
R10	"00DC"h
R12	"0070"h
R1E	"00A4"h
R30	"0304"h
R31	"0507"h
R32	"0405"h
R33	"0007"h
R34	"0507"h
R35	"0004"h
R36	"0605"h
R37	"0103"h
R3A	"000F"h
R3B	"000F"h

F. Optical specifications (Note 1, 2)

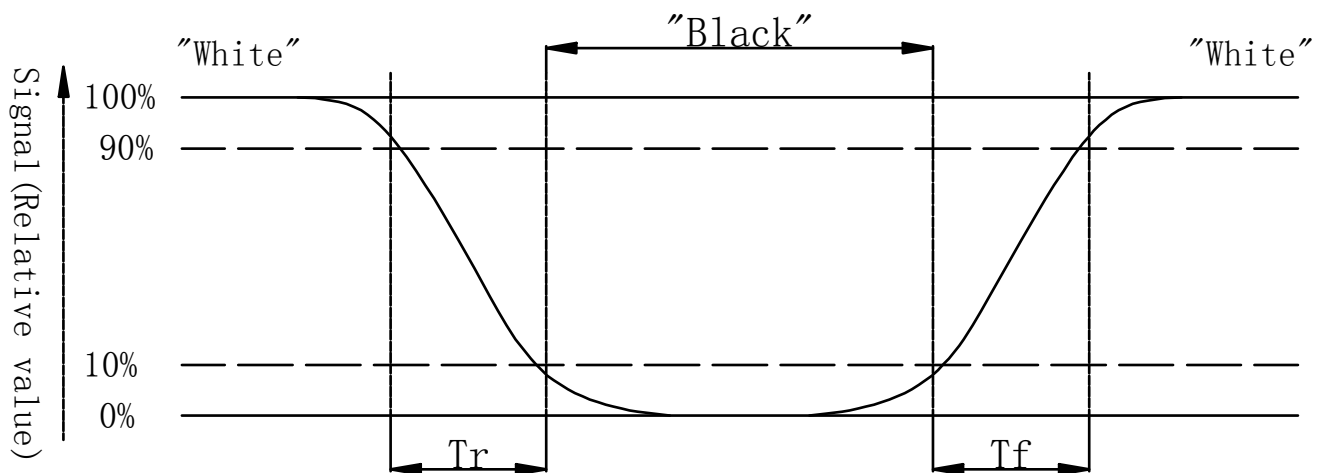
Item	Symbol	Condition	Min	Typ	Max	Uni	Remark
Response Time							
Rise	Tr	$\theta=0^\circ$	–	10	20	ms	Note 3, 4
Fall	Tf		–	15	25	ms	
Contrast ratio	CR	At optimized viewing angle	150	200	–		Note 5, 6
Viewing Angle							
Top		$CR \geq 10$	35	50	–	deg.	Note 7, 8
Bottom			40	55	–		
Left			45	60	–		
Right			45	60	–		
Brightness	Y_L	$\theta=0^\circ$	320		–	Cd/m ²	
White Chromaticity	x	$\theta=0^\circ$	0.26	0.31	0.36		
	y	$\theta=0^\circ$	0.28	0.33	0.38		

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25 C, and backlight current $I_L=20$ mA

Note 2: To be measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-7, after 10 minutes operation

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.



Note 4. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25°C

Note 5. Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White $V_i = V_{i50} + 1.5V$ Black

$V_i = V_{i50} \pm 2.0V$

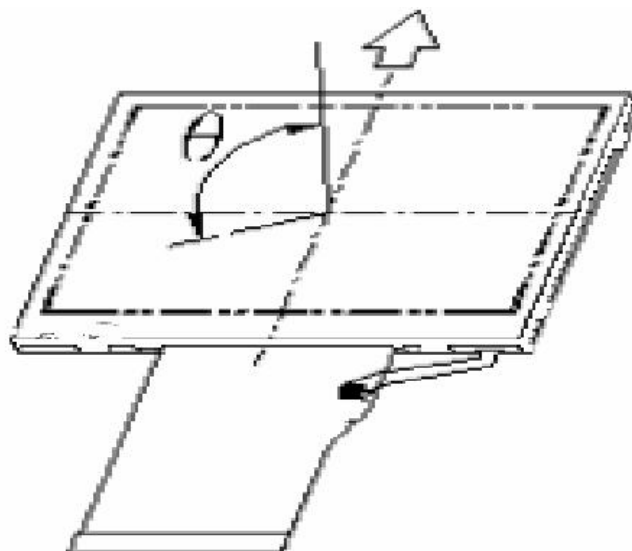
“ $\pm$ ” means that the analog input signal swings in phase with COM signal.

“ ” means that the analog input signal swings out of phase with COM signal.

V_{i50} :The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened

Note 7. Definition of viewing angle: refer to figure as below



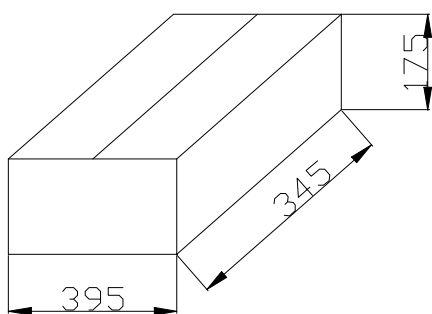
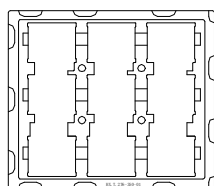
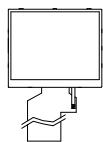
Note 8. The viewing angles are measured at the center area of the panel when all the input terminals of LC panel are electrically opened.

G. Reliability Test Items

No.	Test items	Conditions		Remark
1	High Temperature Storage	Ta= 70℃	96Hrs	
2	Low Temperature Storage	Ta= 10℃	96Hrs	
3	High Temperature Operation	Ta= 60℃	96Hrs	
4	Low Temperature Operation	Ta= 0℃	96Hrs	
5	High Temperature & High Humidity	Ta= 60℃. 80% RH	96Hrs	Operation
6	Heat Shock	-20℃~60℃, 50 cycle, 2Hrs/cycle		Non-operation
7	Electrostatic Discharge	±200V, 200pF(0Ω), once for each terminal		Non-operation
8	Vibration (With Carton)	X、Y、Z each orientation 10~~50Hz, 2G, 1h		
9	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		

Note : Ta: Ambient temperature

H. Packing Form



一个产品

一个包装盘

包装盘尺寸: 290*340*14mm

即一个包装盘产品: 9 pcs

一个小箱装16PCS包装盘

(其中最上面一个包装盘不装产品)

即一小箱装产品: $15 \times 9 = 135$ pcs

一个小箱的尺寸: 345*395*175mm

I. Application Note

1. Power on/off sequence

The LCD panel adopts high voltage driver ICs, so it could be permanently damaged if a wrong power on/off sequence is used. When powering on the LCD, VDD should go up firstly, and then turn on VGL and AVDD, and finally VGH. Turn off the LCD panel with reversed order or shut off all the power supplies simultaneously

