May 1990

Operational Transconductance Amplifiers (OTA's)

Gatable-Gain Blocks

Features:

- *Slew rate (unity gain, compensated): 50 V/μs*
- *Adjustable power consumption: 10μW to 30 mW*
- *Flexible supply voltage range: ±2 V to ±15 V*
- *Fully adjustable gain: 0 to $g_m R_L$ limit*
- *Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)*
- *Extended g_m linearity: 3 decades*

Applications:

- *Sample and hold*
- *Multiplex*
- *Voltage follower*
- *Multiplier*
- *Comparator*

The CA3080 and CA3080A types are Gatable-Gain Blocks which utilize the unique operational-transconductance-amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A types are notable for their excellent slew rate (50 V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (-55 to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

These types are supplied in the 8-lead Small Outline package (CA3080M, CA3080AM), the 8-lead TO-5-style package (CA3080, CA3080A), and in the 8-lead TO-5-style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080 is also supplied in the 8-lead dual-in-line plastic ("MINI-DIP") package (CA3080E, CA3080AE), and in chip form (CA3080H).

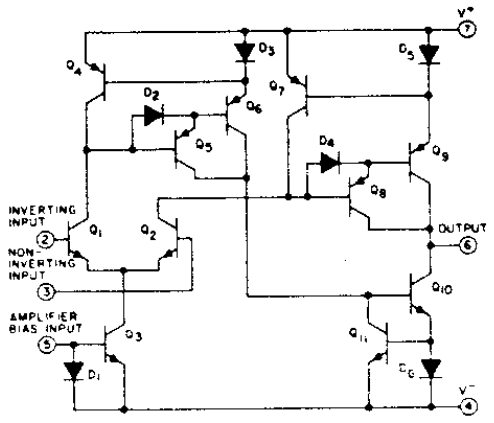


Figure 1- Schematic diagram for CA3080 and CA3080.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS $V^+ = 15\ V, V^- = -15\ V$, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	CA3080, CA3080E, CA3080S LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}		–	0.4	5	mV
		$T_A = 0$ to 70^oC	–	–	6	
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = 0$ to 70^oC	–	–	7	
Forward Transconductance (large signal)	g_m		6700	9600	13000	μmho
		$T_A = 0$ to 70^oC	5400	–	–	
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	350	500	650	μA
		$R_L = 0$, $T_A = 0$ to 70^oC	300	–	–	
Peak Output Voltage: Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	V
Peak Output Voltage: Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	μV/V
Input Offset Voltage Sensitivity: Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CA3080, CA3080E, CA3080S

Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	0.3	mV
Input Offset Voltage Change	$\lvert \Delta V_{IO} \rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	0.2	mV
Peak Output Current	I_{OM}	$I_{ABC} = 5\ \mu A$	5	μA
Peak Output Voltage: Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$	13.8	V
Peak Output Voltage: Negative	V^-_{OM}		−14.5	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	0.08	nA
		$I_{ABC} = 0$, $V_{TP} = 36\ V$	0.3	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4\ V$	0.008	nA
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate: Maximum (uncompensated)	SR		75	V/μs
Slew Rate: Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}		2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	C_{I-O}	f = 1 MHz	0.024	pF
Propagation Delay	t_{PHL}, t_{PLH}	$I_{ABC} = 500\ \mu A$	45	ns

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS: V^+ = 15 V, V^- = −15 V, I_{ABC} = 500 μA, T_A = 25°C (unless indicated otherwise)	CA3080A, CA3080AE, CA3080AS LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage	V_{IO}	I_{ABC} = 5 μA	–	0.3	2	mV
			–	0.4	2	
		T_A = −55 to +125°C	–	–	5	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	I_{ABC} = 500 μA to I_{ABC} = 5 μA	–	0.1	3	mV
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		T_A = −55 to + 125°C	–	–	8	
Forward Transconductance (large signal)	g_m		7700	9600	12000	μmho
		T_A = −55 to + 125°C	4000	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$	I_{ABC} = 5 μA, R_L = 0	3	5	7	μA
		R_L = 0	350	500	650	
		R_L = 0, T_A = −55 to +125°C	300	–	–	
Peak Output Voltage:						V
Positive	V^+_{OM}	I_{ABC} = 5 μA, R_L = ∞	12	13.8	–	
Negative	V^-_{OM}		−12	−14.5	–	
Positive	V^+_{OM}	R_L = ∞	12	13.5	–	
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						μV/V
Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	
Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Magnitude of Leakage Current		I_{ABC} = 0, V_{TP} = 0	–	0.08	5	nA
		I_{ABC} = 0, V_{TP} = 36 V	–	0.3	5	
Differential Input Current		I_{ABC} = 0, V_{DIFF} = 4 V	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

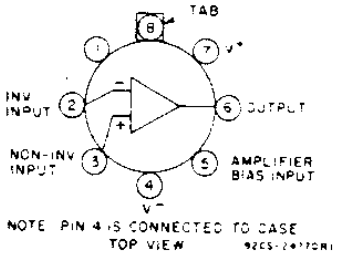
ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080A, CA3080AE, CA3080AS	
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				V/μs
Maximum (uncompensated)	SR		75	
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}	–	2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	I_{ABC} = 100 μA, T_A = −55 to +125°C	3	μV/°C
Propagation Delay	t_{PHL}, t_{PLH}	I_{ABC}=500 μA	45	ns

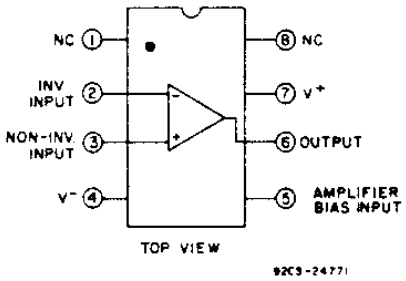
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- terminals)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE	V^+ to V^-
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA3080, CA3080E, CA3080S	0 to + 70 °C
CA3080A, CA3080AE, CA3080AS	−55 to + 125 °C
Storage	−65 to + 150 °C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 265 °C

* Short circuit may be applied to ground or to either supply.



TO-5 Style Package



Plastic Package (E Suffix)

Fig.2 – Functional diagrams.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

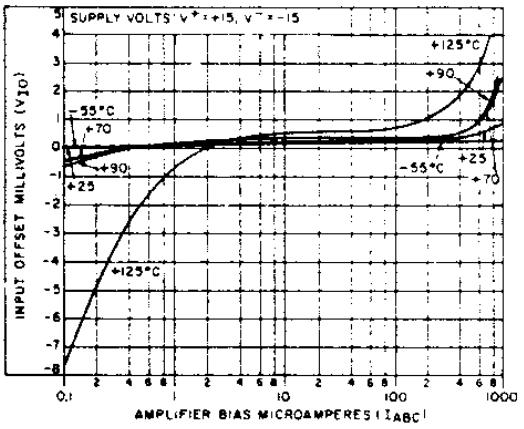


Fig.3 – Input offset voltage as a function of amplifier bias current.

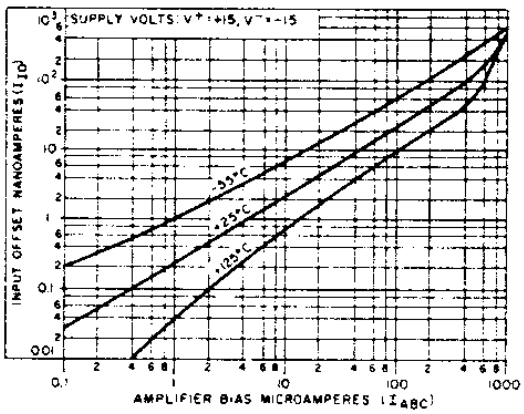


Fig.4 – Input offset current as a function of amplifier bias current.

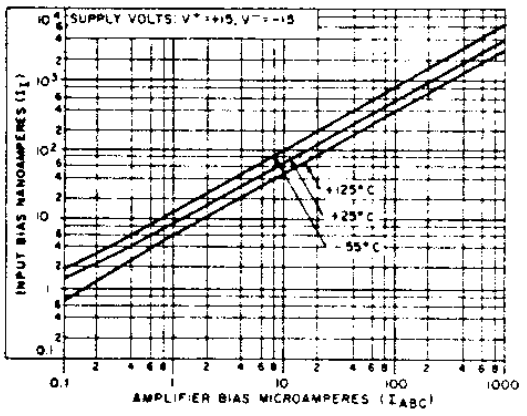


Fig.5 – Input bias current as a function of amplifier bias current.

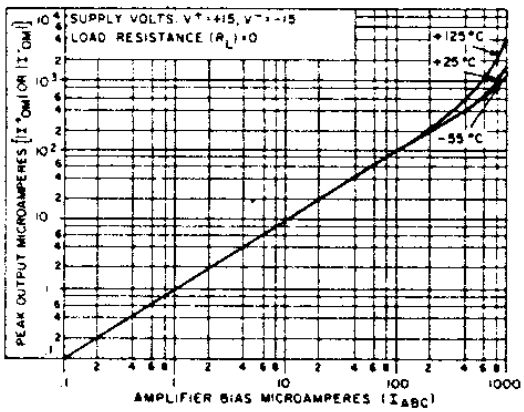


Fig.6 – Peak output current as a function of amplifier bias current.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

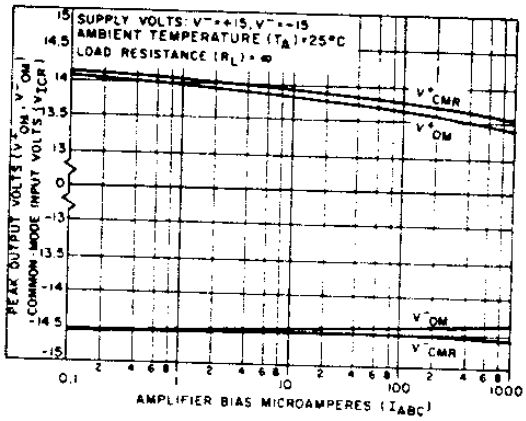


Fig.7 – Peak output voltage as a function of amplifier bias current.

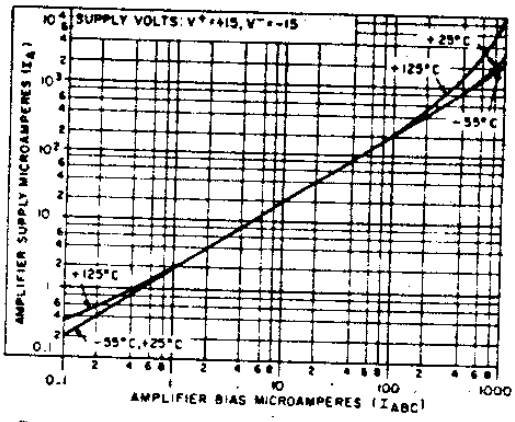


Fig.8 – Amplifier supply current as a function of amplifier bias current.

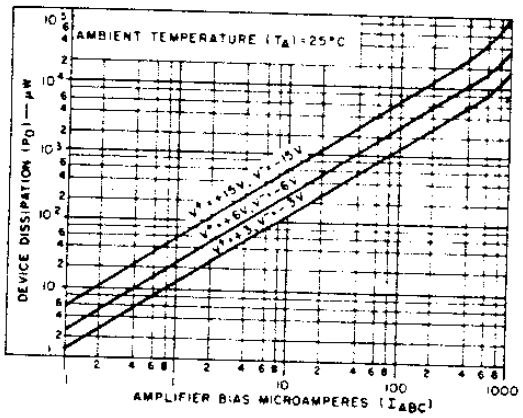


Fig.9 – Total power dissipation as a function of amplifier bias current.

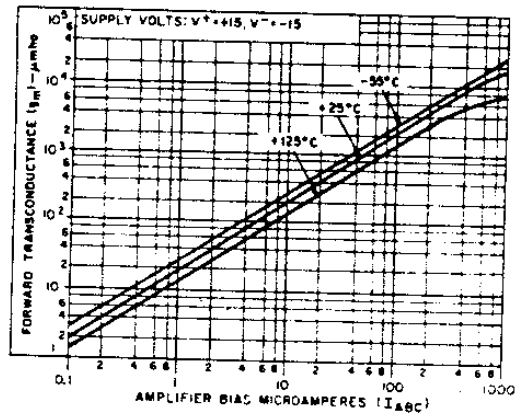


Fig.10 – Transconductance as a function of amplifier bias current.

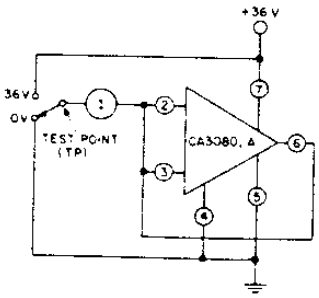


Fig.11 – Leakage current test circuit.

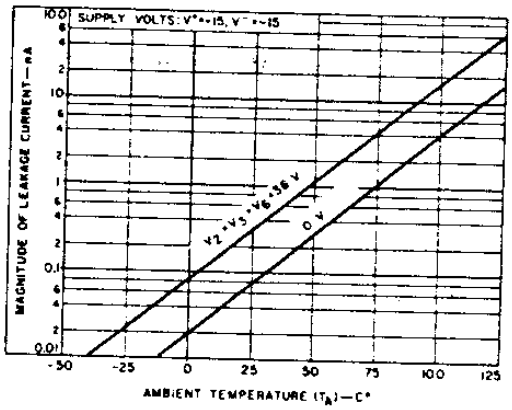


Fig.12 – Leakage current as a function of temperature.

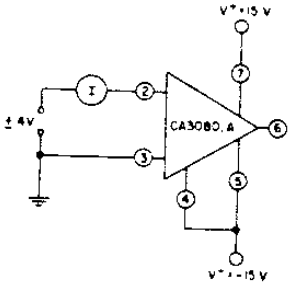


Fig.13 – Differential input current test circuit.

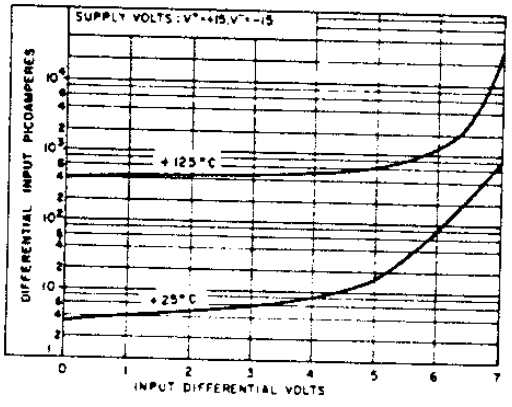


Fig.14 – Input current as a function of input differential voltage.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

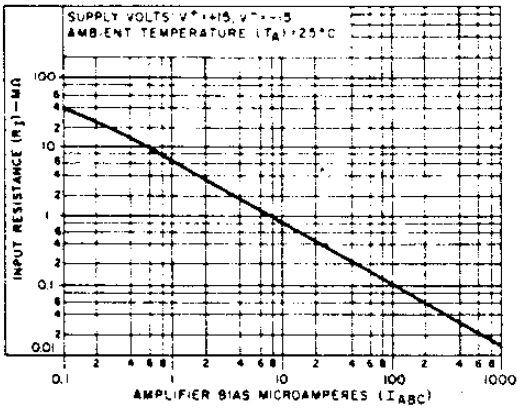


Fig. 15 — Input resistance as a function of amplifier bias current.

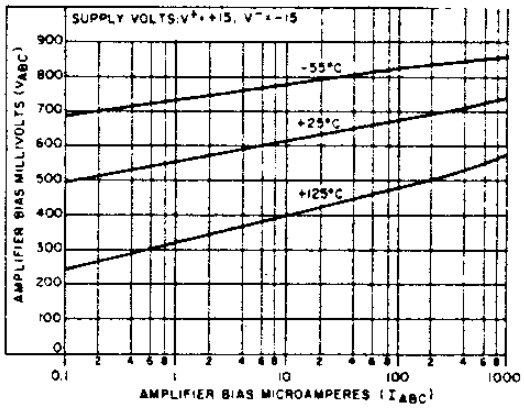


Fig. 16 — Amplifier bias voltage as a function of amplifier bias current.

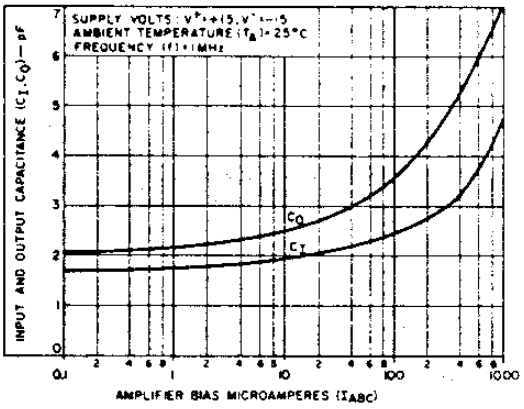


Fig. 17 — Input and output capacitance as a function of amplifier bias current.

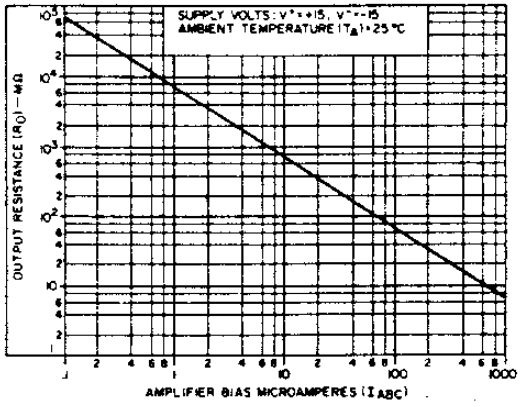


Fig. 18 — Output resistance as a function of amplifier bias current.

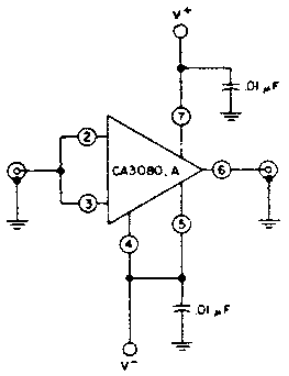


Fig. 19 — Input-to-output capacitance test circuit.

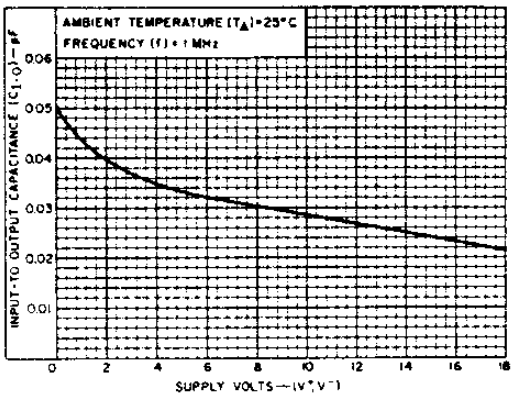


Fig. 20 — Input-to-output capacitance as a function of supply voltage.

APPLICATIONS

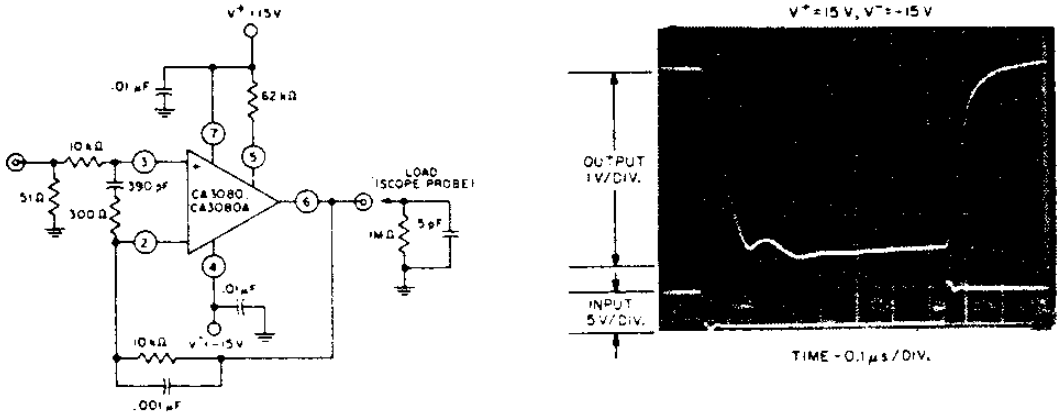


Fig. 21 — Schematic diagram of the CA3080 and CA3080A in a unity-gain voltage follower configuration and associated waveform.

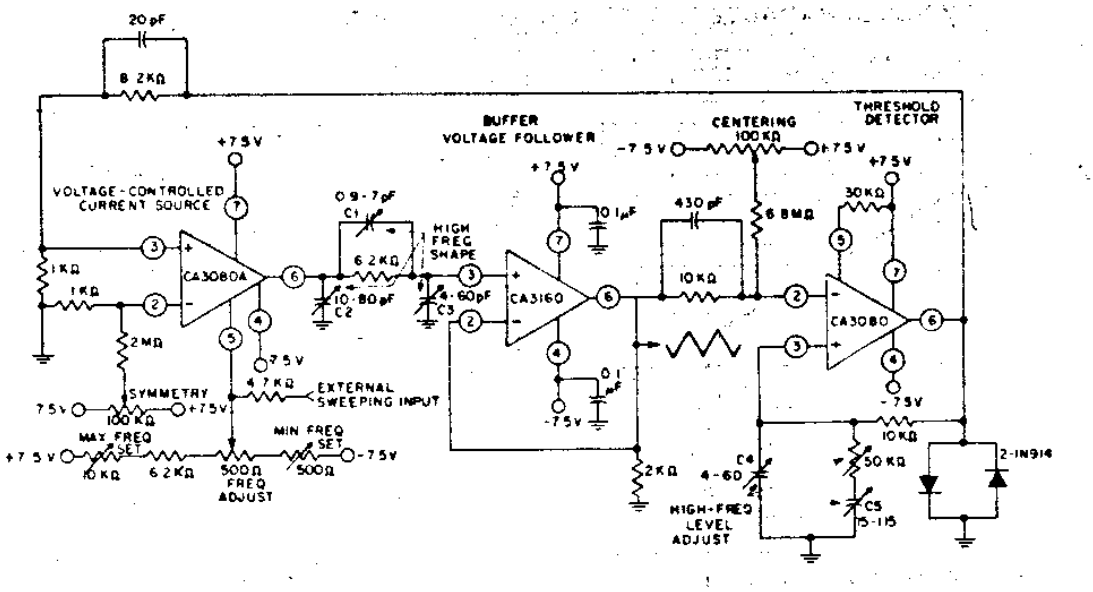
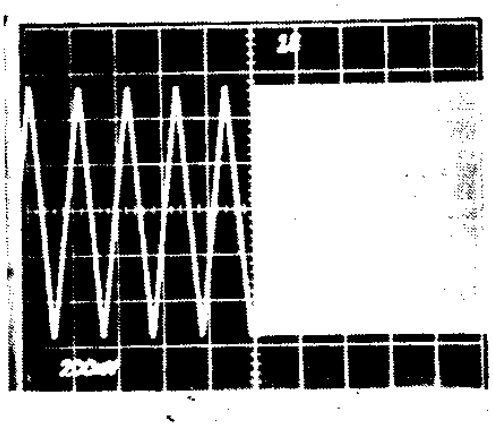
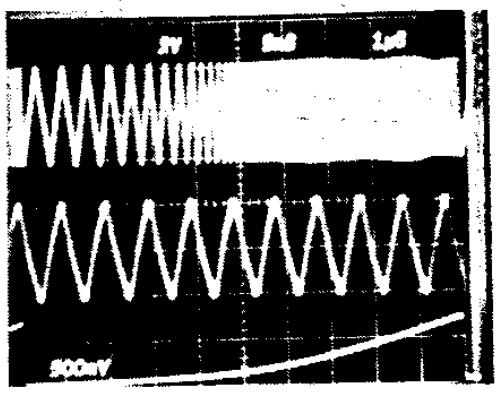


Fig.22 – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.

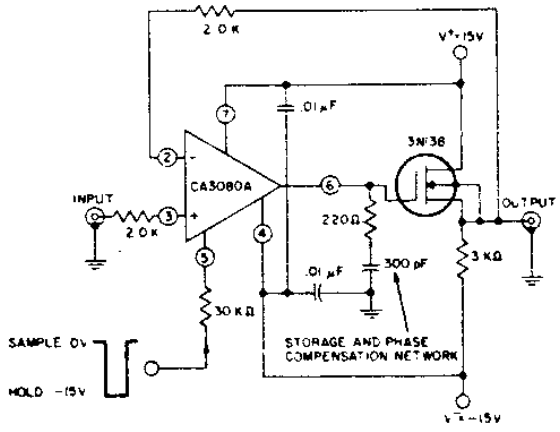


(a) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.



(b) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Fig.23 – Function generator dynamic characteristics waveforms.



SLEW RATE IN SAMPLE MODE = 1.3 V/μs
ACQUISITION TIME* = 3 μs

* TIME REQUIRED FOR OUTPUT TO SETTLE WITHIN ±3mV OF A 4-VOLT STEP

Fig.24 – Schematic diagram of the CA3080A in a sample-hold configuration.

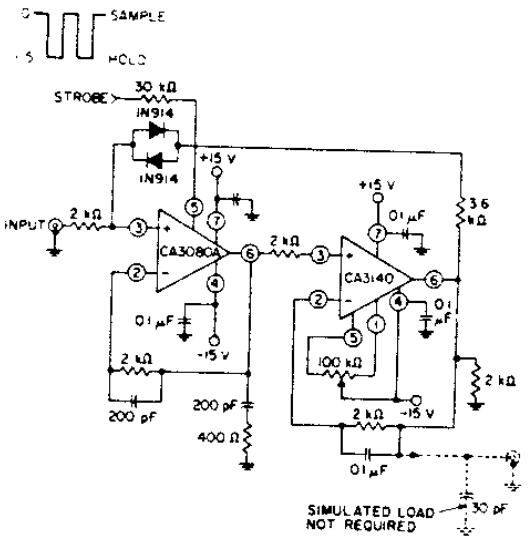
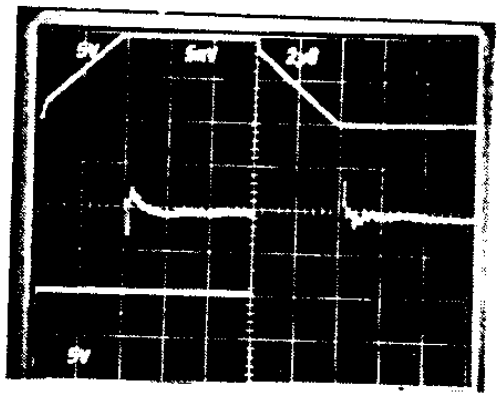
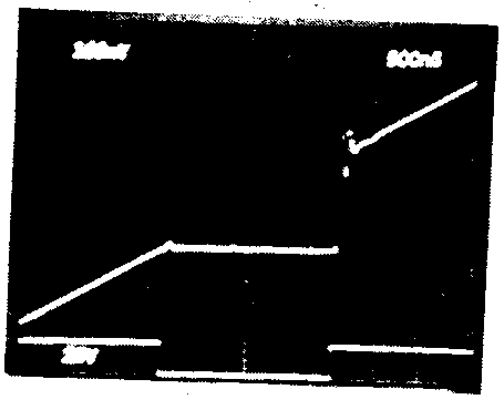


Fig.25 – Sample- and hold circuit.



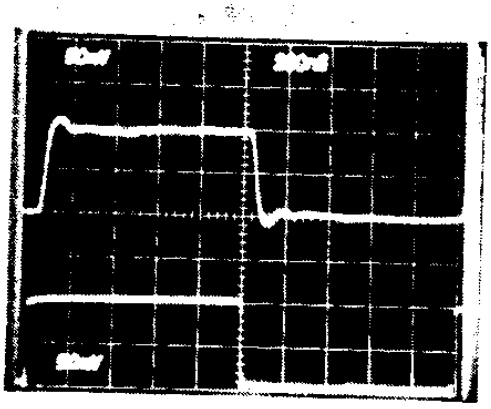
LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE : OUTPUT SIGNAL
(5 V/DIV AND 2 μs/DIV.)
BOTTOM TRACE : INPUT SIGNAL
(5 V/DIV AND 2 μs/DIV.)
CENTER TRACE DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5 mV/DIV AND 2 μs/DIV.)

Fig.26 – Large-signal response and settling time for circuit shown in Fig.25.



SAMPLING RESPONSE
TOP TRACE : SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE : SAMPLING SIGNAL
(20 V/DIV AND 500 ns/DIV.)

Fig.27 – Sampling response for circuit shown in Fig. 25.



TOP TRACE : OUTPUT
(50 mV/DIV AND 200 ns/DIV.)
BOTTOM TRACE : INPUT
(50 mV/DIV AND 200 ns/DIV.)

Fig.28 – Input and output response for circuit shown in Fig. 25.

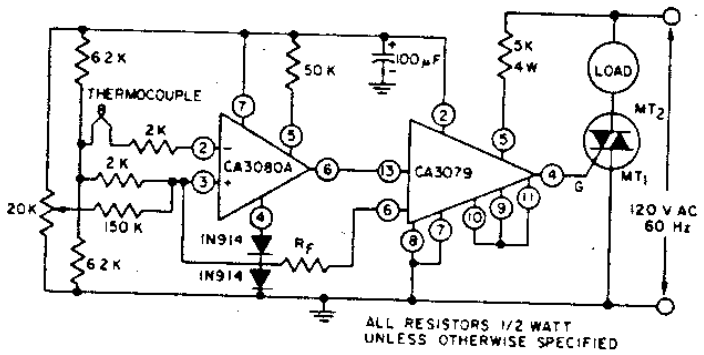


Fig.29 – Thermocouple temperature control with CA3079 zero voltage switch as the output amplifier.

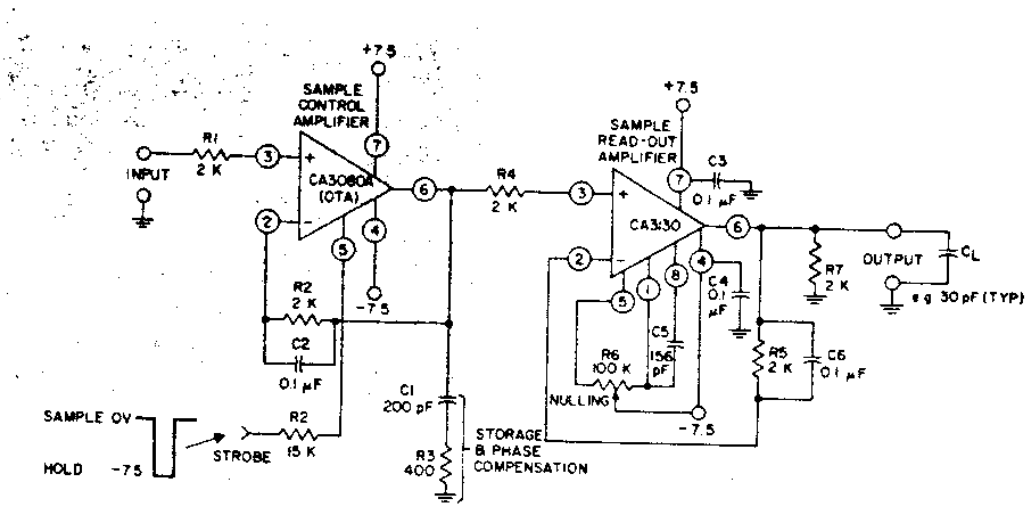
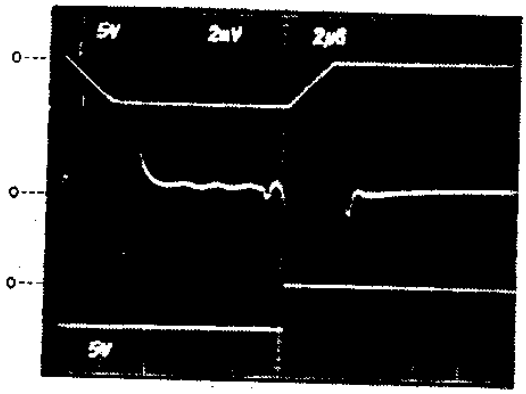
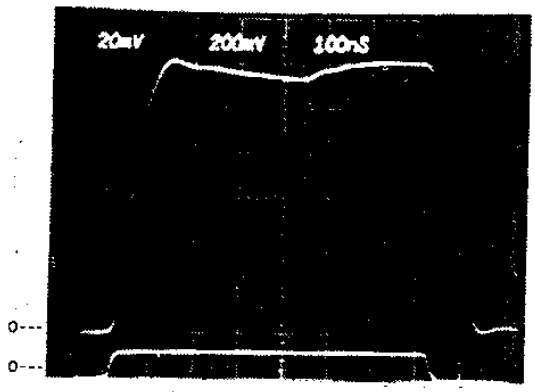


Fig.30 – Schematic diagram of the CA3080A in a sample-hold circuit with BiMos output amplifier.



TOP TRACE: OUTPUT—5 V/DIV. @ 2 μs/DIV.
CENTER TRACE: DIFFERENTIAL COMPARISON OF INPUT & OUTPUT—2 mV/DIV. @ 2 μs/DIV
BOTTOM TRACE: INPUT—5 V/DIV. @ 2 μs/DIV.

Fig.31 – Large-signal response for circuit shown in Fig. 30.



TOP TRACE: OUTPUT—20 mV/DIV @ 100 ns/DIV.
BOTTOM TRACE: INPUT—200 mV/DIV. @ 100 ns/DIV.

Fig.32 – Small-signal response for circuit shown in Fig. 30.

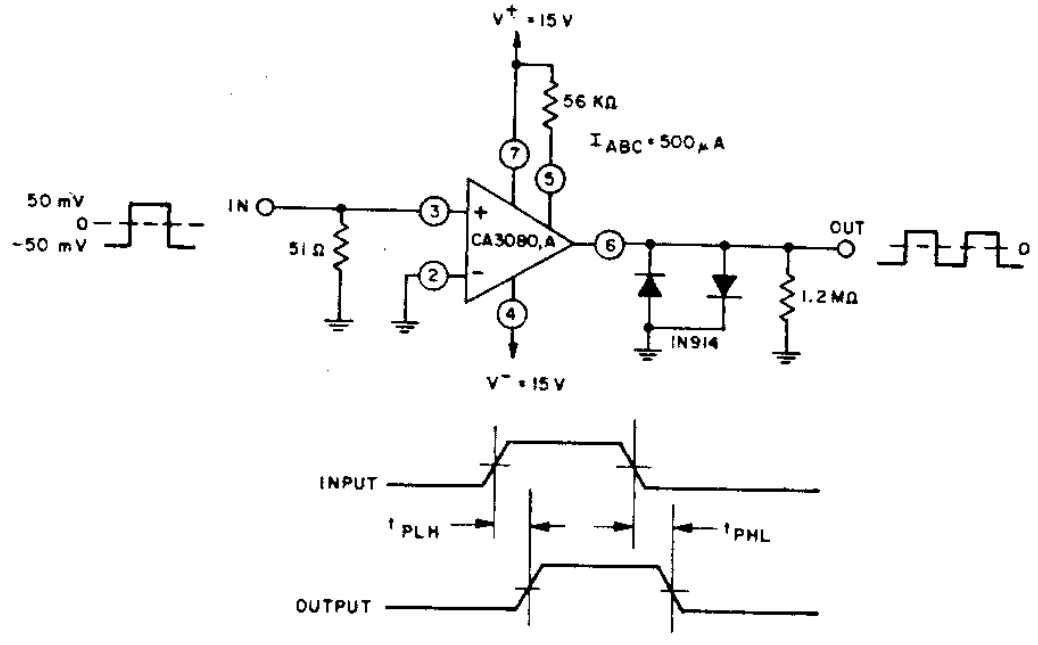


Fig. 33 - Propagation delay test circuit and associated waveforms.