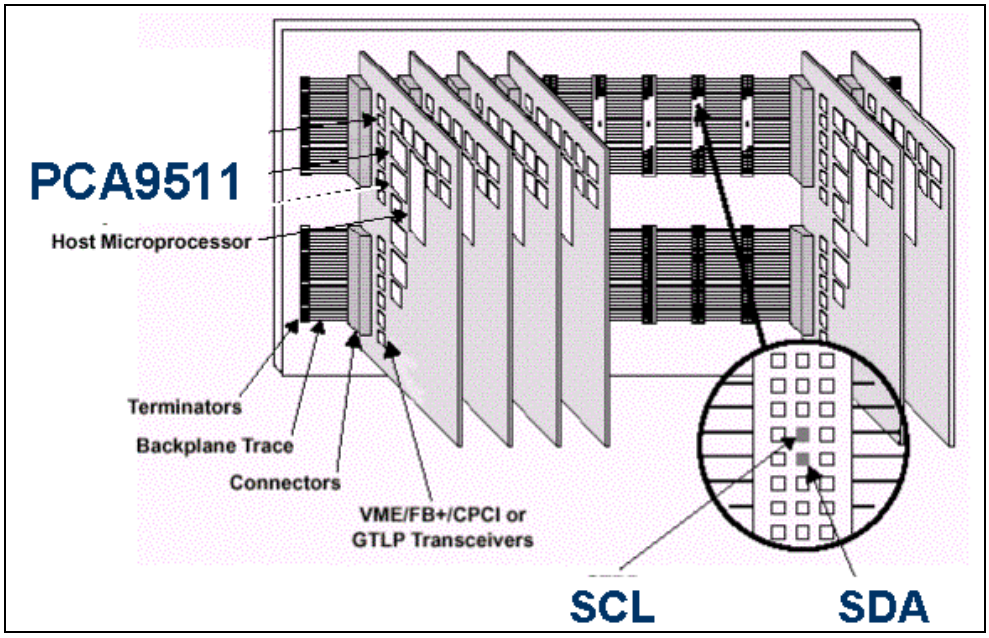
APPLICATION NOTE (preliminary)



AN10160_1
LEVEL SHIFTING I²C and SMBus HOT SWAPPABLE BUS BUFFERS

PCA9511, PCA9512, PCA9513, PCA9514

Abstract - Philips Semiconductors family of Hot Swap Bus Buffers are detailed in this application note that discusses device operation, maximum cable length and frequency calculations and typical applications.

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Philips Semiconductors **June 9, 2003**

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OVERVIEW

Description

The PCA9511/12/13/14 series of level shifting hot swappable I^2C and SMBus bus buffers allow I/O card insertion into a live backplane without corruption of the I^2C data and clock busses. When the connection is made, the devices provide bi-directional buffering, keeping the backplane I^2C bus and card I^2C bus capacitances isolated. Rise-time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. During insertion, the SDA and SCL lines are precharged to 1V (PCA9511/12 only) to minimize bus disturbances.

The PCA9511/13/14 incorporates a CMOS threshold digital ENABLE input pin, which forces the part into a low current mode when driven to ground and sets normal operation when driven to V_{CC}. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together.

The PCA9512 replaces the ENABLE pin with a dedicated supply voltage pin, V_{CC2}, for the card side, providing level shifting between 3.3 V and 5 V systems with optimal noise margin. Both the backplane and card may be powered with supply voltages ranging from 2.7 V to 5.5 V, with no constraints on which supply voltage is higher. The PCA9512 replaces the READY pin with a digital CMOS input pin, ACC, which enables or disables the built-in rise-time accelerator currents for lightly loaded circuits.

The PCA9511, PCA9512, PCA9513 and PCA9514 allow a larger or longer I^2C or SMBus system where the following constraints previously restricted its size:

a) More I^2C devices or larger wiring capacitance than the 400 pF maximum allowed in the I^2C specifications.
b) Long bus wiring or multi-point backplane traces
c) Different operating supply voltages or logic voltage levels within one system
d) Isolation of a section of a system that has lost its power supply
e) Insertion of unpowered cards into an active I^2C bus

The PCA9511/12/13/14 are designed to work with I^2C clock frequencies up to 400 kHz and are suitable for utilization in a multi-master I^2C bus or SMBus environment. They are specifically designed for backplane multi-point applications and hot swap applications. The devices support bus arbitration and contention with bus masters located on any segment. They are bi-directional and require no direction control.

Operational voltage supply is 2.7 V to 5.5 V with 5.5 V tolerant I/Os.
Operational temperature range is -40 ºC to 85 ºC.

The PCA9511DP is a replacement for the Linear Tech LTC4300-1IMS8 and LTC4300-1CMS8.
The PCA9512DP is a replacement for the Linear Tech LTC4300-2IMS8 and LTC4300-2CMS8.

Applications

These hot swap devices can be used for a wide variety of applications:

I^2C or SMBus Extension – The PCA9511/12/13/14 Hot Swap Bus Buffers supports two I^2C or SMBus branches of 400 pF as shown in Figure 1. They allow extension of the I^2C or SMBus on systems requiring capacitance loads larger than the 400 pF maximum specified by the I^2C protocol. Designers can extend the use of the I^2C or SMBus in systems with more devices and / or longer bus lengths with only one repeater delay between any devices. The devices are multi master capable and support arbitration and bus contention on any segment.

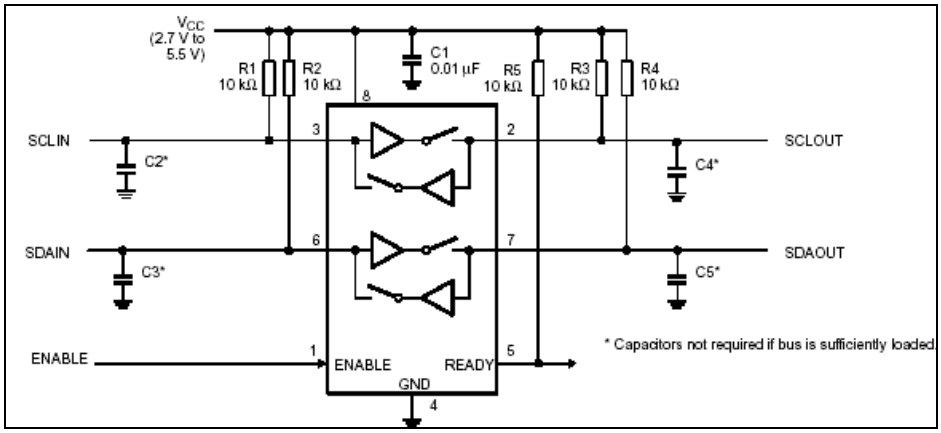

Figure 1. Typical Bus Buffer Application

I²C or SMBus Isolation - The PCA9511/13/14 have an individual repeater channel with an enable/disable feature that can be used to electrically isolate that segment of the I²C or SMBus. The PCA9512 does not have the enable/disable feature that was replaced with the rise time accelerator enable/disable. All devices release their I/O pins should their supply voltage fail.

Examples where this isolation feature could be useful include:
1. Allow mixed operation of 100 kHz and 400 kHz devices on a combined bus by isolating the segment with 100 kHz devices from the rest of the 400 kHz system so that the 400 kHz devices can operate at their maximum speed.
2. Supporting the PCI management bus with 8 or more PCI slots.
3. Sensing multiple power supplies on different bus segments and providing automatic isolation of failed segments or segments suffering 'brown-out' of their power supplies.

Voltage Translation - The PCA9512 has two V_{CC} supply inputs specifically designed for voltage translation applications and allow voltage translations between 2.7 V and 5.5 V to voltages between 2.7 V and 5.5 V. Having two voltage supplies ensures that the noise margin on each side is optimal with Vih set at $0.7V_{CC}$ and Vil set at $0.3\ V_{CC}$. The PCA9511/13/14 also support logic level translations since either side voltage can range from 2.7 V to 5.5 V and both sides do not need to be at the same voltage level but both sides are set at the same input voltage levels based on V_{CC} so the noise margin is not as good.

The GTL2000/02/10 devices allow I²C voltage level translation at any voltage between 1.0 V and 5.0 V to any voltage between 1.0 V and 5.0 V. See application note AN10145 Bi-Directional Voltage Translators for more information on the use of these passive devices to support voltage level translations. These GTL-TVC devices are less expensive than the PCA9511/12/13/14 Hot Swappable Bus Buffers but do not isolate the bus capacitance and rise time is dependant on the RC time constant.

Hot Swapping Slave Cards - The PCA9511/12 are featured with special circuitry that precharges the SDA and SCL pins to prevent glitching data on an active I²C bus when the unpowered slave card is inserted into the system. They also feature an idle detect circuit that will not connect the active I²C bus to the slave device I²C bus until the bus is idle. The PCA9513/14 also have the idle detect feature but do not have the precharge feature since it is not needed or desired in some applications. All devices are designed for systems that include Intel IPMI (Intelligent Platform Management Interface), VME and PICMG (PCI Industrial Computer Manufacturers Group) CompactPCI® and AdvancedTCA™ architectures.

Internal Current Source as Pull Up Resistor Substitution - The PCA9513 has a 92 µA internal current source. This current source is substituted for the external bus pull up resistors normally found on the backplane I²C bus. If each card uses the PCA9513, as cards are added or removed, the I²C bus RC time constant stays the same since as card capacitance is added, the effective resistance decreases. This option was designed for PICMG 2.9 and PICMG 3.x applications.

Figure 2 shows the PCA9511/12/13/14 used in a typical backplane hot swap application with the device located on the card edge to isolate and buffer the backplane and card capacitance.

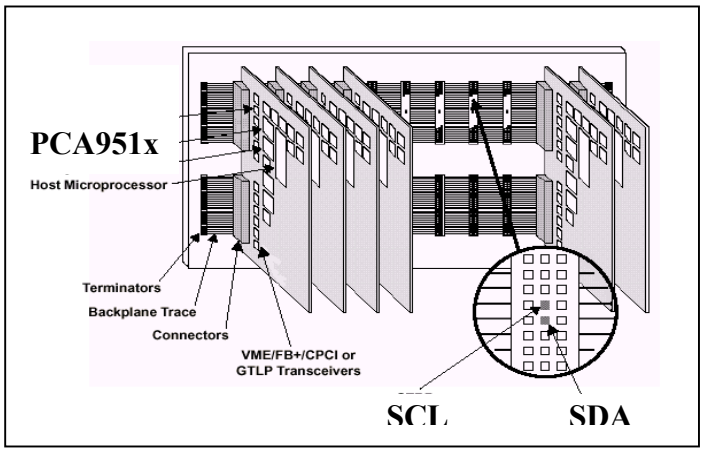

Figure 2. PCA9511/12/13/14 Typical Multi-Point Hot Swap Application

Device Features and Characteristics

- Bi-directional buffer for the SDA and SCL lines designed to prevent I^2C bus corruption during live board insertion and removal from the backplane
- Idle detect circuit connects board only when bus is idle
- 1 V precharge on all SDA and SCL lines prevents data glitch (PCA9511/12 only)
- Compatible with I^2C standard mode, I^2C fast mode, and SMBus standards, multi-master capable
- $\Delta V/\Delta t$ rise time accelerators on all SDA and SCL lines
- Rise time accelerator enable/disable (PCA9512 only)
- Low I_{CC} chip enable/disable: <1 mA (PCA9511/13/14 only)
- READY open-drain output (PCA9511/13/14 only)
- 92 μA current source for PICMG 2.9 and 3.x applications (PCA9513 only)
- Operating voltage range is 2.7 V to 5.5 V with 5.5 V tolerant I^2C and enable pins
- Two V_{CC} pins for optimal 3.3 V and 5 V level translation (PCA9512 only)
- Operating temperature range is -40 ºC to 85 ºC
- ESD protection exceeds:
  - 2000 V HBM per JESD22-A114
  - 200 V MM per JESD22-A115
  - 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Offered in 8-pin SO (D) and TSSOP (MSOP) (DP) packages

FEATURE SELECTION CHART

FEATURES	PCA9511	PCA9513	PCA9514		PCA9512
Replacement for Linear Tech LTC4300-1	Yes	Same footprint	Same footprint		—
Replacement for Linear Tech LTC4300-2	—	—	—		Yes
Idle detect	Yes	Yes	Yes		Yes
High impedance SDA, SCL pins for V_{CC} = 0 V	Yes	Yes	Yes		Yes
Rise time accelerator circuitry on all SDA and SCL lines	Yes	Yes	Yes		Yes
Rise time accelerator circuitry hardware disable pin for lightly loaded systems	—	—	—		Yes
Rise time accelerator threshold 0.8 V vs 0.6 V improves noise margin	—	Yes	Yes		—
Low I_{CC} chip disable < 1 μA	Yes	Yes	Yes		—
Ready open drain output	Yes	Yes	Yes		—
Two V_{CC} pins to support 5 V to 3.3 V level translation with improved noise margins	—	—	—		Yes
1 V precharge on all SDA and SCL lines	Yes	—	—		Yes
92 μA current source on SCLIN and SDAIN for PICMG applications	—	Yes	—		—
Improve acknowledge and clock stretching behavior over LTC4300	Yes	Yes	Yes		Yes

Table 1. Device Selection Summary

Device Pinout

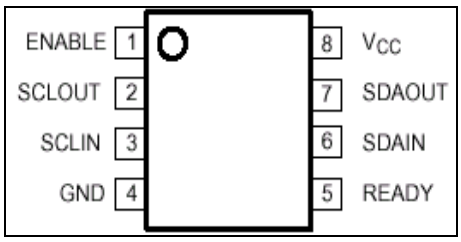

Figure 3. Device pinout for PCA9511/13/14

Pin Functions

- **ENABLE (Pin 1):**
  Chip Enable Pin. This is a digital CMOS threshold input pin. Grounding this pin puts the part in a low current (<1μA) mode. It also disables the rise-time accelerators, disables the bus precharge circuitry, drives READY low, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT. Drive ENABLE all the way to V_{CC} for normal operation. Connect ENABLE to V_{CC} if this feature is not being used.
- **SCLOUT (Pin 2):**
  Serial Clock Output. Connect this pin to the SCL bus on the card.
- **SCLIN (Pin 3):**
  Serial Clock Input. Connect this pin to the SCL bus on the backplane.
- **GND (Pin 4):**
  Ground. Connect this pin to a ground plane for best results.
- **READY (Pin 5):**
  Connection Flag. This is an open-drain NMOS output that pulls low when either ENABLE is low or the start-up sequence described in the Operation section has not been completed. READY goes high when ENABLE is high and start-up is complete. Connect a 10k resistor from this pin to V_{CC} to provide the pull up.
- **SDAIN (Pin 6):**
  Serial Data Input. Connect this pin to the SDA bus on the backplane.
- **SDAOUT (Pin 7):**
  Serial Data Output. Connect this pin to the SDA bus on the card.
- **V_{CC} (Pin 8):**
  Main Input Power Supply from Backplane. This is the supply voltage for the devices on the backplane I^2C busses. Connect pull-up resistors from SDAIN and SCLIN to this pin.

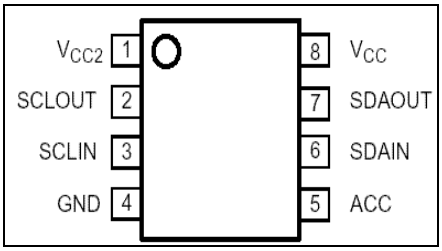

Figure 4. Device Pinout for the PCA9512

Pin Functions

- **V_{CC2} (Pin 1):**
  Card Supply Voltage. This is the supply voltage for the devices on the card I^2C busses. Connect pull-up resistors from SDAOUT and SCLOUT to this pin. Place a bypass capacitor of at least 0.01μF close to this pin for best results.
- **SCLOUT (Pin 2):**
  Serial Clock Output. Connect this pin to the SCL bus on the card.
- **SCLIN (Pin 3):**
  Serial Clock Input. Connect this pin to the SCL bus on the backplane.
- **GND (Pin 4):**

Ground. Connect this pin to a ground plane for best results.

- **ACC (Pin 5):**
  Rise-Time Accelerator Control. This is a CMOS threshold digital input pin that enables and disables the rise-time accelerators on all four SDA and SCL pins. Drive ACC all the way to the V_{CC2} supply voltage to enable all four accelerators; drive ACC to ground to turn them off.
- **SDAIN (Pin 6):**
  Serial Data Input. Connect this pin to the SDA bus on the backplane.
- **SDAOUT (Pin 7):**
  Serial Data Output. Connect this pin to the SDA bus on the card.
- **V_{CC} (Pin 8):**
  Main Input Power Supply from Backplane. This is the supply voltage for the devices on the backplane I^2C busses. Connect pull-up resistors from SDAIN and SCLIN to this pin.

Ordering Information

Package	Container	PCA9511	PCA9512	PCA9513	PCA9514
SO	Tube	PCA9511D	PCA9512D	PCA9513D	PCA9514D
	T & R	PCA9511D-T	PCA9512D-T	PCA9513D-T	PCA9514D-T
TSSOP	T & R	PCA9511DP-T	PCA9512DP-T	PCA9513DP-T	PCA9514DP-T

Table 2. Ordering Information

In Europe and Asia, add ",112" for tube orders and substitute ",118" for "-T" for tape and reel orders (e.g., PCA9511D,112 and PCA9511D,118). Additional information on packages including outline dimensions, MSL ratings, Theta JA can be obtained at www.philipslogic.com/packaging.

Note: The devices are sampling and samples can be requested from your Philips sales representative or by e-mail to pc.mb.svl@philips.com. Device release is planned for 4Q03 through 1Q04.

Data Sheets and IBIS/SPICE Models

Data sheets and IBIS models can be downloaded from www.philipslogic.com.
SPICE models require a device specific NDA. Encrypted SPICE models are available that do not require a NDA. Request SPICE models at pc.mb.svl@philips.com

TECHNICAL INFORMATION

Block Diagram

The PCA9511/12/13/14 are bi-directional translators that require no external directional control and are specifically designed to support a multi-master I^2C/SMBus environment where masters can be located on both sides of the device. The PCA9511/12/13/14 operates at a supply voltage from 2.7 V to 5.5 V with 5.5 V tolerant I/Os. All devices are similar with slight differences as shown in Table 1. The block diagram for the PCA9511 is shown in Figure 5.

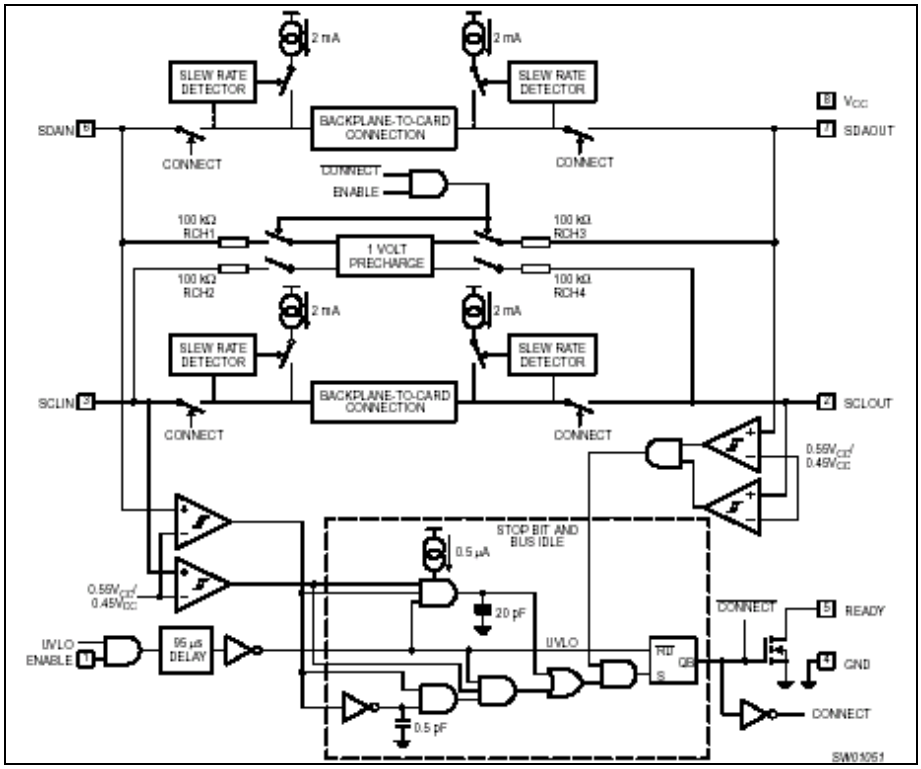

Figure 5. PCA9511 Block Diagram

The block diagram for the PCA9512 is shown in Figure 6. The PCA9512 is different from the PCA9511/13/14 since it has two separate V_{CC} pins so that the noise margin is optimized for both sides at $0.3V_{CC}$ and $0.7V_{CC}$ for any voltage between the range of 2.7 V and 5.5 V and the rise time accelerator can be disabled for use in lightly loaded systems.

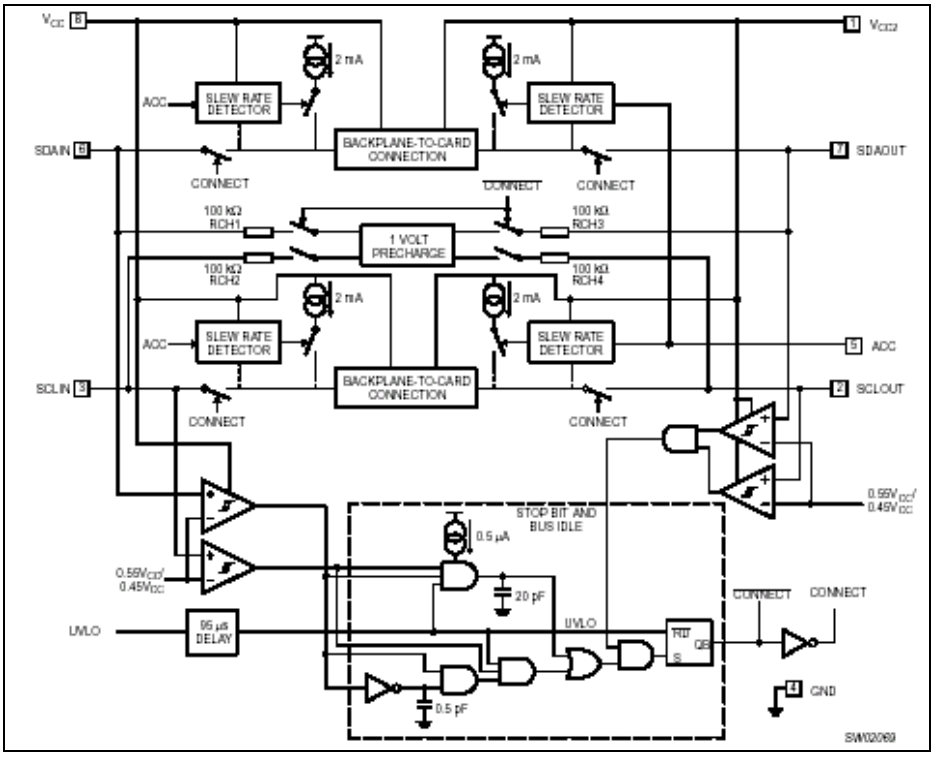

Figure 6. PCA9512 Block Diagram

The block diagram for the PCA9513 is shown in Figure 7. The special feature of this device is the internal 92 μA current source that replaces the pull up resistor on the backplane I^2C SDA and SCL lines.

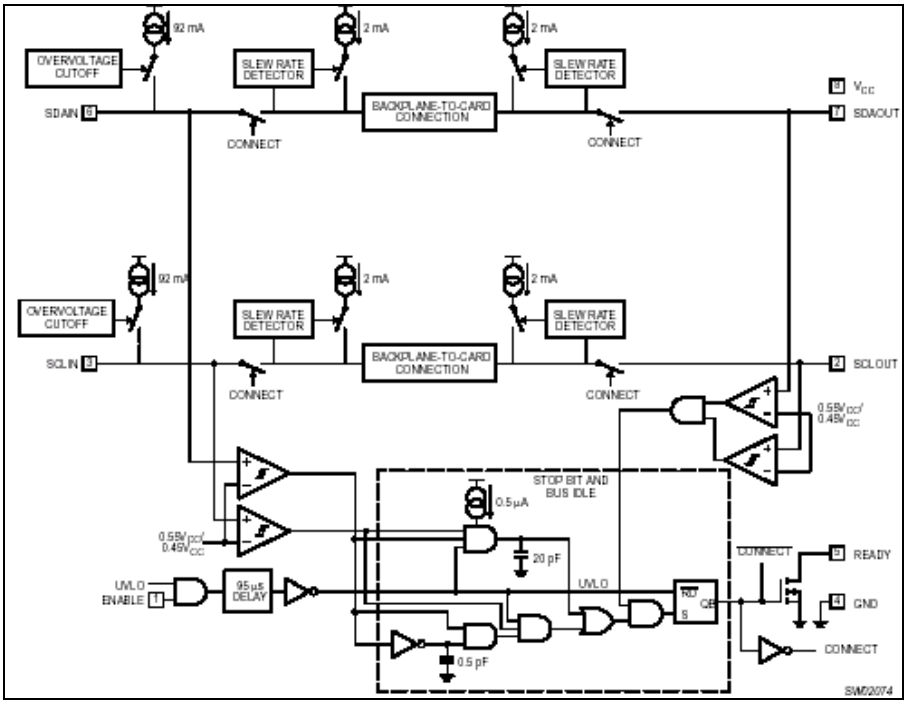

Figure 7. PCA9513 Block Diagram

The block diagram for the PCA9514 is shown in Figure 8. The PCA9514 is like the PCA9513 except it does not have the internal 92 μA current source.

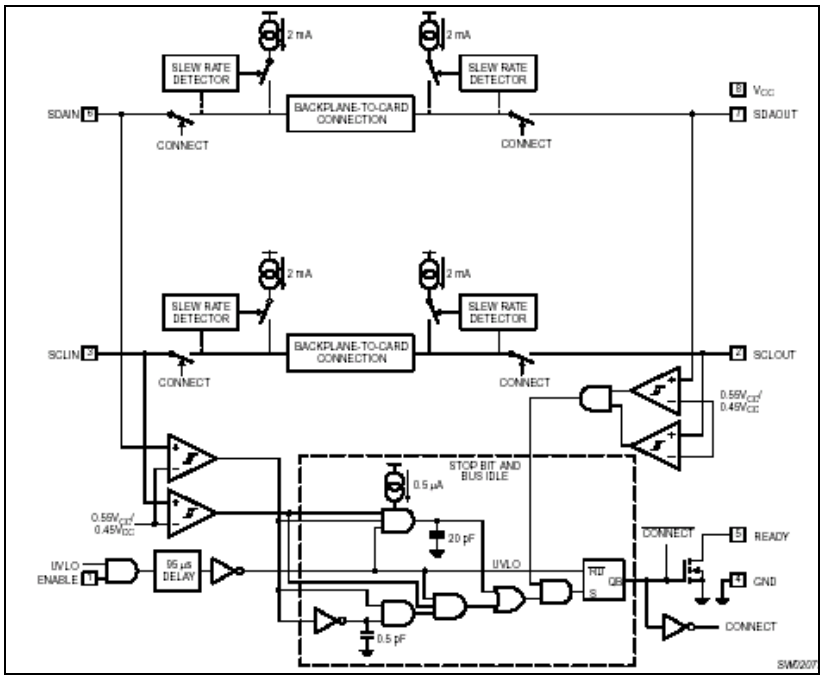

Figure 8. PCA9514 Block Diagram

There are no external hardware address pins since these devices do not have an I^2C address. The bus buffer devices merely buffer the I^2C signals from segment to segment and do not respond to any I^2C commands.

Operation

Start-Up

When the PCA9511/12/13/14 devices first receive power on their V_{CC} pin, either during power-up or during hot swapping, they start in an under voltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until V_{CC} rises above 2.5 V. For the PCA9512, the part also waits for V_{CC2} to rise above 2 V. This ensures that the part does not try to function until it has enough voltage to do so. During this time, the 1 V precharge circuitry (PCA9511/12 only) is active and forces 1 V through internal100 kΩ nominal resistors to the SDA and SCL pins.

Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0 V and V_{CC}. Precharging the SCL and SDA pins to 1 V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing the amount of disturbance caused by the I/O card. The PCA9513/14 do not have the precharge feature since in some cases, it is detrimental to proper system response, most I^2C devices having a 50 ns input filter that will screen out glitches and nanosecond discontinuities between the pin and socket negate the effect of the precharge. TYCO Quiet Mate™ pins provide the best protection in live insertion applications (see Texas Instruments DesignCon 2001 paper titled "GTLP in Live Insertion Applications" for more information on glitching open drain buffer during live insertion and Quite Mate™ pins).

Once the PCA9511/12/13/14 come out of the UVLO state, it is assumed that SDAIN and SCLIN have been hot swapped into a live system and that SDAOUT and SCLOUT are being powered up at the same time as the devices themselves. Therefore, they look for either a Stop command or a bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the parts also verify that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane.

Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT force a high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the PCA9511/12/13/14.

Another key feature of the connection circuitry is that it provides bi-directional buffering, keeping the backplane and card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms, as described here.

Input to Output Offset Voltage

When a logic low voltage, V_{LOW1}, is driven on any of the PCA9511/12/13/14's data or clock pins, the device regulates the voltage on the other side of the chip, V_{LOW2}, to a slightly higher voltage, as directed by the equation below:

$$V_{LOW2} = V_{LOW1} + 50mV + 100 \frac{V_{CC}}{R}$$

Where:

- R is the bus pull-up resistor at the output in Ω.
- V_{CC} is the voltage applied to the pull-up resistor in V

For example, if a device is forcing SDAOUT to 10 mV and V_{CC} = 3.3 V and the pull-up resistor R on SDAIN is 10kΩ, then the voltage on SDAIN = 10 mV + 50 mV + 100 • (3.3/10000) = 93 mV. See the Typical Performance Characteristics section of the data sheets for curves showing the offset voltage as a function of V_{CC} and R.

Propagation Delays

During a rising edge, the rise-time on each side is determined by the combined pull-up current of the PCA9511/12/13/14 boost current , the bus resistor and the equivalent capacitance on the line. If the pull-up currents are the same, a difference in rise-time occurs which is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 9 for V_{CC} = 3.3 V and a 10kΩ pull-up resistor on each side (50 pF on one side and 150 pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective t_{PLH} is negative. There is a finite propagation delay, t_{PHL}, through the connection circuitry for falling waveforms.

(Figure to be inserted later)

Figure 9. Input-Output Connection t_{PLH}

Figure 10 shows the falling edge waveforms for the same V_{CC}, pull-up resistors and equivalent capacitance conditions as used in Figure 9.

(Figure to be inserted later)

Figure 10. Input-Output Connection t_{PHL}

An external NMOS device pulls down the voltage on the side with 150 pF capacitance; the PCA9511/12/13/14 devices pull down the voltage on the opposite side, with a delay of 55 ns. This delay is always positive and is a function of supply voltage, temperature, pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section in the data sheet shows t_{PHL} as a function of temperature and voltage for 10kΩ pull-up resistors and 100 pF equivalent capacitance on both sides of the part. By comparison with Figure 10, the V_{CC} = 3.3 V curve shows that increasing the capacitance from 50 pF to 150 pF results in a t_{PHL} increase from 55 ns to 75 ns. Larger output capacitances translate to longer delays (up to 150 ns). Users must quantify the difference in propagation times for a rising edge vs a falling edge in their systems and adjust setup and hold times accordingly.

Rise-Time Accelerators

Once connection between the 2 sides has been established, rise-time accelerator circuits on all four SDA and SCL pins are activated. These allow the user to choose weaker DC pull-up currents on the bus, reducing power consumption while still meeting system rise-time requirements. During positive bus transitions, the PCA9511/12/13/14 devices switch a 2 mA current source to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6 V (0.8 V for the PCA9513/14).

Using a general rule of 20 pF of capacitance for every device on the bus (10 pF for the device and 10 pF for interconnect), choose a pull-up current so that the bus will rise on its own at a rate of at least 1.25 V/µs to guarantee activation of the rise-time accelerators. For example, assume an SMBus system with V_{CC} = 3.3 V, a 10kΩ pull-up resistor and an equivalent bus capacitance of 200 pF. The rise-time of an SMBus system is calculated from ($V_{IL(MAX)}$ − 0.15 V) to ($_{VIH(MIN)}$ + 0.15 V), or 0.65 V to 2.25 V. It takes 0.92•RC time constant to traverse this voltage for a 3.3 V supply; in this case, 0.92 • (10kΩ • 200 pF) = 1.85 µs. Thus, the system exceeds the maximum allowed rise-time of 1µs by 85%. However, using the rise-time accelerators, which are activated at a DC threshold of below 0.65 V, the worst-case rise-time is: (2.25 V – 0.65 V) • 200 pF/1 mA = 320 ns, which meets the 1µs rise-time requirement.

READY Digital Output (PCA9511/13/14 only)

This pin provides a digital flag that is low when either ENABLE is low or the start-up sequence described earlier in this section has not been completed. READY goes high when ENABLE is high and start-up is complete. The pin is driven by an open drain pull-down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10kΩ to V_{CC} to provide the pull-up.

ENABLE Low Current Disable (PCA9511/13/14 only)

Grounding the ENABLE pin:

- Disconnects the backplane side from the card side
- Disables the rise-time accelerators
- Drives READY low
- Disables the bus precharge circuitry
- Puts the part in a near-zero current state.

When the pin voltage is driven all the way to V_{CC}, the part waits for data transactions on both the backplane and card sides to be complete (as described in the Start-Up section) before reconnecting the two sides.

ACC Boost Current Enable (PCA9512)

Users having lightly loaded systems may wish to disable the rise-time accelerators. Driving the ACC pin to ground turns off the rise-time accelerators on all four SDA and SCL pins. Driving the ACC pin to the V_{CC2} voltage enables normal operation of the rise-time accelerators, as described in the Rise-Time Accelerators section above.

Design Constraints

Maximum Current - The bus can be operated at no more than 3 mA and the bus IR drops must be controlled such that the device sees 0.4 V or less V_{IL} during a contention condition or clock-stretching event. Normally the bus pull-up resistor would need to be at the opposite end of the bus segment from the device. The device bus pins are over voltage tolerant to 5.5 V so that the I^2C bus on one or all sides of the device can be operated at 5 V while the device is operated from a 3.3 V supply.

5 V Bus Operation - The bus pull-up resistors need to be tied to the 5 V supply if any 5 V parts are on the bus to guarantee that the V_{IH} of the 5 V device is reached. If no 5 V parts are used, a 3.3 V bus pull-up resistor supply should be used as this will result in a smaller RC time constant for the same 3 mA current.

Operation at 400 kHz - Fast- mode parts can only be operated at 400 kHz clock frequency if no standard-mode parts are on the bus. The maximum acceptable capacitive load for 400 kHz operation with a 3 mA current is 331 pF at V pull-up = 3.3 V +/- 0.3 V, and 208 pF at V pull-up = 5.0 V +/- 0.5 V, in order to satisfy the fast-mode rise time requirement.

Rise Time - Rise time must be less than or equal to 1000 ns because the device regenerates the I^2C signal, the pull-up voltages on either side need not be equal, i.e., one side could be 5 V +/- 0.5 V and the other side could be 3.3 V +/- 0.3 V.

Device Segment Enable - Only enable or disable the devices when all buses are in an idle state, to prevent system failures.

Resistor Pull-Up Value Selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value R using the formula:

$$R < \frac{800 \times 10^{-3} \cdot (V_{CC(MIN)} - 0.6)}{C}$$

Where R is the pull-up resistor value in Ω, $V_{CC(MIN)}$ is the minimum V_{CC} voltage in V and C is the equivalent bus capacitance in pF. In addition, regardless of the bus capacitance, always choose R < 16kΩ for V_{CC} = 5.5 V maximum, R < 24kΩ for V_{CC} = 3.6V maximum. The start-up circuitry requires logic high voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up resistor values are needed to overcome the precharge voltage. See the curves in Figure 11a and Figure 11b for guidance in resistor pull-up selection.

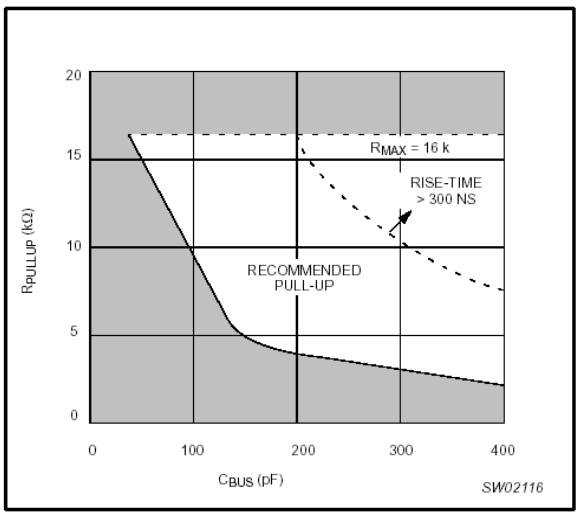

Figure 11a.
Bus Requirements for 3.3 V Systems

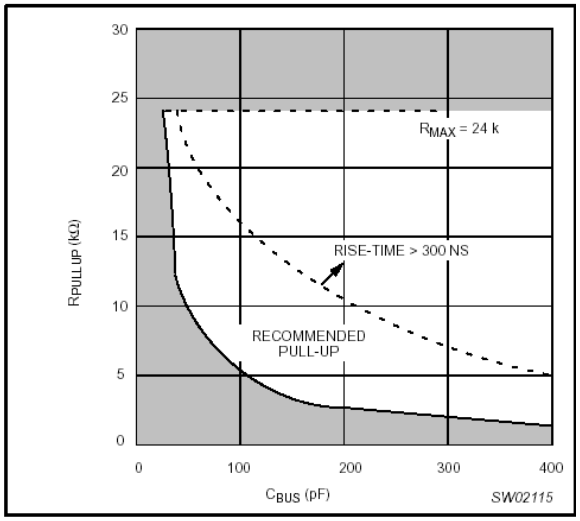

Figure 11b.
Bus Requirements for 5 V Systems

Minimum SDA and SCL Capacitance Requirements

The PCA9511/12/13/14 I/O connection circuitry requires a minimum capacitance loading on the SDA and SCL pins in order to function properly. The value of this capacitance is a function of V_{CC} and the bus pull-up resistance. Estimate the bus capacitance on both the backplane and the card data and clock busses, and refer to Figures 11 and 12 to choose appropriate pull-up resistor values. Note from the figures that 5 V systems must have at least 47 pF capacitance on their busses and 3.3 V systems must have at least 22 pF capacitance for proper operation of the PCA9511/12/13/14. For applications with less capacitance, add a capacitor to ground to ensure these minimum capacitance conditions.

Systems with Disparate Supply Voltages (PCA9511/13/14 only)

In large 2-wire systems, the V_{CC} voltages seen by devices at various points in the system can differ by a few hundred millivolts or more. This situation is well modeled by a series resistor in the V_{CC} line, as shown in Figure 12. For proper operation of the PCA9511/13/14, make sure that $V_{CC(BUS)} > V_{CC(PCA9511/13/14)} - 0.5$ V.

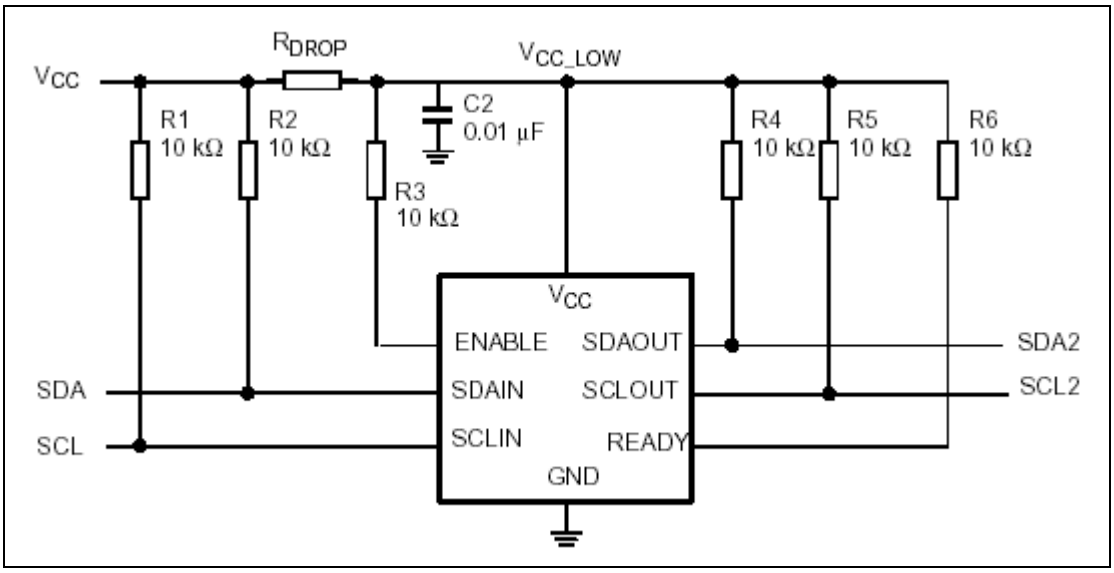

Figure 12. System with Disparate V_{CC} Voltages

Use of Multiple Devices in the same I^2C System

Multiple PCA9511/12/13/14 Hot Swap Bus Buffers can be used in series.

There are no fundamental restrictions on making series connections between any of the following groups…

a) The Tx/Rx side of P82B96
b) Either side of the PCA9511/12/13/14
c) Either side of P82B715
d) Either side of just one PCA9515/16, OR just one Sx connection of a single P82B96

The selected system impedance levels, voltages, and propagation delays of course need to be considered. Application Note AN255 Repeaters, Hubs and Expanders provide additional information.

APPLICATIONS

Bus Expansion beyond the 400 pF Limitation

Adding more I^2C and SMBus devices on the bus may exceed the 400 pF limitation. The PCA9511/12/13/14 can isolate device and trace capacitance to different segments that are 400 pF or less capacitive loading so that the I^2C and SMBus devices can operate properly. A typical PCA9511/12/13/14 application is shown in Figure 13.

If all masters are on one side of the PCA9511/12/13/14 bus buffer and none of the slaves on the other side of the bus buffer use clock stretching and if all of these slaves are capable of 6 mA I_{OL}, then the slave side pull-up can be sized for 6 mA because there will be no contention nor clock strectching to be communicated by the bus buffer.

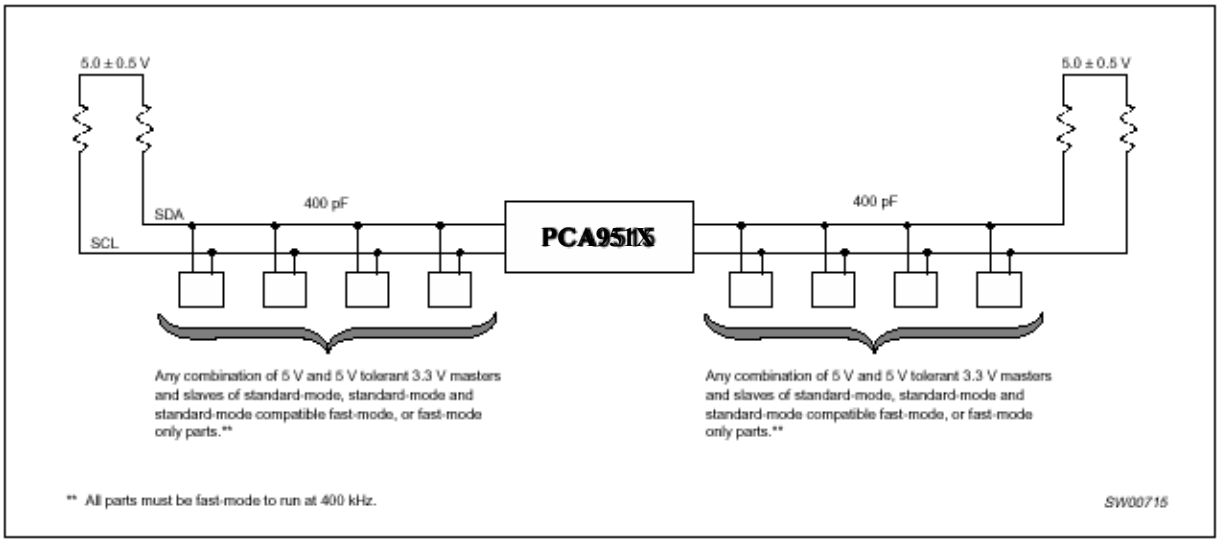

Figure 13. Typical Bus Expansion Application

Split Bus 100 kHz and 400 kHz Application

If all of the masters and slaves on the master side of the PCA9511/13/14 are capable of fast-mode operation, none of the slaves on the opposite side of the bus buffer require clock stretching and the master(s) is able to generate enable and disable changes during the bus idle time, then the enable feature of the PCA9511/13/14 could be used to isolate the master side to allow the master to run at 400 kHz rather than the standard-mode 100 kHz necessary when any standard-mode slave are present on the slave side of the repeater. The PCA9512 does not have an enable pin so it cannot be used.

If an individual slave is particularly badly behaved during power-up but performs correctly after power-up, or power-up and system reset on power-up, then the PCA9511/12/13/14 enable function could be used to isolate the offending part until it is well behaved and both sides of the bus buffer are in an idle state. The enable should never be changed, enabled nor disabled, except when both sides of the bus buffer are in an idle state. If the part being isolated is a slave that does not use clock stretching, then the isolation technique and the standard bus expansion technique can be combined.

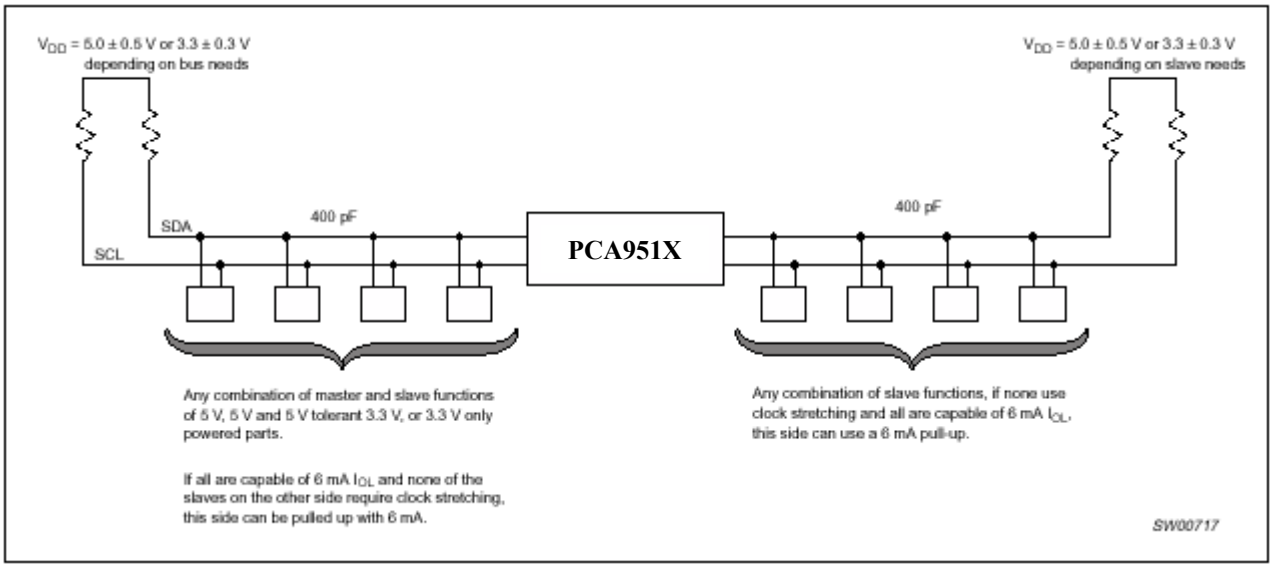

Figure 14. PCA9511/13/14 in Split Bus 100 kHz and 400 kHz Application

Voltage Level Shifting

Systems requiring different supply voltages for the backplane side and the card side can use the PCA9512, as shown in Figure 15. The pull-up resistors on the card side connect from SDAOUT to SCLOUT to V_{CC2}, and those on the backplane side connect from SDAIN and SCLIN to V_{CC}. The PCA9512 functions for voltages ranging from 2.7 V to 5.5 V on both V_{CC} and V_{CC2}. There is no constraint on the voltage magnitudes of V_{CC} and V_{CC2} with respect to each other and each side Vil is set at $0.3V_{CC}$ and the Vih is set at $0.7V_{CC}$ for that side. This application also provides power supply redundancy. If either the V_{CC} and V_{CC2} voltage falls below its UVLO threshold, the PCA9512 disconnects the backplane from the card, so that the side that is still powered can continue to function.

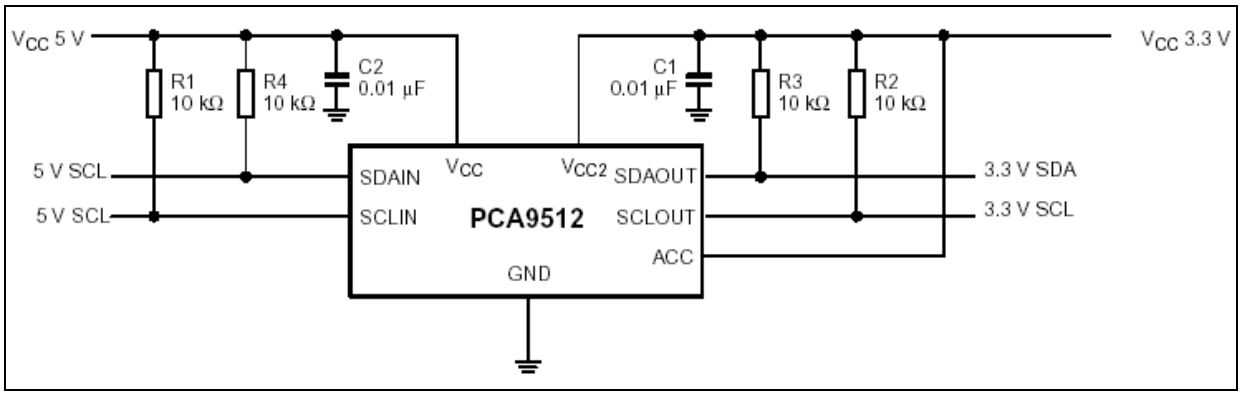

Figure 11. 5 V to 3.3 V Level Translator

The PCA9511/13/14 with one V_{CC} also allows translations between 3.3 V and 5 V since the I/Os are 5 V tolerant but does so with the Vil and Vih set on both sides at 0.3 and 0.7 of the single V_{CC}. The GTL2000/02/10 family of bi-directional low voltage translators can also be used to translate between any voltage between 1.0 V and 5.0 V but these devices do not buffer any capacitance. Refer to Application Note AN10145 Bi-Directional Low Voltage Translators for more information on the GTL level translators.

I^2C Multi-Point Hot Swap Applications

In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing a PCA9511/12/13/14 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O

card, the PCA9511/12/13/14 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the PCA9511/12/13/14 that is less than 10pF, the connector and the backplane trace.

Figure 16 shows the PCA9511/14 in a PICMG 2.9 CompactPCI/VME or PICMG 3.x AdvancedTCA configuration. Connect V_{CC} to the output of one of the power supply hot swap circuits and connect ENABLE to the short "board enable" pin. V_{CC} is monitored by a filtered UVLO circuit. With the V_{CC} voltage powering up after all other pins have established connection, the UVLO circuit ensures that the backplane and card data and clock busses are not connected until the transients associated with hot swapping have settled. Owing to their small capacitance, the SDAIN and SCLIN pins cause minimal disturbance on the backplane busses when they make contact with the connector.

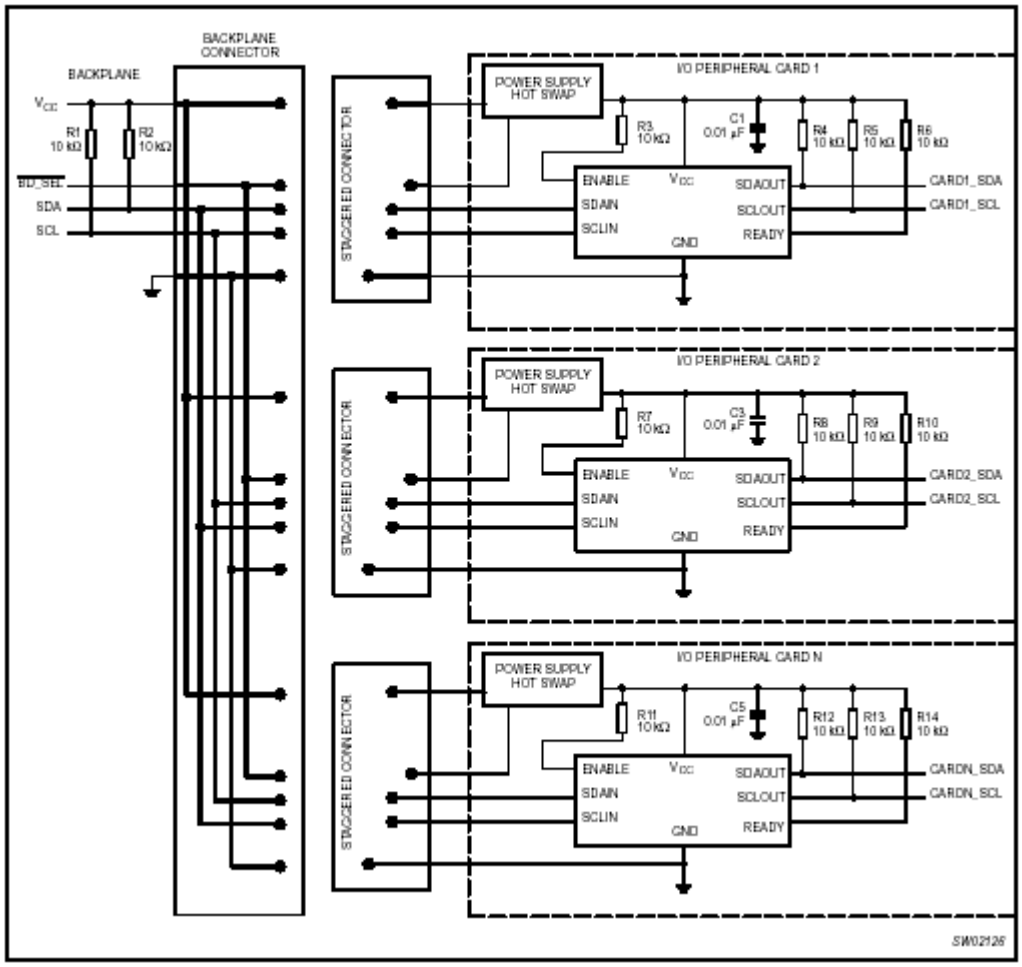

Figure 11. Hot Swapping Multiple I/O Cards into a Backplane Using thePCA9511/14 in a CompactPCI/VME or AdvancedTCA System

Figure 17 shows the PCA9512 in a PICMG 2.9 CompactPCI/VME or PICMG 3.x AdvancedTCA configuration. The PCA9512 receives its V_{CC} voltage from one of the long “early power” pins. Because this power is not switched, add a 5Ω to 10Ω resistor between the V_{CC} pins of the connector and the PCA9512, as shown in the figure. In addition, make sure that the V_{CC} bypassing on the backplane is large compared to the 0.01 μF bypass capacitor on the card. Establishing early power V_{CC} ensures that the 1 V precharge voltage is present at the SDAIN and SCLIN pins before they make contact. Connect V_{CC2} to the output of one of the power supply hot swap circuits. V_{CC2} is monitored by a filtered UVLO circuit. With the V_{CC2} voltage powering up after all other pins have established connection, the UVLO circuit ensures that the backplane and card data and clock busses are not connected until the transients associated with hot swapping have settled.

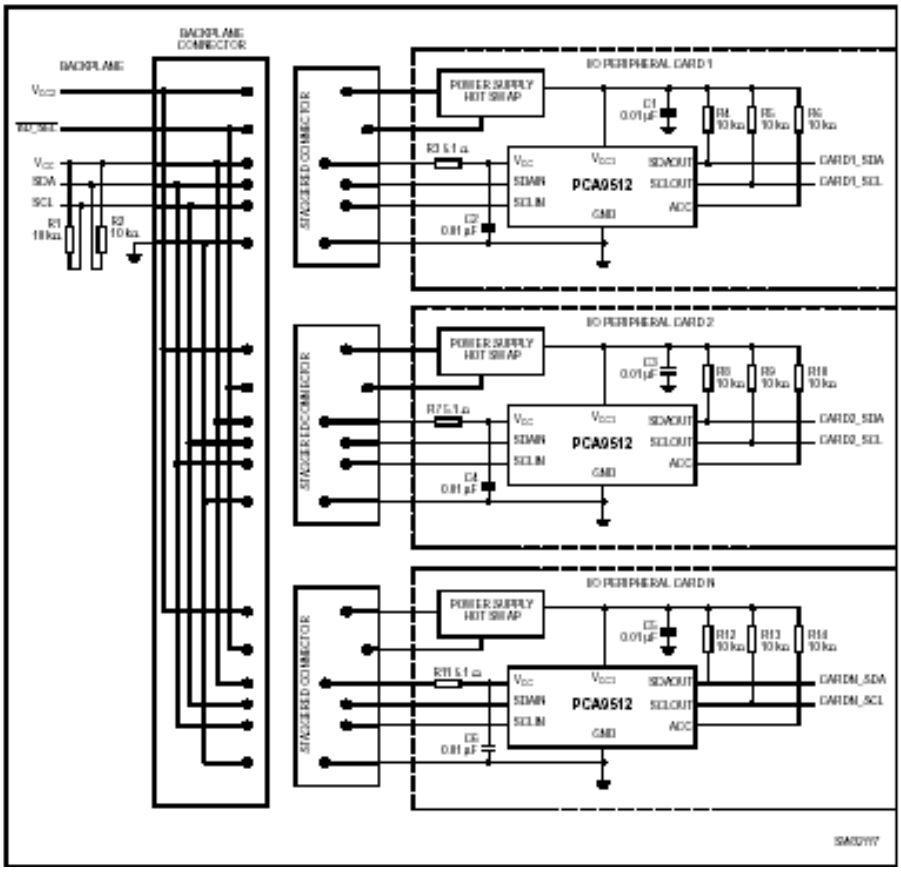

Figure 17. Hot Swapping Multiple I/O Cards into a Backplane Using the PCA9512 in a CompactPCI/VME or AdvancedTCA System

Figure 18 shows the PCA9513 in cPCI, VME or AdvancedTCA applications. The PCA9513 has a 92 μA internal current source. This current source is substituted for the external bus pull up resistors normally found on the backplane I^2C bus. Each card uses the PCA9513 and as cards are added or removed, the I^2C bus RC time constant stays the same since as card capacitance is added, the effective resistance decreases. This option was designed for PICMG 2.9 and PICMG 3.x applications.

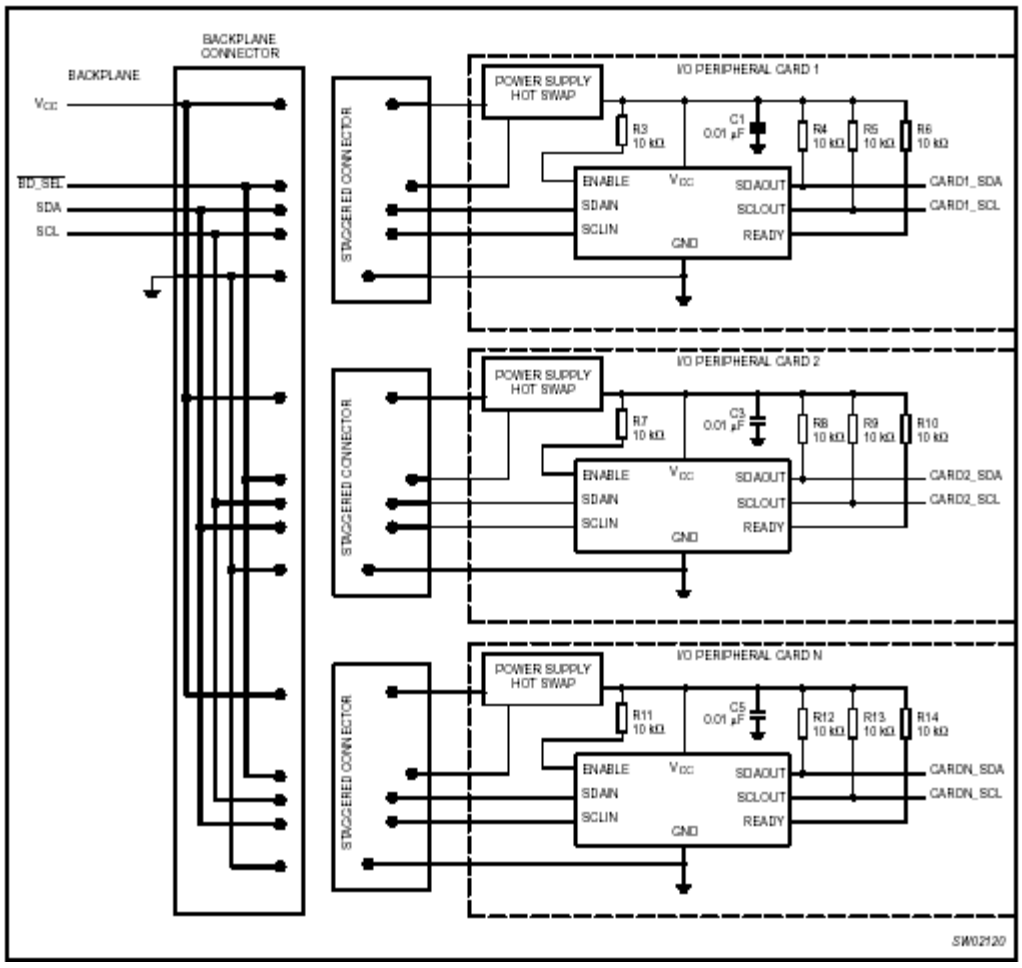

Figure 18. Hot Swapping Multiple I/O Cards into a Backplane Using the PCA9513 in a CompactPCI/VME or AdvancedTCA System

Figure 19 shows the PCA9511/14 in a PCI application, where all of the pins have the same length. In this case, connect an RC series circuit on the I/O card between V_{CC} and ENABLE. An RC product of 10 ms provides a filter to prevent the PCA9511/14 from becoming activated until the transients associated with hot swapping have settled.

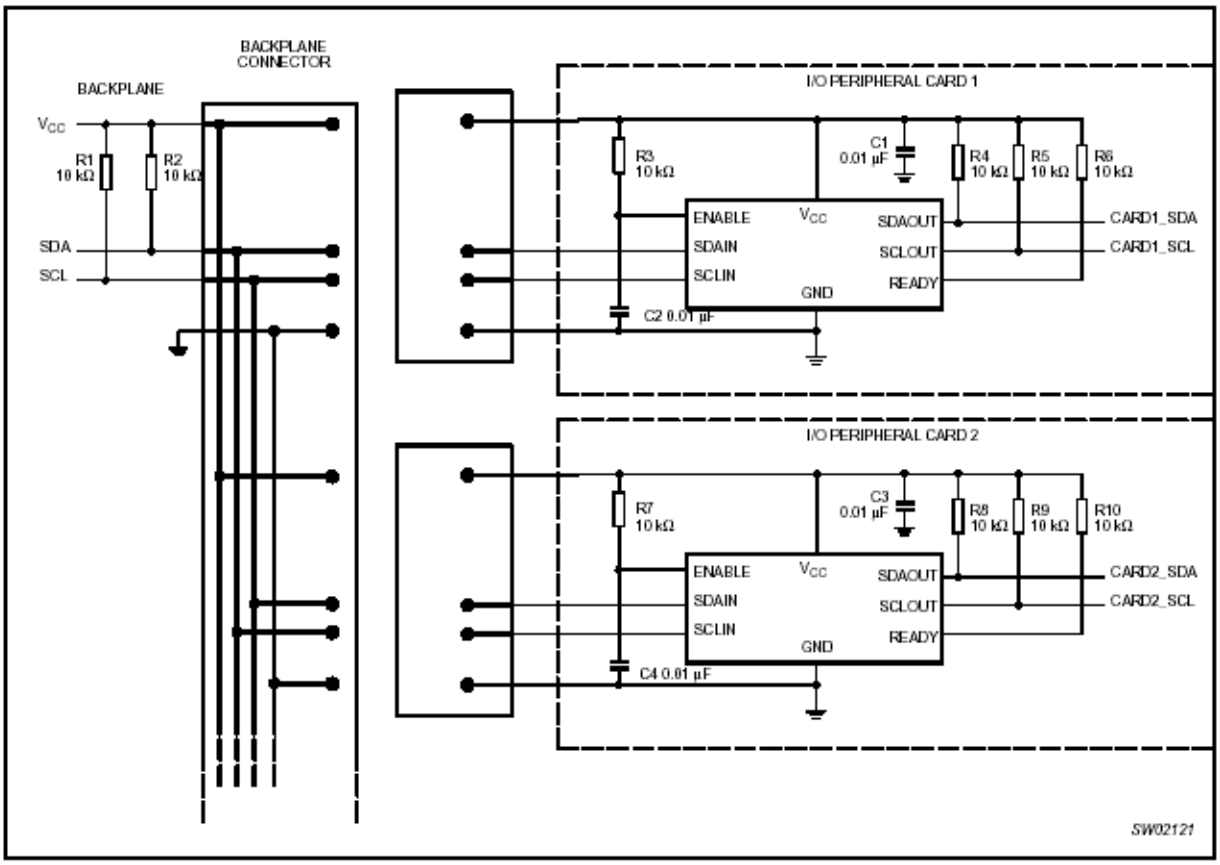

Figure 19. Hot Swapping Multiple I/O Cards into a Backplane Using the PCA9511/14 in a PCI System

Figure 20 shows the PCA9512 in an application where the user has a custom connector with pins of three different lengths available. Making V_{CC2} the shortest pin ensures that all other pins are firmly connected before V_{CC2} receives any voltage. A filtered UVLO circuit on V_{CC2} ensures that the V_{CC2} pin is firmly connected before the PCA9512 connects the backplane to the card.

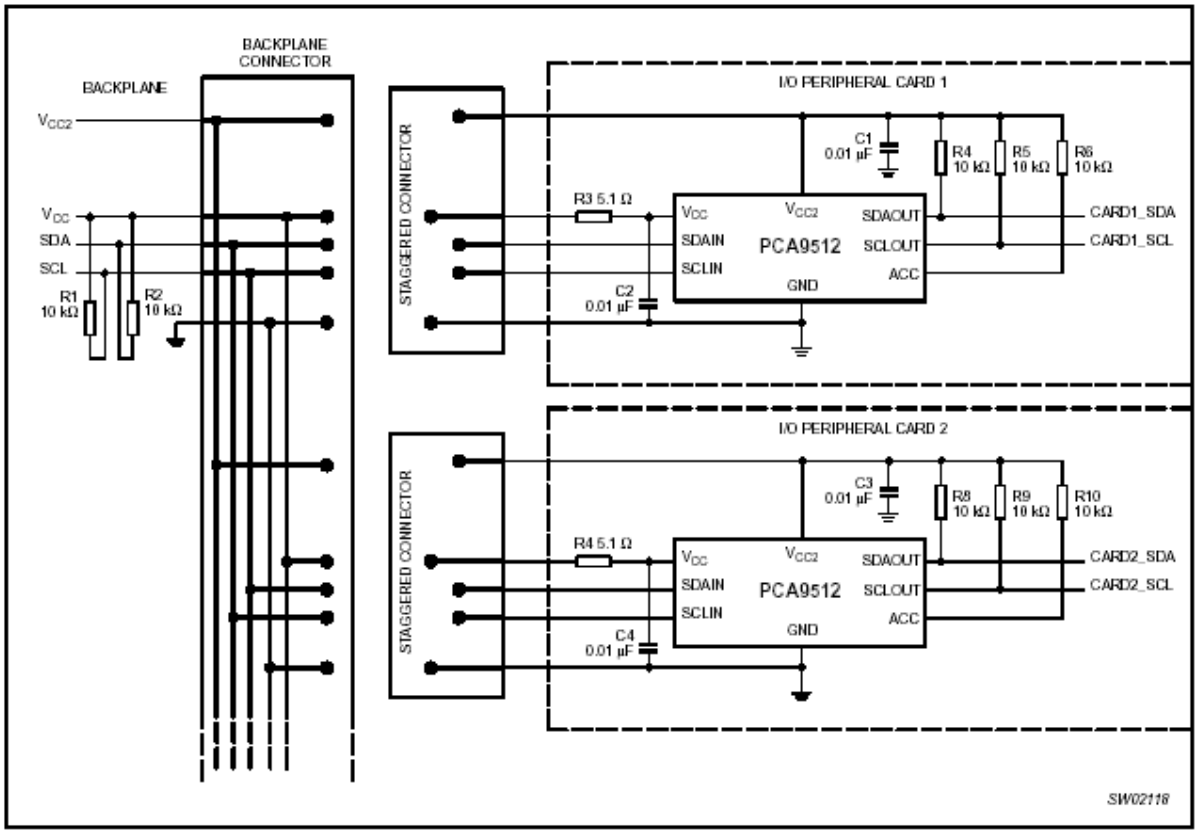

Figure 20. Hot Swapping Multiple I/O Cards into a Backplane Using thePCA9512 with a Custom Connector

Use of the I^2C bus in backplane systems is increasing and either a point to point arrangement with multiple individual buses to each line card from the master or a single multi-point bus to every line card is often used.

IPMI and PICMG Architectures

Intelligent Platform Management Interface (IPMI)

Intelligent Platform Management Interface (IPMI) is an Intel initiative in conjunction with hp, NEC and Dell and consists of three specifications:

- Intelligent Platform Management Interface (IPMI) for software extensions
- Intelligent Platform Management Bus (IPMB) for intra-chassis (inside the box) extensions and uses I^2C/SMBus as the physical means to transfer information across the bus.
- Inter Chassis Management Bus (ICMB) for inter-chassis (outside of the box) extensions and uses various different means like CAN, RS-424 or I^2C to transfer information.

IPMI defines a standardized, abstracted, message-based interface to intelligent platform management hardware and defines standardized records for describing platform management devices and their characteristics. IPMI provides a self monitoring capability increasing reliability of the systems

This new standard was needed since as the complexity of systems increase, MTBF decreases, and there needed to be a way to monitor and control platform components outside of the normal system operation so that failures could be detected and corrected or rerouted.

- IPMI provides a self monitoring capability increasing the reliability of the systems and monitor the server physical health characteristics such as:
  - Temperatures
  - Voltages
  - Fans
  - Chassis intrusion

- IPMI provides General system management such as:
  - Automatic alerting
  - Automatic system shutdown and re-start
  - Remote re-start
  - Power control

More information: www.intel.com/design/servers/ipmi/ipmi.htm

IPMI is a standardized bus and protocol for extending management control, monitoring, and event delivery within the chassis. It is:

- I^2C based
- Multi-master capable
- Simple Request/Response Protocol
- Uses IPMI Command sets
- Supports non-IPMI devices
- Physically I^2C but write only (master capable devices), hot swap not required.
- Enables the Baseboard Management Controller (BMC) to accept IPMI request messages from other management controllers in the system.
- Allows non-intelligent devices as well as management controllers on the bus.
- BMC serves as a controller to give system software access to IPMB

It defines a standardized interface to intelligent platform management

Hardware

- Prediction and early monitoring of hardware failures
- Diagnosis of hardware problems
- Automatic recovery and restoration measures after failure
- Permanent availability management
- Facilitate management and recovery
- Autonomous Management Functions: Monitoring, Event Logging, Platform Inventory, Remote Recovery

Implemented using Autonomous Management Hardware:
Designed for Microcontrollers based implementations
Hardware implementation is isolated from software implementation
New sensors and events can then be added without any software changes

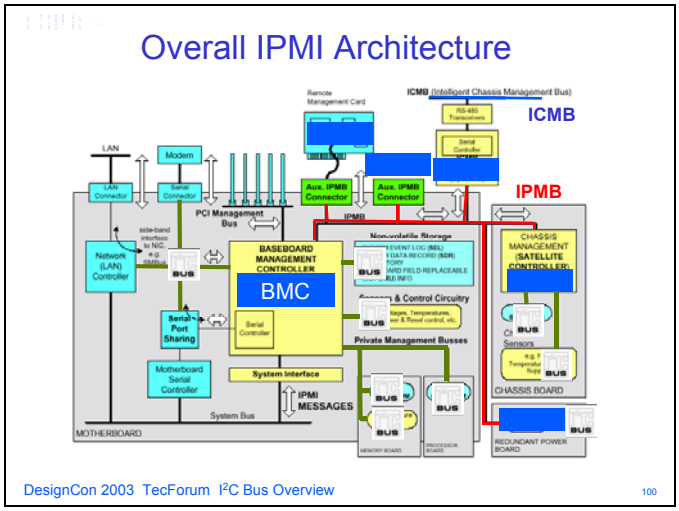

Figure 21. Overall IPMI Architecture

Where IPMI is being used

Intel Server Management

Servers today run mission-critical applications. There is literally no time for downtime. That is why Intel created Intel® Server Management – a set of hardware and software technologies built right into most Intel® sever boards that monitors and diagnoses server health. Intel Server Management helps give you and your customers more server uptime, increased peace of mind, lower support costs, and new revenue opportunities.

More information: http://program.intel.com/shared/products/servers/boards/server_management

PICMG

PICMG (PCI Industrial Computer Manufacturers Group) is a consortium of over 600 companies who collaboratively develop open specifications for high performance telecommunications and industrial computing applications. PICMG specifications include CompactPCI® for Eurocard, rack mount applications and PCI/ISA for passive backplane, standard format cards. Recently, PICMG announced it was beginning development of a new series of specifications, called AdvancedTCA™, for next-generation telecommunications equipment, with a new form factor and based on switched fabric architectures. More information can be found at: http://www.picmg.org

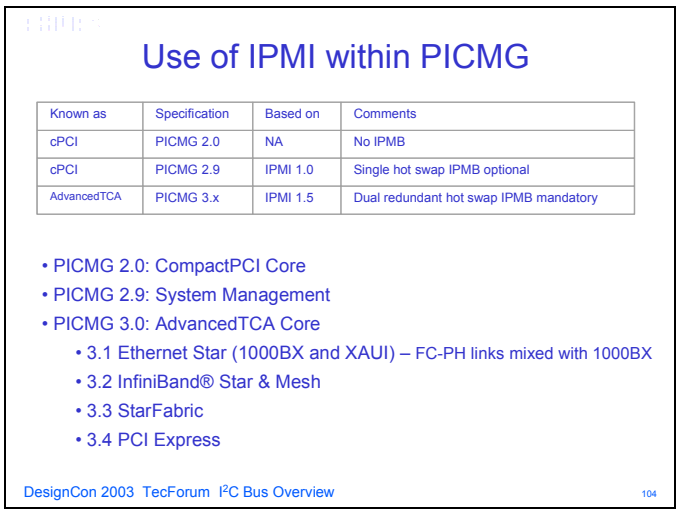

Figure 22. Use of IPMI within PICMG

IPMI with additional extension is used as the basis for PICMG 2.9 and PICMG 3.x.

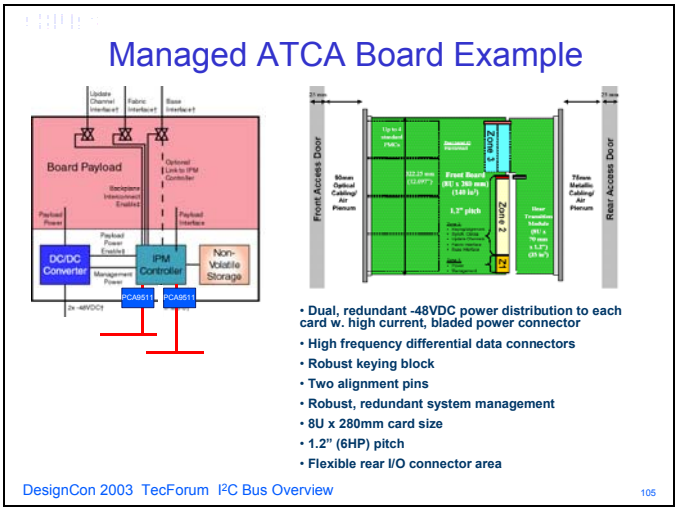

Figure 23. Managed ATCA Board Example

Figure 23 shows how IPMI is used within an AdvancedTCA card.

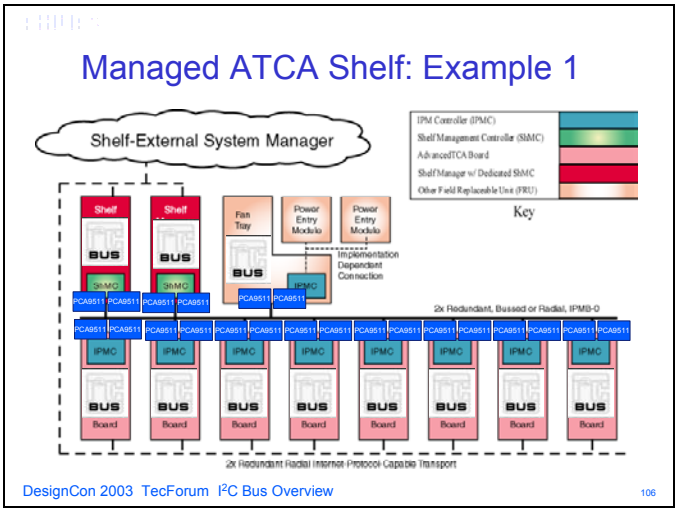

Figure 24. Managed ATACA Shelf: Example 1

Figure 24 shows one of the two redundant buses that would interface through the PCA9511 or PCA9512/13/14.

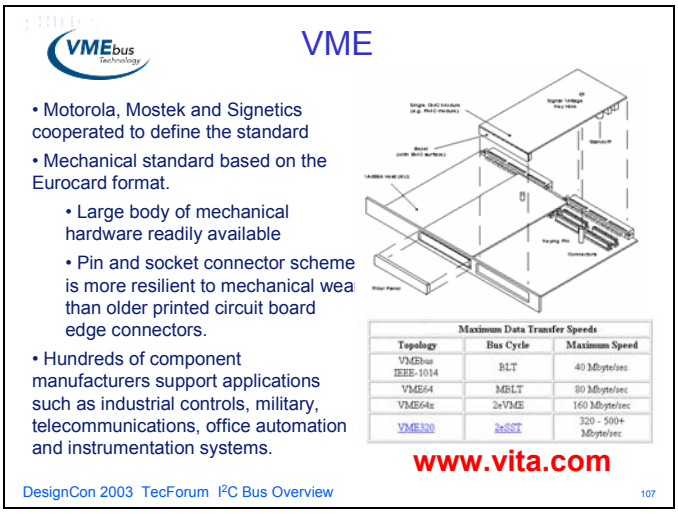

Figure 25. VME

VMEbus

VMEbus is a computer architecture. The term 'VME' stands for VERSAmodule Eurocard and was first coined in 1980 by the group of manufacturers who defined it. This group was composed of people from Motorola, Mostek and Signetics corporations who were cooperating to define the standard. The term 'bus' is a generic term describing a computer data path, hence the name VMEbus. Actually, the origin of the term 'VME' has never been formally defined. Other widely used definitions are VERSAbus-E, VERSAmodule Europe and VERSAmodule European. However, the term 'Eurocard' tends to fit better, as VMEbus was originally a combination of the VERSAbus electrical standard, and the Eurocard mechanical form factor.

VERSAbus was first defined by Motorola Corporation in 1979 for its 68000 microprocessor. Initially, it competed with other buses such as Multibus™, STD Bus, S-100 and Q-bus. However, it is rarely used anymore. The microcomputer bus industry began with the advent of the microprocessor, and in 1980 many buses were showing their age. Most worked well with only one or two types of microprocessors, had a small addressing range and were rather slow. The VMEbus architects were charged with defining a new bus that would be microprocessor independent, easily upgraded from 16 to 32-bit data paths, implement a reliable mechanical standard and allow independent vendors to build compatible products. No proprietary rights were assigned to the new bus, which helped stimulate third party product development. Anyone can make VMEbus products without any royalty fees or licenses. Since much work was already done on VERSAbus it was used as a framework for the new standard.

In addition, a mechanical standard based on the Eurocard format was chosen. Eurocard is a term that loosely describes a family of products based around the DIN 41612 and IEC 603-2 connector standards, the IEEE 1101 PC board standards and the DIN 41494 and IEC 297-3 rack standards. When VMEbus was first developed, the Eurocard format had been well established in Europe for several years. A large body of mechanical hardware such as card cages, connectors and sub-racks were readily available. The pin and socket connector scheme is more resilient to mechanical wear than older printed circuit board edge connectors.

The marriage of the VERSAbus electrical specification and the Eurocard format resulted in VMEbus Revision A. It was released in 1981. The VMEbus specification has since been refined through revisions B, C, C.1, IEC 821, IEEE 1014-1987 and ANSI/VITA 1-1994. The ANSI, VITA, IEC and IEEE standards are important because they make VMEbus a publicly defined specification. Since no proprietary rights are assigned to it, vendors and users need not worry that their products will become obsolete at the whim of any single manufacturer. Since its introduction, VMEbus has generated thousands of products and attracted hundreds of manufacturers of boards, mechanical hardware, software and bus interface chips. It continues to grow and support diverse applications such as industrial controls, military, telecommunications, office automation and instrumentation systems.

Use of IPMI in VME Architecture

New VME draft standard indirectly calls for IPMI over I^2C for the system management protocol since there was nothing to be gained by reinventing a different form of system management for VME. The only change from the PICMG 2.9 system management specification is to redefine the backplane pins used for the I^2C bus and to redefine the capacitance that a VME board can present on the I^2C bus. The pin change was required because the VME backplane connectors are different from cPCI. The capacitance change was required because cPCI can have a maximum of 8 slots and VME can have a maximum of 21 slots. System Management for VME Draft Standard VITA 38 – 200x Draft 0.5 9 May 02 draft at: http://www.vita.com/vso/draftstd/vita38.d0.5.pdf provides more information.

I^2C Bus Extension Over Long Cables

Users who wish to connect two 2-wire systems separated by a distance can do so by connecting two PCA9511/12/14s back-to-back, as shown in Figure 26. The I^2C specification allows for 400 pF maximum bus capacitance, severely limiting the length of the bus. The SMBus specification places no restriction on bus capacitance, but the limited impedances of devices connected to the bus require systems to remain small if rise- and fall-time specifications are to be met. The strong pull-up and pull-down impedances of the PCA9511/12/14 are capable of meeting rise and fall-time specifications for one nanofarad of capacitance, thus allowing much more interconnect distance. In this situation, the differential ground voltage between the two systems may limit the allowed distance, because a valid logic low voltage with respect to the ground at one end of the system may violate the allowed V_{OL} specification with respect to the ground at the other end. In addition, the connection circuitry offset voltages of the back-to-back PCA9511/12/14s add together, directly contributing to the same problem. See Application Note AN255 Repeaters, Hubs and Extenders for more information on the P82B96 and P82B715 that are optimally designed for this type of application.

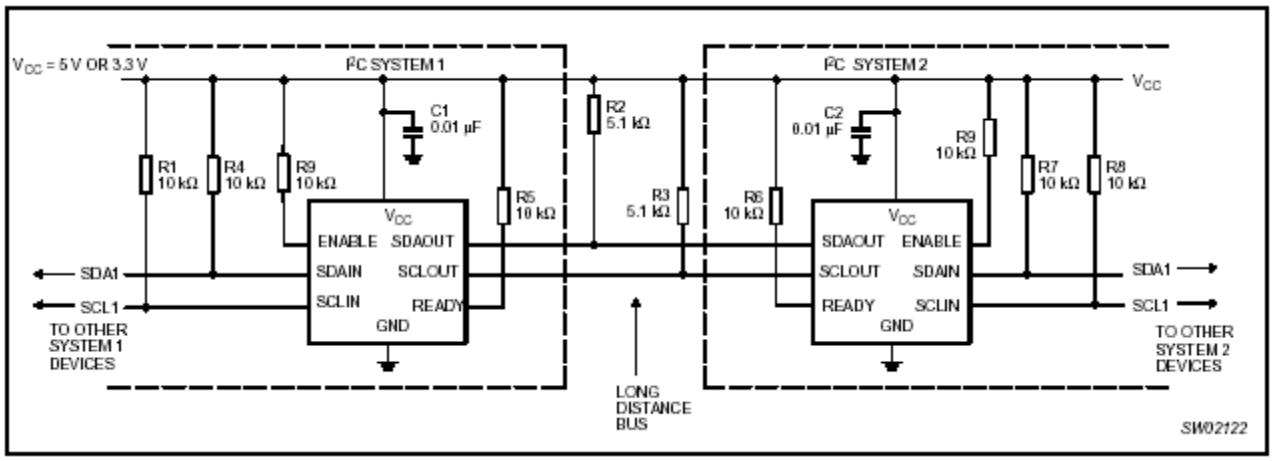

Figure 26. Repeater/Bus Extender Application

FREQUENTLY ASKED QUESTIONS

1. **Question:** Does the PCA9511 hot swappable 2-wire bus buffer need to be put on both the backplane and the I/O card to allow hot swapping?
   Answer: No, only one device is necessary. The device should be placed on the card itself next to the connector. When the card is connected to the I^2C backplane bus, the PCA9511 will first check the bus activity and then when an idle condition is detected, it will connect the I^2C -backplane to the I^2C-card. It also precharges the SDA and SCL pins to 1V to avoid voltage spikes due to the uncharged pin capacitance that prevents glitching the I^2C data and clock lines.

2. **Question:** We are passing signals from a PCA9515 through the PCA9544. On the I^2C bus lines, we are using a 1.3 kΩ pull-up resistor to 3.3 V on the PCA9515 side of the pass transistor and a 20 kΩ pull up resistor to 3.3 V on the other. We see a PCA9515 Vol = 0.5 V to 0.6 V and on the other side of the pass transistor a signal level of 0.7 V to 0.8 V. This makes the combination unsuitable for use with a Linear Tech ® LTC4300-1 (which has a max Vil spec. of 0.6 V and which is used on the other side of the pass transistor). Does Philips have a plot of Vol vs Iol for the PCA9515 - if we're at 0.6 V @ 2.7 mA, we will be out of datasheet specification at 6 mA? Using the 20 kΩ ohm resistors we appear to be limiting the amount of current through the pass transistor in order to reduce the drop across it. From our calculations we have about 165 µA of pull-up current through the pass transistor. To get a 200 mV delta Ron is quite considerable. Do we see any Ron dependency with through current?
   Answer: You are suffering from one of the unintended outcomes of using the LTC4300-1 part.

   1st - The PCA9515 uses an output driver that is essentially a voltage source that only sinks current and its level is set at 0.52 V. Thus, from zero to more than 10 mA the output voltage only changes by a few millivolts. Even with variations over process, temperature, and power supply the voltage is within a few tens of millivolts of 0.52 V. The output voltage at even 10 mA is less than 0.6 V.

   2nd -The maximum R-on for the PCA9544 is 55 Ω. Assuming 135 µA from the 20 KΩ resistor, the voltage drop across the PCA9544 should be less than 0.01 V. Even at 55 Ω R-on, which is the maximum limit, to get a 0.2 V drop across the PCA9544 would require 3.6 mA.

Therefore, the LTC4300-1 is the most likely source of the extra current. I believe a check of the system with the LTC4300-1 removed will confirm that the voltage driven at the output of the PCA9544 is less than 0.6 V. The problem is that the "pull-up" current one-shot in the LTC4300-1 is being triggered by noise and is contending with the low level driven by the PCA9515. The pull-up current source in the LTC4300-1 speeds the low to high transition by increasing the total pull-up current and is switched off when the pin is high so as not to contend on the next high to low transition. If the current source of the LTC4300-1 gets turned on when the PCA9515 is driving a low, it will remain on because the pin does not go high. The current supplied by the current source will be high enough to pull the voltage up to 0.7 V - 0.8 V.

Note: The LTC4300-1 is 100% equivalent to the PCA9511. The PCA9513/14 are footprint identical to the PCA9511 with some modifications, one of which is that the rise time accelerator threshold has been moved up to 0.8 V from 0.6 V to provide more noise margin. The LTC4300-2 is 100% equivalent to the PCA9512 and has a disable pin for the rise time accelerators.

3. **Question:** One of the channels of the PCA9544 Multiplexer is connected to the card that will be hot swapped. In this case, does the PCA9511 also need to be used to prevent glitching the bus data?
   Answer: Let's presume that the PCA9544 or any other of the other devices in the PCA954X Mux/switch family is located on the backplane or controller card and the individual downstream channels are connected to one or several slave cards.
   - The PCA9511 is not needed if the slave card is inserted prior to activating that channel since the bus is dead and the system capacitance is < 400 pF.

   The PCA9511 should be used if the channel is active prior to inserting the card since the PCA9511 will not connect the card until the bus is idle and the precharge feature will prevent glitching data to other I^2C slave card that may already be inserted into that sub bus. It should also be used if system capacitance is > 400 pF.

4. **Question:** I was wondering how similar the PCA9511 is to the LTC4300-1I. The problem we had with the LTC4300-1I was that it had a very weird waveform. It would slowly rise up to 1 V, and then accelerate up to 3.3 V. This slow rise to 1 V caused us to fail rise time specs. A picture of this is included below and is also in the LTC4300-1I datasheet. Does this new Philips part also have this characteristic as well?
   Answer: Answer in progress, to be checked during characterization.

5. **Question:** General application is where we plug in multiple modules into a backplane. So there is a master I^2C module that communicates with up to six slave I^2C modules across a backplane. So the I^2C tracks branch off to each module, and the longest track could be up to 12 - 16 inches (3 pf per inch). Each module has this LTC4300-1 buffer to the backplane. We want to isolate the capacitance of the tracks. The buffer is placed on the slave modules and uses a 4.75 K pull-up. The pictures I sent you are the waveform at one of the modules using a 4.7 5K pull-up and the LTC4300-1 part. Increasing the pull-up does improve the rise time, but the slow rise to 1V does not improve at all.
   Answer: I think it has many conditions that need to be met before it will behave as system designer's hope/expect that it will. Have a look at figure 3 on page 10 in the data sheet of the combined LTC4300-1/LTC4300-2 and the paragraph immediately above that figure. They seem to say to me that there is only a very narrow range of acceptable rise times. This requirement sets limits on minimum bus capacitance, and the I^2C rise time limits the maximum bus capacitance, for a given pull-up. This applies to both sides of the chip. So for your 4k75 there seems to be a minimum capacitance requirement of over 100pF, even on the side connected to the slave chips. Maybe you do not have that much on each slave card? Its data does not say HOW it might deviate from "functioning properly" if you do not meet this requirement.

   There are conditions necessary to activate the strong pull-up in these devices. a) a slew rate FASTER than about 1.25V/us PLUS b) a rise to a dc LEVEL of at least one Vbe junction voltage (about 0.6-0.7V).

   While several customers have found it ideal in applications even with relatively short wiring and lower capacitance it might be slightly 'overkill' for your application, at least as I understand it from the description so far. The P82B96 totally isolates the chips on each card from the capacitance on the backplane. It can cope with a backplane capacitance of at least 4 nF. The chips on each card see only a few pF of P82B86 input capacitance. You are free to choose any pull-ups on each card or the backplane. They do not interact. It has x10 drive capability on the Tx/Rx side (used for driving the backplane) so pull-ups could be down at 100 ohms - but you do not need to go that far.

If you want to try it, connect its Sx/Sy inputs to the chips on each card. Select a pull-up to give the necessary rise time with the capacitance of the connected chips and tracks. Your 4k75 should be fine unless you have lots of I^2C chips on each board. You need to select a pull-up for the backplane to keep the rise time fast. From your figures you have 6 tracks at maybe average 12 inches each (36 pF) for a total of 216 pF. Pull-ups of, say, 470 ohms should be fine.

If you want to run all your system at 3.3V then all pull-ups and the P82B96 simply connect to that 3.3V supply. If, for noise immunity, you wanted to run the backplane at a higher logic voltage then you simply connect the supplies of all P82B96 and the backplane pull-up to that higher voltage - to 5 V, 12 V, or whatever is convenient. The Sx/Sy pins just keep their pull-ups to the 3.3 V logic supply and the bus on each board runs at 3.3 V. Even there you have free choice of logic voltage on each card so 3 V, 5 V or whatever suits.

In common with all true I^2C buffer devices there has to be SOMETHING to prevent the whole system latching or oscillating. P82B96 works its magic by using an extra dc logic voltage level, so you will notice unusual logic low levels within each card. There will be small steps in the waveforms, but nothing that isn't compatible with normal I^2C bus logic voltage levels. The step is located below 0.9V, so below the lower reference threshold (0.3Vcc) that is used to specify bus rise times so it won't count. The logic levels used on the backplane are perfectly standard, nothing unusual there.

You can use a similar argument to discount the slowly rising section in your present bus waveforms. So I would say your waveforms actually look OK, no reason for concern. The real logic threshold at half supply (about 1.6V) is crossed quickly and that's one key reason we specify a maximum rise time.

For both solutions (P82B96/LTC4300-1) you must count any delays of the signal as components of the total signal propagation delay. There are no published limits in I^2C specifications for propagation delays, but they are implied in the other timings.

Given your waveforms, I doubt P82B96 will actually improve either the delays or the rise times - at the point you measured. All I could claim in its favor is that you won't encounter any system instabilities as are sometimes reported when using rise time accelerators. You can also cope with much larger backplane capacitance, if required for system expansion, and ESD protection can be easier because its I/Os are rated to 18 V.

6. **Question:** What are some types of system instabilities that are encountered with rise time accelerators found in the PCA9511/12/13/14? Also, is it possible for a rise time accelerator to hold a line low indefinitely for some reason or another?
Answer: There are two different types of rise time accelerators, the type used in the PCA9511/12/13/14 and LTC4300 that we were discussing - and Linear Tech's basic accelerators like the LTC1694i. The simple accelerators in the PCA9511/12/13/14 have no pull-down capability so certainly should never hold any bus low. When a part "requires a minimum capacitance in order to function properly" then that says to me the design is probably only conditionally stable. By contrast, P82B96 is unconditionally stable for all combinations of loadings that we could imagine during its design simulations. There is no bus loading conditions to be met for system stability. We suspect the accelerators (being designed to trigger on dV/dt) can also be triggered by noise if the bus lines are not held very close to 0V. We have seen problems when they are interfaced with buffers like PCA9515 that use 0.5-0.6V logic low levels. PCA9515 has more sink capability than the pull-up sources in the accelerators. If the accelerators turn on due to noise while the bus is being driven low (0.6V) by PCA9515 that causes large power supply currents. A P82B96 alternative would make your waveforms "different" but not necessarily "better".

ADDITIONAL INFORMATION

The latest datasheets and IBIS models for the I^2C Hot Swap family of products and other I^2C and SMBus products can be found at the Philips Semiconductors website http://www.semiconductors.philips.com/i2c or the Philips Semiconductors Logic Products Group website at http://www.philipslogic.com/i2c.

Only the Logic Product Groups website will include data sheets and IBIS models for new unreleased sampling I^2C devices.

Software tools for most of Philips' I^2C products can be found at: http://www.demoboard.com

Additionnal technical support for the I^2C and SMBus Repeater/Hub/Expander family of products and other I^2C and SMBus products can be requested by e-mailing the question to: pc.mb.svl@philips.com

See AN460 for further application information about P82B96
See AN255 for further application information about all Philips I^2C bus buffers
See AN462 for further application information about PCA954x Multiplexers/Switches
See AN10145 for further application information about GTL2000/02/10 Bi-Directional Low Voltage Translators

Reference: Linear Technology LTC4300-1/LTC4300-2 Hot Swappable 2-wire Bus buffer data sheet 430012f

APPENDIX 1 – LTC4300-1 and PCA9511 Characterization Data Comparison

Characterization data comparison to be added in 3Q 2003

Review of LTC4300-1 Behavior

The "Normal" behavior of the LTC4300-1 seams reasonable and consistent with the data sheet description. For large swings i.e. Vih near V_{CC} to Vil <= 0.5 v the output is well behaved as shown in Figure 27.

(Figure to be inserted later)

Figure 27

In spite of the 6 ns signal generator edge, the output falls quickly to about 0.1 V above the input low level with only a small bounce. The 6 ns rising edge of the signal generator is essentially instantaneous as far as the part is concerned. A series 50 Ω resistor between the input and the terminated signal generator driver allows the input pull down and input pull up currents to be measured. As the input swing high, it overshoots the ~0.2 V above Vil level that the input side driver wants to regulate, within ~ 20 ns the driver is on fighting the signal generator driven level. At the same time the output starts to rise pulled up by an external resistor, this in turn raises the level that the input side driver is trying to drive. At some point the input has risen above the input trip level, which appears to be ~ 0.6 V, and the rising edge rate detector has tripped. The rising edge accelerator current source then fires and the input rises rapidly to within ~0.8 V of V_{CC}. If Vih is less than V_{CC} the current level of the current source can be measured as well as its duration. After the output has risen enough that both the level of ~0.6 V and the edge rate have been satisfied the pull up current source fires. It appears that the pull down driver is shut off when the pull up current source fires. All four I/O pins show the same behavior that is SCLin to SCLout in either direction as well as SDAin to SDAout in either direction.

Expected Behavior

Since the propagation in the data sheet appears to be measured at 1.5 V for a 3.3 V V_{CC} (a level that is between the 0.3 V_{CC} max V_{IL} and the 0.7 V_{CC} min Vih of the I^2C specification) it is reasonable that the output pull down would be turned on if the input falls below 0.7 V_{CC}. The pull down is an offset amplifier referencing the other side and adding ~ 0.1 V, so if the input were at 1.5 V the output would be 1.6 V.

Because the current source pull ups fire on a rising edge if the edge rate is sufficient and the level is above ~0.6 V it is reasonable to turn the pull down off when the pull up fires. The effect of the current source pull up is to pull the pin up to nearly V_{CC}, however if the input only goes part of the way high and the output pull down were enabled at the end of the pull up cycle the output would show a glitch by falling back to just above the input level. The pull down is therefore latched off once the pull up current source fires and is not turned back on until the input falls again.

The precharge and Icc were not checked, but it seams reasonable to turn on the precharge when the power up reset cell engages at ~0.8 V and turn the precharge off when the power up reset shuts off before V_{CC} = 2.5 V.

Anomalous Behaviors

The LTC4300-1 shows several unusual behaviors that were not copied.

Input transitions which start at or near V_{CC} and only go part of the way down i.e. with V_{CC} = 3.3 V , Vih = 3.3 V, and Vil = 1.91 V , the output just starts to drop then remains at a nearly constant at V_{CC} - 0.1 V until the input rises. See Figure 28. When the Vil ~1.2 V the output swings look normal.

(Figure to be inserted later)

Figure 28

There is a drop-out behavior where the output gets stuck high as shown in Figure 29 and Figure 30. The input levels depend on V_{CC}. At V_{CC} = 2.7 V the drop-out starts if Vih <= 1.03 V and Vil >= 0.5 V , once the output is high it will not start again until Vih >1.5 V or Vil < 0.5 V. At V_{CC} = 5.5 V the drop-out expands to Vih <= 1.5 V and Vil >= 0.6 V, and remains high until Vih > 3.5 V or Vil < 0.49 V.

(Figure to be inserted later)

Figure 29

(Figure to be inserted later)

Figure 30

A slow rise is observed at V_{CC} = 5.5 V when Vih is near V_{CC} and Vil ~ 0.7 V . The output swings up like normal then at ~3.5 V turns around and drops back to ~2 V then rises slowly with the output below the input and both pull downs on. The rise takes more than 1000 ns from ~2 V to ~4 V then the rise speeds up above ~4 V. From other observations of the pull up current source it is most likely on during the entire time and the pull down must also be on and with the output offset below the input rather than above it.

Another strange result occurred at V_{CC} = 5.5 V, Vih = 5.0 V, and Vil = 0.65 V where the output only glitches low rather than following the input as shown in Figure 31. The output falling edge looks normal for the first 200 ns then it slowly rises, eventually the pull up current source fires and the output returns high with the input at 0.65 V.

(Figure to be inserted later)

Figure 31

Proposal for PCA9511/12/13/14 Devices

Each pin will have a precharge resistor and enable transistor, a pull up current source, a rising edge detector, a falling edge detector a 0.7 V_{CC} level detector, a 0.6 V level detector, a 0.25 V level detector, a 0.5 V_{CC} level detector, a latch or flip flop to store the active or inactive condition of the pull down, the offset amplifier / pull driver, and the necessary logic. The power up reset cell, precharge voltage source, enable cell, ready output, voltage reference , current reference, and bus idle detect logic are all shared circuitry.

Expected Operation

Input changes between 0.7 V_{CC} and V_{CC} will not affect the output. If the input swings below 0.7 V_{CC} with sufficient amplitude change and edge rate, the output pull down will turn on and the output will fallow the input with a ~0.1 V offset. If the input rises with an amplitude and edge rate sufficient to trip the rising edge detector and the Vih is > 0.6 V then the pull up current source will fire and the pull down will be disabled. Any transitions that will cause the input pull up current to fire will also cause the output current source to fire. The input swing may be limited but the output will swing all the way high if the pull up current source fires unless prevented by external means. Small input changes for input voltages below 0.6 V and above 0.3 V will be reflected in the output. If the input goes below ~0.25 V the output will lock at ~0.3 V until the input returns above ~0.25 V.

APPENDIX 2 – LTC4300-2 and PCA9512 Characterization Data Comparison

To be completed in 4Q 2003