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Input signal definitions for the 3.5" TFTs TX09D CCA & CDA versions (with Tcon controller)

Introduction

For the Hitachi 3.5" TFTs with timing controller (Tcon) on board (CCA & CDA) , the electrical input requirements can be split into the 3 areas described below:

1) Power supply: V_{DD} (3.3V) and V_{ss} (Ground).

   The typical power consumption including LED backlight of the product is about 660mW.

2) Timing controller: DCLK, Hsync, DTMG, PCI and RGB data bus.
   DTMG signal can be derived from the Hsync and Vsync signals generated by the display controller in accordance with the timing chart in the CAS. For the TX09 Vsync is not required and is replaced by DTMG.

3) LED backlight voltage: V*ctrl* (LED current control pin).

   The Vctrl input is used to accurately control the LED current via a LED control IC. The input signal can be either DC or PWM (Pulse Width Modulation) for dimming control.
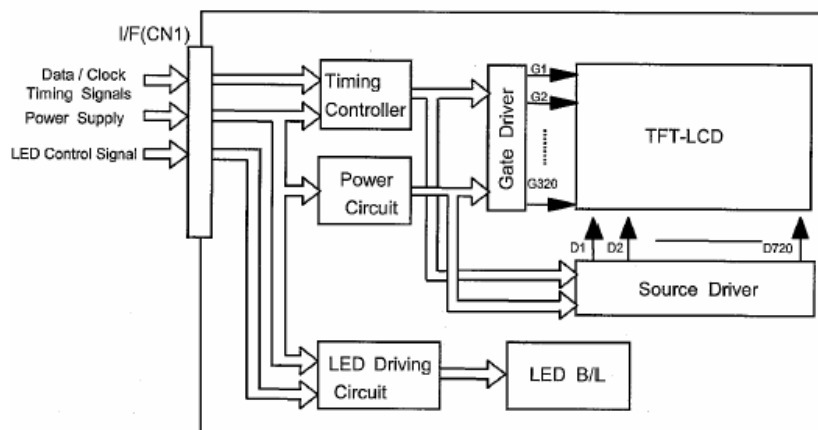
Figure 1: The block diagram of TX09D with Tcon series of products.

All input signals have to be generated by customers system and must meet the parameters defined in the Hitachi CAS (Customer Acceptable Specification).

All essential information has been defined in the CAS. In this application note the signals DTMG. Vsync , Hsync, Vctrl and PCI will be discussed in detail.

Note: Hitachi recommends the use of bypass capacitors to reduce any spikes in the mother board design for the worst application environments.

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1 What is DTMG?

Most graphic controllers on the market provide the Hsync and Vsync signals necessary to drive most TFT display.

H*sync* (Horizontal Synchronization): This signal marks the point at which the current line of data ends, and the next line begins. There are N number of DCLK periods per H*sync* period where N is the number of RGB pixels in a line.

V*sync* (Vertical Synchronization): This signal marks the point at which the current frame ends, and the new frame begins. There are M number of Hsync periods per V*sync* period where M is the number of vertical lines in the display.

For all of Hitachi's TFT displays with Tcon the input signals DCLK & DTMG are used, by the timing controller IC, to generate the signals required by the row and column drivers. DTMG is a valid data signal.

If the DTMG signal is not available as a dedicated output pin of your graphics controller it can be derived from V*sync* and *Hsync*. This signal contains all the information the Tcon IC requires to determine both vertical and horizontal delay periods (these delays are known as front and back porches).

For the TX09 range of displays both DTMG and H*sync* signals are necessary for the Tcon to operate correctly. V*sync* is not a required input signal but is included in the CAS as it's timing characteristics are necessary to ensure the correct DTMG signal is generated.

1.1 DTMG & Hsync relationship

For every Hsync pulse there is a DTMG pulse the position of which is determined by the horizontal front and back porch settings (HBP & HFP). The HBP specifies the number of clock periods between the end of the H*sync* pulse and the beginning of valid data and the HFP is the number of clock periods between the end of valid data and the beginning of the H*sync* pulse.
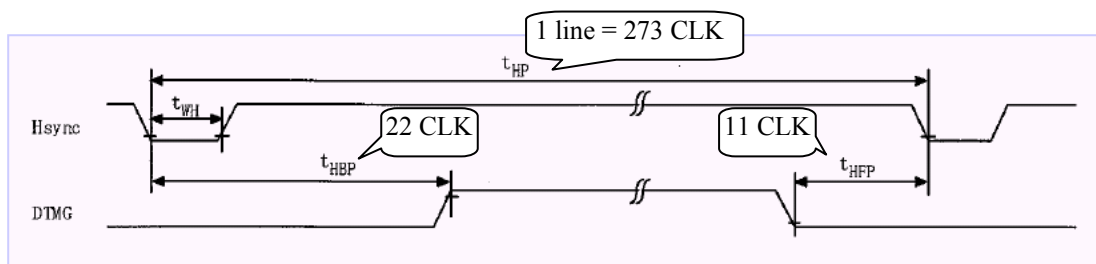

Figure 2: DTMG setting related to Hsync.

1.2 DTMG & Vsync relationship

The vertical timing part of the DTMG signal is the inactive part between the horizontal pulses defined by the vertical front and back porches. The VBP is the number of inactive lines at the start of a frame and the VFP is the number of inactive lines at the end of a frame.
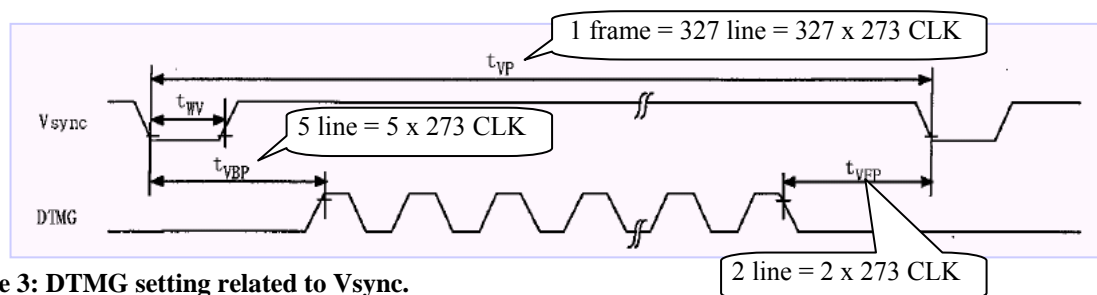

Figure 3: DTMG setting related to Vsync.

2 PCI function of Tcon board

So far, Hitachi has developed two version of the Tcon PCB for the TX09 range of displays. Each version was the same in all respects other than the Tcon IC used:

1) Epson timing controller,

2) Hitachi timing controller.

The Hitachi Tcon IC matches the Epson timing controller functionality in every aspect other than the PCI function.

For the Epson timing controller, the PCI function is used to enable / disable the signals of data bus.

• Pulled high (3.3V):

  The Tcon ICs data bus output is enabled and an image can be shown on the display.

• Pulled low (GND):

  The Tcon ICs data bus output is disabled and the display will not show any image even if the data continues to be sent to the Tcon. Under this condition, the LED backlight is still working independently and the power consumption will be the same as PCI pulled high.

For the Epson version of the Tcon PCB the On/Off sequence of for the PCI pin was defined in the CAS as Figure 3 shows. This timing was recommended to prevent spurious data appearing on the display.
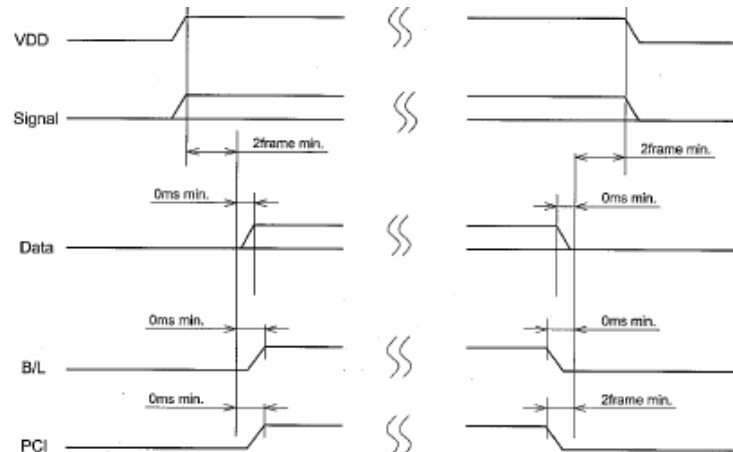
Figure 4: Power sequence of the TX09D.

For the Hitachi Tcon IC the PCI pin has no fucntion. Therefore, the input voltage level for the PCI pin is not critical and can be either high or low, there will be no effect on the displayed image. PCI was kept in order to provide backward compatibility and still appears in the CAS power On/Off sequence and pinout table.

3 LED backlight control by Vctrl

LEDs are variable current devices and as such require a constant current to be supplied to operate to the specified brightness. The LED current on the TX09 Tcon PCB is controlled using a Linear Technologies LED control IC. The LEDs are connected in series. A constant 20mA current output can be maintained using a 10Ω feedback resister. The equation is:

$$I_{LED} = V_{FB} / R_{FB}.$$

Where ILED = 20mA VFB = 200mV.

The feedback reference voltage can be adjusted using Vctrl. Figure 5 shows the feedback voltage generated at various Vctrl input voltages. VFB is maximum (200mV) when V*ctrl* is 1.8v or higher this results in a full LED current of 20mA and maximum brightness. Although maximum brightness can be achieved at 1.8v the maximum Vctrl input voltage is 10v.
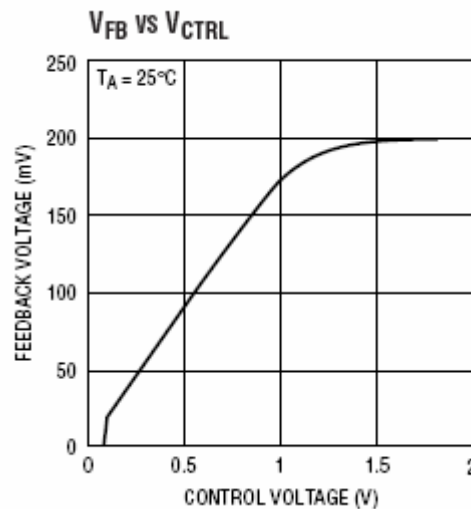
Figure 5: The curve of VFB and Vctrl.

The V*ctrl* pin can be used as a DC dimming control when it's input voltage is adjusted between 200mV & 1.5V see Figure 5.

For digital brightness control a PWM signal can be used on the Vctrl input. Average LED current increases proportionally with the duty cycle of the PWM signal. The recommend frequency should be between 1 KHz to 10 KHz for the PWM signal.

In order to reduce signal spikes the addition of a low pass filter should be considered on the system board before inputting the PWM signal to V*ctrl* pin. Furthermore, the frequency of low pass filter should be lower than the frequency of the PWM signal.

Note: For more LED information, please refer to AN-012.

4 Cautions

Keep safety first in your circuit designs!
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