1.3 General Specifications

Item	Specification	Unit				
Screen size (diagonal)	10.3	inch				
Aspect ratio	12:9	-				
Display resolution	1280RGBx480	-				
Pixel Arrangement	RGB – stripe	_				
	0.0635(x3) x 0.1905 (square pixels)					
LCD technology	Active matrix TFT	-				
Image mode	Normally Black	-				
Display type / technology	Transmissive IPS	-				
Brightness	1233	Cd/m ²				
Display colors	262K (6 bits) / 16.2M (8 bits)	-				
Backlight	White LED	-				
Module type	LCD, backlight, TP	-				
Operating Temperature	-30to +85 (surface temperature)	က				
Operating reinperature	-40'C with limited performance					
	Electronics and interface					
Panel interface	RSDS					
LCD Power consumption	1000	mW				
LED BL Power consumption	10.24(20 pcs LED)	W				
Total Power consumption	11.24(LCD driving + LED)	W				
	Basic display features					
Preferred viewing direction	Horizontal axis	-				
Surface treatment	Hard Coating (3H), AG	-				
Visibility with polarised sunglass	OK	-				
Mechanical dimensions						
Active area (LCD)	243.84x 91.44	mm ²				
Outline dimension	Max.262x108.5	mm ²				
Thickness	Max.15.0	mm				
Weight	470	g				

3 Input / output pinning and connector description

3.1 LC-module without power board on FPC

	Input signal name RSDS	I/Opin (I:input, O:output, P:power)	Ту	ypical voltage (Volt)		description		
				and the second				
1	VCC1	Р		3.0	power supply	External main and I/O power supply		
2	VSS	Р		0.00	Digital ground	External main and I/O power supply		
3	VDDN	Р		-6.60	power supply	External power supply for source driver		
4	VSSA	P		0.00	analog ground	Analog circuit ground		
5	VDDP	P		6.60	power supply	External power supply for source driver		
6	RSDS B0/B1 +	OPEN		-		,		
7	RSDS B0/B1 -	OPEN						
8	RSDS B2/B3 +	- 1						
9	RSDS B2/B3 -	Î						
10	RSDS B4/B5 +	1						
11	RSDS B4/B5 -	1						
12	RSDS B6/B7 +	1						
13	RSDS B6/B7 -	1						
14	RSDS G0/G1 +	OPEN						
15	RSDS G0/G1 -	OPEN						
16	RSDS G2/G3 +	I						
17	RSDS G2/G3 -	i		6 bit mode is sele	cted for this module.	Pin 6 ,7,14,15,22,23 should be open.		
18	RSDS G4/G5 +	1						
19	RSDS G4/G5 -	T						
20	RSDS G6/G7 +	L						
21	RSDS G6/G7 -	- 1						
22	RSDS R0/R1 +	OPEN						
23	RSDS R0/R1 -	OPEN						
24	RSDS R2/R3 +	1						
25	RSDS R2/R3 -	1						
26	RSDS R4/R5 +	1						
27	RSDS R4/R5 -	1						
28	RSDS R6/R7 +		9					
29	RSDS R6/R7 -	T						
30	VSS	Р		Digital ground	Digital ground	Logic circuit and I/O ground (0V)		
31	CLKP	I		pixel clock	pixel clock	Pixel clock signal		
32	CLKN	L		pixel clock	pixel clock	, stored organization		
33	vss	Р		Digital ground	Digital ground	Logic circuit and I/O ground (0V)		
34	HS	T.				Line synchronous signal (HS) for SYNC mode, or start pulse (DIO) for dumb source mode.		
35	vs	Ë	Synchronous signal Synchronous signal Synchronous signal (VS) for SYNC mode, or polarity (POL) for dumb source mode.					
36	DE	L				Data enable signal (DE) for DE mode, or latch (LD) for dumb source mode.		
37	BIST	OPEN	Н	3.0	For internal test	This pin is not in use since this function is controlled by software setting for this module.		
			L	0.00				
38	page 300 (862)	(5)	Н	3.0	10000 100000	Reset pin		
36	RESET	I i	L	500-114 (1979)	Reset pin	RESETB=0: reset		
				0.00		RESETB=1: normal operation		

		1	_		Υ	EEDEN OUTUBE (4-5W)		
			80			EEPEN=0: disable (default) EEPEN=1: enable		
			L			Set Low to disable this function for this		
				0.00		module		
			Н	3.0		Enable chip ID identification in SPI.		
40				0.0	-	See "SPI interface".		
40	SIDEN	1	12		chip ID identification	SIDEN=0: disable SIDEN=1: enable (default)		
			L			Set Low to disable this function for this		
			9 4	0.00		module		
41		ODEN	Н	3.0		This pin is not in use since this function is		
MATERIAL PA	U/D	OPEN	L	0.00	For internal test only	controlled by software setting for this module.		
-		1		0.00		This pin is not in use since this function is		
42	R/L	OPEN	н	3.0	For internal test only	controlled by software setting for this module.		
			L	0.00				
43			Н	3.0	FED 1000 1900 10 10	This pin is not in use since this function is		
	DINT	OPEN	L	0.00	For internal test only	controlled by software setting for this module		
44	ESDAI	OPEN	97(88	0.00				
45	ESDAO	OPEN						
46	ESCL	OPEN	1			101 NI NI NIN NI NIN		
	2002	O. L.			For internal test only	these pins should be open or connected to		
76553					,	ground as they are not in use for this module		
47	EC S	OPEN						
48	SDAO	0				Serial data output of SPI		
49	SDAI	1				Serial data input of SPI		
50	SCL	1		SPI	SPI	Clock signal of SPI		
			1	SFI	SFI	Chip select signal		
51	CSB	1				CSB=0: Selected (accessible)		
						CSB=1: Not selected (inaccessible)		
52	VSSA	Р	3	0.00	analog ground	Analog circuit ground		
53	VSSA	Р	ÿ.	0.00	analog ground	Analog circuit ground		
54	VCC2	Р		3.0	power supply	External power supply for internal references		
55	VCC1	Р		3.0	power supply	External main and I/O power supply		
	VDD OTD	ODEN		0.50		5		
56	VDD_OTP	OPEN		9.50	For internal test only	this pin should be open or connected to ground as it is not in use for this module		
57	VGL	P		-12.00	power supply	power supply for Gate off output		
58	VGH	P		14.00	power supply	power supply for Gate on output		
59	VDD	P		3.30	power supply	Digital power supply		
60	VSS	Р		0.00	Digital ground	Logic circuit and I/O ground (0V)		
00	•00	25.70		0.00	Digital ground	Logic circuit and iro ground (01)		

Note:
Voltage levels listed in this table are for indication, chapter Electrical characteristics is leading.
Pins reserved for internal test are suggested to keep open or default setting.
H and L are both allowed since the pins are useless for function setting.

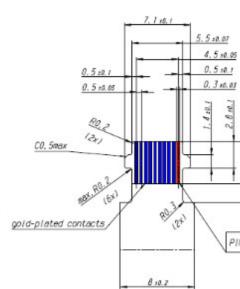
3.2 Backlight

Left side

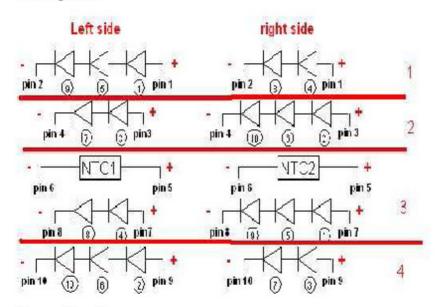
Pin1	LED1+I
Pin2	LED1-I
Pin3	LED3+I
Pin4	LED3-I
Pin5	NTC1
Pin6	GND
Pin7	LED4+I
Pin8	LED4-I
Pin9	LED 2+I
Pin10	LED 2-I

Right side

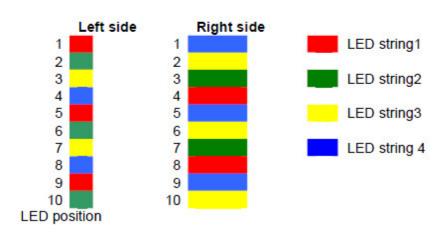
Pin1	LED1+r
Pin2	LED1-r
Pin3	LED3+r
Pin4	LED3-r
Pin5	NTC2
Pin6	GND
Pin7	LED4+r
Pin8	LED4-r
Pin9	LED 2+r
Pin10	LED 2-r



Pinning table



Connection diagram



4 Absolute maximum ratings

There is a difference between the maximum value of a parameter's specification and its absolute maximum value. The maximum value indicates that the performance will be reduced when you go beyond this value but this is reversible. Where the absolute maximum value as indicated in this section is a value beyond which permanent damage to the product or its function may be expected.

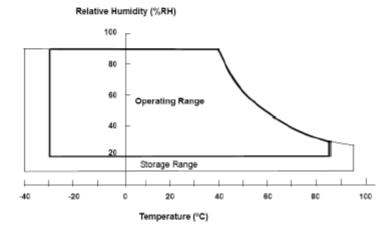
Function operation should be restricted to the conditions described under Normal Operating Conditions.

4.1 Absolute ratings of environment

Item	Symbol	Min.	Max.	Unit	Remark
Operating temperature	OTR	-30	+85	℃	Note 1,2
Storage temperature	STR	-40	+90	℃	Note 1

Note 1: Panel surface temperature, no condensation allowed under any condition.

Note 2: Operating from -40/-30'C possible, readable to some extent, cosmetic defects can happen.



To prevent overheating the LCM backside cold air flow is required.

4.2 Absolute ratings of TFT LCD module

Item	Symbol	Min.	Max.	Unit	Remark
Main and I/O power Supply	VCC1	0	3.96	V	rtemant
Power Supply for internal reference	VCC2	0	3.96	V	
Power Supply Source driver	VDDN	-7.37	0	V	
Power Supply Source driver	VDDP	0	7.37	V	
Power Supply Gate driver	VDD	-0.3	7.0	V	
Power Supply Gate off	VGL	VGH - 42	0.3	V	
Logic signals Gate on	VGH	-0.3	42	V	
Digital inputs		-0.3	7.3		

Note: GND=0V

4.3 Absolute ratings of Backlight unit

Item	Symbol	Min.	Max.	Unit	Remark
LED Light Bar Power Supply	led	0	280	mA	Per chain
Current					

5

5.1 Recommended operation conditions (based on GND=0V; Ta 25'C±2'C)

Item	Symbol	Min.	Тур	Max.	Unit	Remark
Power Supply	VCC1	2.7	3.0	3.6	٧	Note 2
Power Supply	VCC2	2.7	3.0	3.6	٧	Note 2
Power Supply Source	VDDN	-6.7	-6.6	-6.5.	٧	Note 1,2
driver						
Power Supply Source	VDDP	6.5	6.6	6.7	V	Note 1,2
driver						
Digital Power Supply	VDD	2.3	3.3	5.0	V	Note 2
Power Supply Gate off	VGL	-13	-12	-10	٧	Note 2
Power Supply Gate on	VGH	13	14	20	V	Note 2
Logic signals off	VIL	0		0.2VCC	V	
Logic signals on	VIH	0.8VCC		VCC	٧	
Power Supply	VCC1	26	30.7	35.6	mA	
Power Supply	VCC2	26	30.7	35.6	mA	
Power Supply Source	VDDN	46.3	56.6	61.9	mA	
driver						
Power Supply Source	VDDP	36.2	45.4	50.4	mA	
driver						
Digital Power Supply	VDD	0.1	0.12	0.15	mA	
Power Supply Gate off	VGL	0.23	0.25	0.3	mA	
Power Supply Gate on	VGH	0.22	0.27	0.31	mA	

Note 1 Typ value of VDDP and VDDN might be adjusted for design margin if the optical performance can be kept.

The VCC (VCC1, VCC2) & VDD ripple shall be less than 50m Volt (+/- value)

The VDDN &VDDP ripple is suggested to be less than 100mVolt mVolt (+/- value).

The VGH &VGL ripple is suggested to be less than 100mVolt mVolt (+/- value)

Ripple higher than the suggested value should be verified by the actual application.

5.2 Backlight Unit (based on GND=0V; Ta 25'C±2'C)

Item	Symbol	min	Тур	Max.	Unit	Remark
LED Power Supply Voltage			16	18	V	Per chain
LED Power Supply Voltage			3.2	3.6	V	Per LED *
LED Power Supply current			160		mA	Per chain
Power Consumption	Р		10.24	11.52	W	Total backlight
LED Life Time	Lbl	50000			hours	
Number of Chains		-	4			
Leds per Chains		-	5			

Note:

- 1. LED type used Nichia NS2W150T. There are 2 brightness ranks PA12 and PA13, 3 color ranks t03, t04, t05 used.
- 2. The lifetime of LED is defined as the time when it continues to operate under the conditions at $Ta = 25 \pm 2$ °C and $I_L = typ$ setting (Per EA) until the brightness becomes 50% of its original value.