DISPLAY UNIT USER'S MANUAL

Dot-Matrix LCD Units

(with built-in controllers)

SHARP

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PREFACE

The Sharp dot-matrix LCD units, with built-in controllers, operate under the control of a 4-bit or 8-bit microcomputer to display alphanumeric characters, symbols, etc.

The LCD unit provides the user with a dot-matrix display panel featuring simple interface circuitry.

Table 1.
Dot-Matrix LCD Unit with Built-In Controllers

MODEL NO.	NUMBER OF CHARACTERS	DISPLAY FORMAT
LM161XXX	16 × 1	5 × 7 dots
LM162XXX	16 × 2	5 × 7 dots
LM202XXX	20 × 2	5 × 7 dots
LM40X2XX	40 × 2	5 × 7 dots

FEATURES

- Interface with either 4-bit or 8-bit microprocessor.
- Display data RAM
- 80 × 8 bits (80 characters).
- Character generator ROM
- 160 different 5 × 7 dot-matrix character patterns.
- Character generator RAM
- 8 different user programmed 5 × 7 dot-matrix patterns.
- Display data RAM and character generator RAM may be accessed by the microprocessor.
- Numerous instructions
- Clear Display, Cursor Home, Display ON/OFF, Cursor ON/OFF, Blink Character, Cursor Shift, Display Shift.
- Built-in reset circuit is triggered at power ON.
- Built-in oscillator.

OVERVIEW

The LCD unit receives character codes (8 bits per character) from a microprocessor or microcomputer, latches the codes to its display data RAM (80-byte DD RAM for storing 80 characters), transforms each character code into a 5 × 7 dot-matrix character pattern, and displays the characters on its LCD screen.

The LCD unit incorporates a character generator ROM which produces 160 different 5 × 7 dot-matrix character patterns. The unit also provides a character generator RAM (64 bytes) through which the user may define up to eight additional 5 × 7 dot-matrix character patterns, as required by the application.

To display a character, positional data is sent via the data bus from the microprocessor to the LCD unit, where it is written into the instruction register. A character code is then sent and written into the data register. The LCD unit displays the corresponding character pattern in the specified position. The LCD unit can either increment or decrement the display position automatically after each character entry, so that only successive characters codes need to be entered to display a continuous character string. The display/cursor shift instruction allows the entry of characters in either the left-to-right or right-to-left direction. Since the display data RAM (DD RAM) and the character generator RAM (CG RAM) many be accessed by the microprocessor, unused portions of each RAM may be used as general purpose data areas. The LCD unit may be operated with either dual 4-bit or single 8-bit data transers, to accommodate interfaces with both 4-bit and 8-bit microprocessors. The low power feature of the LCD unit will be further appreciated when combined with a CMOS microprocessor.

HARDWARE

Interface Signals

Table 2. Interface Signals

SIGNAL NAME	INPUT/OUTPUT	EXTERNAL CONNECTION	FUNCTION
RS	Input	MPU	Register select signal "0": Instruction register (when writing) Busy flag and address counter (when reading) "1": Data register (when writing and reading)
R/W	Input	MPU	Read/write select signal: "0": Writing; "1": Reading
E	Input	MPU	Operation (data read/write) enable signal
DB_4 - DB_7	Input/Output	MPU	High-order lines of data bus with three-state, bidirctional function for use in data transactions with the MPU. DB_7 may also be used to check the busy flag.
DB_0 - DB_3	Input/Output	MPU	Low-order lines of data bus with three-state, bidirectional function for use in data transactions with the MPU. These lines are not used when interfacing with a 4-bit microprocessor.
V_{DD}, V_{SS}		Power Supply	V_{DD}: +5 V, V_{SS}: GND
V_0		Power Supply	Contrast adjustment voltage

Functional Blocks

Registers

The LCD unit has two 8-bit registers - an instruction register (IR) and a data register (DR). The instruction register stores instruction codes such as "clear display" or "shift cursor", and also stores address information for the display data RAM and character generator RAM. The IR can be accessed by the microprocessor only for writing.

The data register is used for temporarily storing data during data transactions with the microprocessor. When writing data to the LCD unit, the data is initially stored in the data register, and is then automatically written into either the display data RAM or character generator RAM, as determined by the current operation. The data register is also used as a temporary storage area when reading data from the display data RAM or character generator RAM. When address information is written into the instruction register, the corresponding data from the display data RAM or character generator RAM is moved to the data register. Data transfer is completed when the microprocessor reads the contents of the data register by the next instruction. After the transfer is completed, data from the next address position of the appropriate RAM is moved to the data register, in preparation for subsequent reading operations by the microprocessor. One of the two registers is selected by the register select (RS) signal.

Table 3. Register Selection

RS	R/W	OPERATION
0	0	Write to instruction register, and execute internal operation (clear display, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 - DB_6)
1	0	Write to data register, and execute internal operation (DR $\rightarrow$ DD RAM or DR $\rightarrow$ CG RAM)
1	1	Read data register and execute internal operation (DD RAM $\rightarrow$ DR or CG RAM $\rightarrow$ DR)

Busy Flag (BF)

When the busy flag is set at a logical "1", the LCD unit is executing an internal operation, and no instruction will be accepted. The state of the busy flag is output on data line DB_7 in response to the register selection signals RS = 0, R/W = 1 as shown in Table 3. The next instruction may be entered after the busy flag is reset to logical "0".

Address Counter (AC)

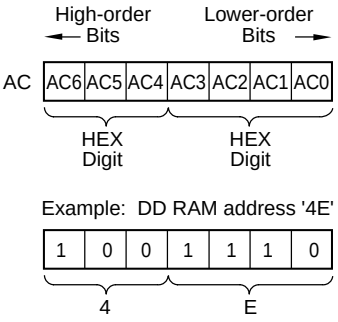
The address counter generates the address for the display data RAM and character generator RAM. When the address set instruction is written into the instruction register, the address information is sent to the address counter. The same instruciton also determines which of the two RAM's is to be selected.

After data has been written to or read from the display data RAM or character generator RAM, the address counter is automatically incremented or decremented by one. The contents of the address counter are output on data lines DB_0 - DB_6 in response to the register selection signals RS = 0, R/W = 1 as shown in Table 3.

Display Data RAM (DD RAM)

This 80 x 8 bit RAM stores up to 80 8-bit character codes as display data. The unused area of the RAM may be used by the microprocessor as a general purpose RAM area.

The display data RAM address, set in the address counter, is expressed in hexadecimal (HEX) numbers as follows:



The address of the display data RAM corresponds to the display position on the LCD panel as follows:

a. Address type a . . . .For dual-line display

Display Position

Digit	1	2	3	4	5	6	7	8	9		39	40
Line 1	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	· · ·	26_H	27_H
Line 2	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H	· · ·	66_H	67_H

DD RAM Address (HEX)

When a display shift takes place, the addresses shift is as follows:

Left Shift	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	09_H	· · ·	27_H	00_H
	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H	49_H	· · ·	67_H	40_H

Right Shift	27_H	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	· · ·	25_H	26_H
	67_H	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	· · ·	65_H	66_H

The addresses for the second line are not continuous to the addresses for the first line. A 40-character RAM area is assigned to each of the two line as follows:

line 1: 00_H - 27_H

line 2: 40_H - 67_H

For an LCD unit with a display capacity of less than 40 characters per line, characters equal in number to the display capacity, as counted from display position 1, are displayed.

b. Address type b . . . .For single-line display with logically dual-line addressing

Digit Display Position

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H

DD RAM Address (HEX)

When a display shift takes place, the addresses shift as follows:

Left Shift	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H

Right Shift	27_H	00_H	01_H	02_H	03_H	04_H	05_H	06_H	67_H	40_H	41_H	42_H	43_H	44_H	45_H	46_H

The right-hand eight characters, for the purposes of addressing and shifting, may be considered to constitute a second display line. For the address type of each model, see Table 12.

Character Generator ROM (CG ROM)

This ROM generates a 5 × 7 dot-matrix character pattern for each of 160 different 8-bit character codes. The correspondence between character codes and character patterns is shown in Tables 4 and 5. Inquiries are invited for units with custom character patterns.

Character Generator RAM (CG RAM)

This RAM stores eight arbitrary 5 x 7 dot-matrix character patterns, as programmed by the user. For displaying a character pattern stored in the CG RAM, a character code corresponding to the left-most column in Tables 4 and 5 is written into the display data RAM.

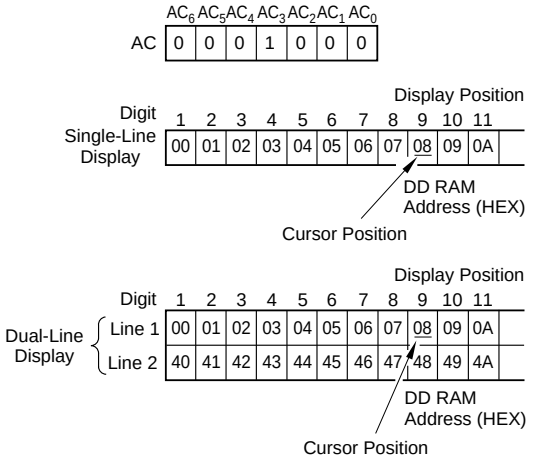
For the relationship among the CG RAM address, the display data, and the displayed pattern, see Table 6. As shown in Table 6., the unused portion of the CG RAM may be used as a general purpose RAM area.

Timing Generator

The timing generator produces timing signals used for the internal operation of the display data RAM, character generator ROM,and character generator RAM. Timing in controlled so that read-out of the RAM for display and access to the RAM by the external microprocessor do not interfere. Display flicker when data is written to the display data RAM is eliminated.

Cursor/Blink Controller

This circuit can be used to generate a cursor or blink a character in the display position indicated by the DD RAM address, which is set in the address counter (AC). The following example shows the cursor position when the address counter contains "08" (HEX).



NOTE:
The address counter has the dual function of containing either a DD RAM address or a CG RAM address. The cursor/blink controller does not distinguish between these two functions, and thus, when activated, it always considers the address counter to contain a DD RAM address. To avoid spurious cursor/blink effects, the cursor/blink function should be turned off while the microprocessor writes to or reads from the CG RAM.

Parallel-to-Serial Converter

This circuit converts parallel data read from the CG ROM or CG RAM to serial data for use by the display driver.

Bias Voltage Generator

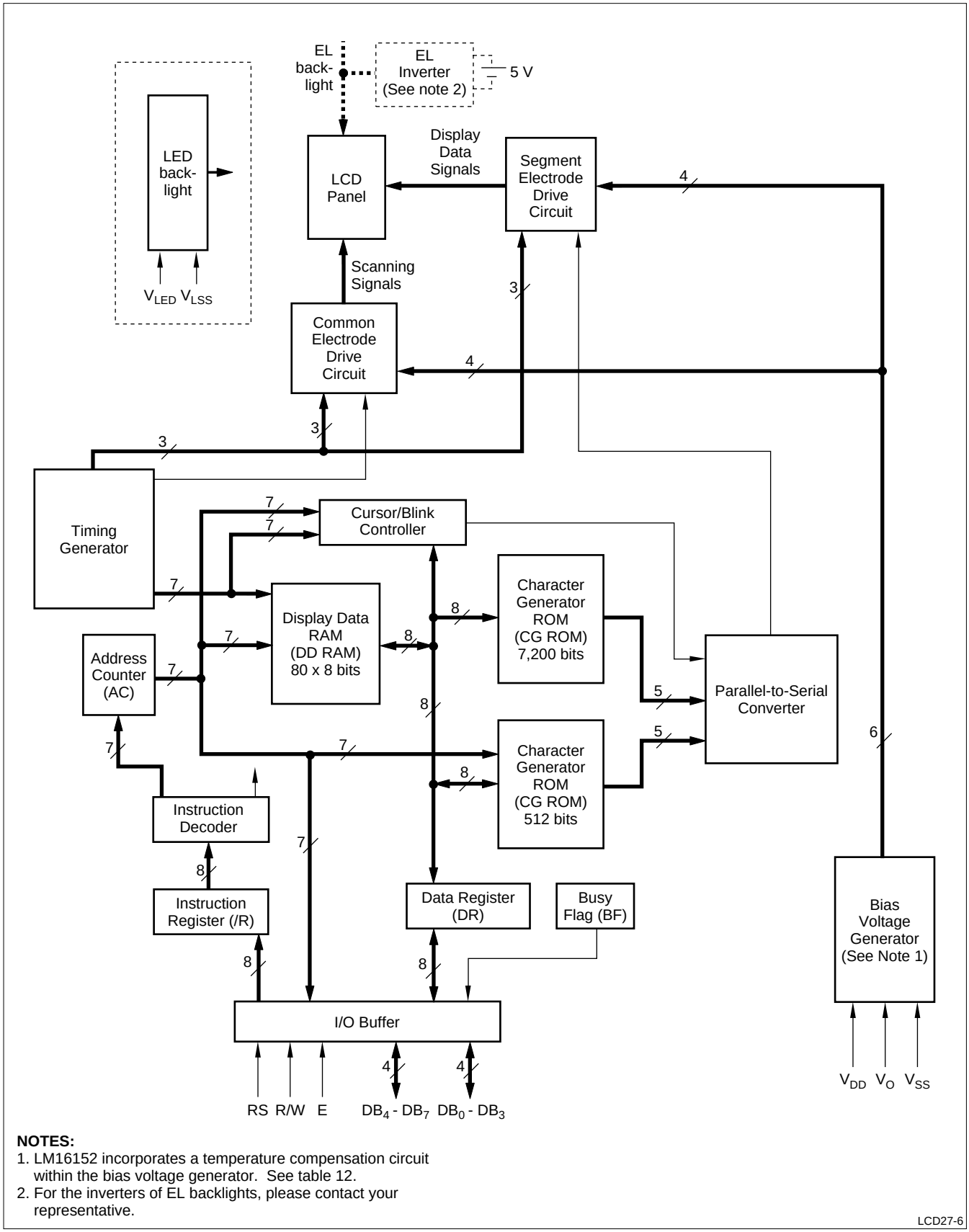
This circuit provides the bias voltage level required for driving the liquid crystal display. Some models incorporate a temperature compensation circuit which generates a temperature dependent bias voltage in order to provide constant display contrast at all ambient temperature levels.

LCD Driver

This circuit receives display data, timing signals, and bias voltage, and produces the common and segment display signals.

LCD Panel

This is a dot-matix liquid crystal display panel arranged in either 1 row of 16 characters, 2 rows of 16 characters, 2 rows of 20 characters, or 2 rows of 40 characters.



NOTES:
1. LM16152 incorporates a temperature compensation circuit within the bias voltage generator. See table 12.
2. For the inverters of EL backlights, please contact your representative.

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Figure 1. Functional Block Diagram

Table 4. Character Codes

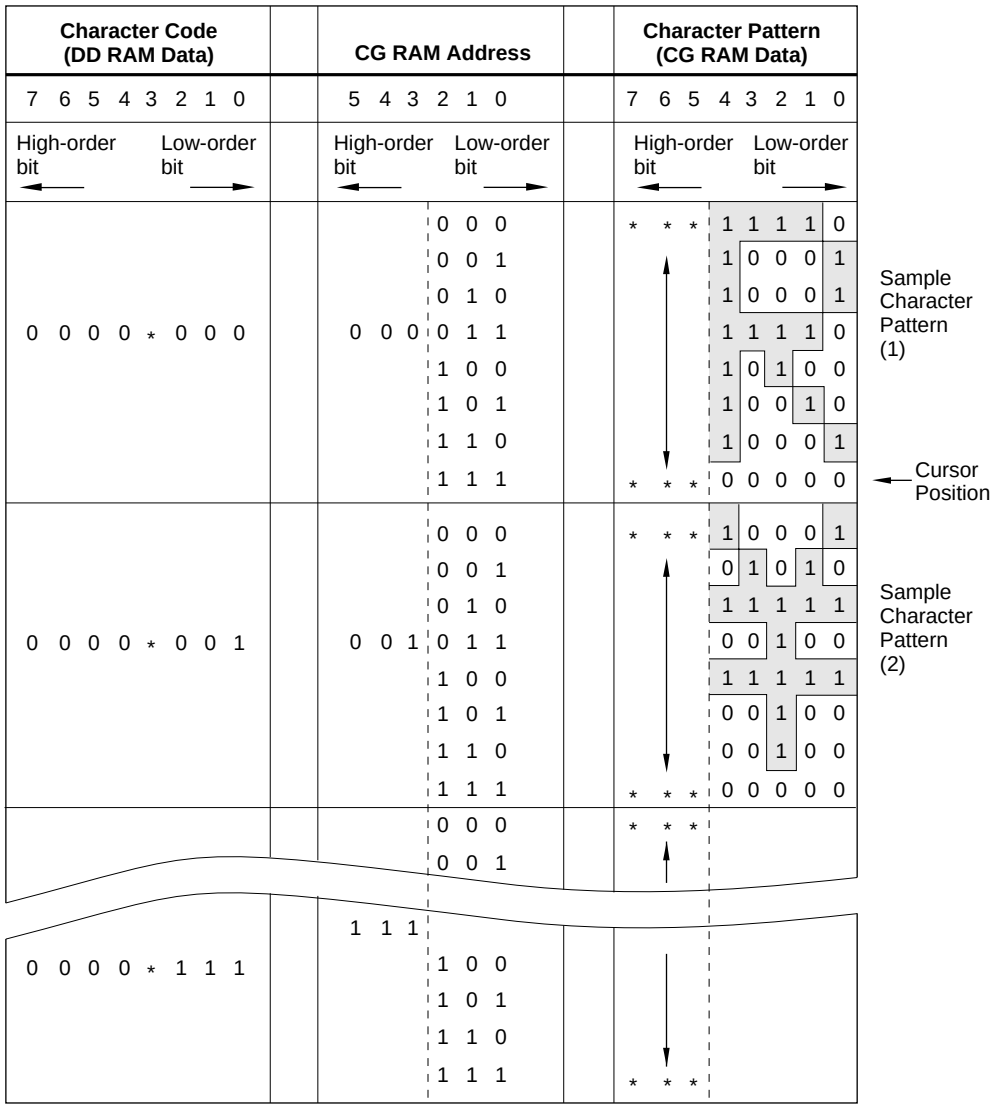
HIGH-ORDER 4 BIT / LOW-ORDER 4 BIT	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxx0101	(6)												
xxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

NOTES:
1. The CG RAM generates character patterns in accordance with the user's program.
2. Shaded areas indicate 5 x 10 dot character patterns.

Table 5. Character Codes

Low-Order 4 bit \ High-Order 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000	CG RAM (1)		0	@	P	\	p		ー	タ	ミ	α	p
××××0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
××××0010	(3)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
××××0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
××××0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
××××0101	(6)	%	5	E	U	e	u	•	オ	ナ	ユ	σ	ü
××××0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
××××0111	(8)	'	7	G	W	g	w	ァ	キ	ヌ	ラ		π
××××1000	(1)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	$\bar{x}$
××××1001	(2)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	−1	y
××××1010	(3)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	
××××1011	(4)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	x	
××××1100	(5)	,	<	L	¥	1	|	ャ	シ	フ	ワ	¢	
××××1101	(6)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
××××1110	(7)	.	>	N	^	n	→	ョ	セ	ホ	゛	$\bar{n}$	
××××1111	(8)	/	?	O	_	o	←	ッ	ソ	マ	°	ö	■

Table 6. Relationship Among Character Code
(DD RAM), CG RAM Address, and Character Pattern (CG RAM)



NOTES:

1. Character code bits 0 - 2 correspond to CG RAM address bits 3 - 5. Each of the 8 unique bit strings designates one of the 8 character patterns.
2. CG RAM address bits 0 - 2 designate the row position of each character pattern. The 8th row is the cursor position. CG RAM data in the 8th row is OR'ed with the display cursor. Any '1' bits in the 8th row will result in a displayed dot regardless of the cursor status (ON/OFF). Accordingly, if the cursor is to be used, CG RAM data for the 8th row should be set to '0'.
3. CG RAM data bits 0 - 4 correspond to the column position of each character pattern bit 4 corresponding to the left most column of the character pattern. CG RAM data bits 5 - 7 are not used for displaying character patterns, but may be used as a general purpose RAM area.
4. As shown in tables 4 and 5, character patterns in the CG RAM are accessed by character codes with bits 4 - 7 equal to '0'. For example, the character pattern 'R', shown in the first sample character pattern of the table, is selected by the character code '00' (HEX) or '08' (HEX), since bit 3 of the character code is a don't care" bit (i.e., can take either value, '00' or '1').
5. CG RAM data '1' produces a dark dot, and data '0' produces a light dot in the corresponding position on the display panel.
6. * = Signifies a "don't care" bit

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Microprocessor Interface

The LCD unit performs either dual 4-bit or single 8-bit data transers, allowing the user to interface with either a 4-bit or 8-bit microprocessor

4-Bit Microprocessor Interface.

Data lines DB_4 - DB_7 are used for data transfers. Data transactions with the external microprocessor take place in two 4-bit data transfer operations.

The high-order 4 bits (corresponding to DB_4 - DB_7 in an 8-bit transfer) are transferred first, followed by the low-order 4 bits (corresponding to DB_0 - DB_3 in an 8-bit transfer). The busy flag is to be checked on completion of the second 4-bit data transfer. Busy flag and address counter are output in two operations.

8-bit Microprocessor Interface

Each 8-bit piece of data is transferred in a single operation using the entire data bus DB_0 - DB_7.

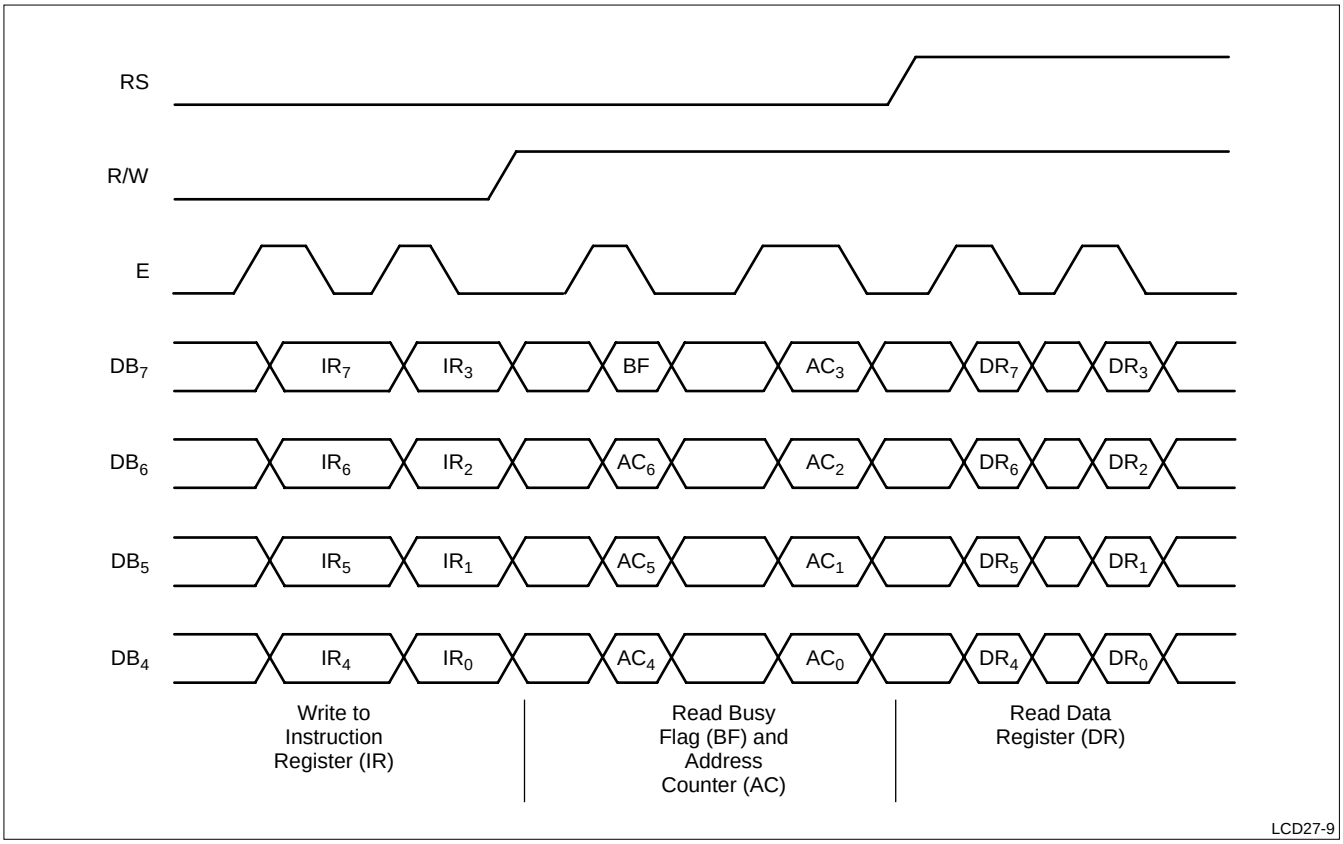


Figure 2. 4-Bit Data Transfer

Reset Function

Initialization by Internal Reset Circuit

The LCD unit has an internal reset circuit for implementing an automatic reset operation at power-on. During the initalization operation, the busy flag is set. The busy state lasts for 10 msec after V_{DD} reaches 4.5 V. The following instructions are executed in initializing the LCD unit.

1. Clear Display

2. Function Set

   DL = 1 . . . . 8-bit data length for interface
   N = 0 . . . . Single-line display
   F = 0 . . . . 5 × 7 dot-matrix character font

3. Display ON/OFF Control

   D = 0 . . . .Display OFF
   C = 0 . . . .Cursor OFF
   B = 0 . . . .Blink function OFF

4. Entry Mode Set

   I/D = 1 . . . .Increment Mode
   S = 0 . . . .Display shift OFF

CAUTION

If the power conditions stated in Table 11, "Power conditions applicable when internal reset circuit is used," are not satisfied, then internal reset circuit will not operate properly and the LCD unit will not be initalized. In this case, the initialization procedure must be executed by the external microprocessor.

Initialization by Instructions

If the power conditions for the normal operation of the internal reset circuit are not satisfied (see Table 11), then LCD unit must be initialized by executing a series of instructions. The procedure for this initialization process is as follows:

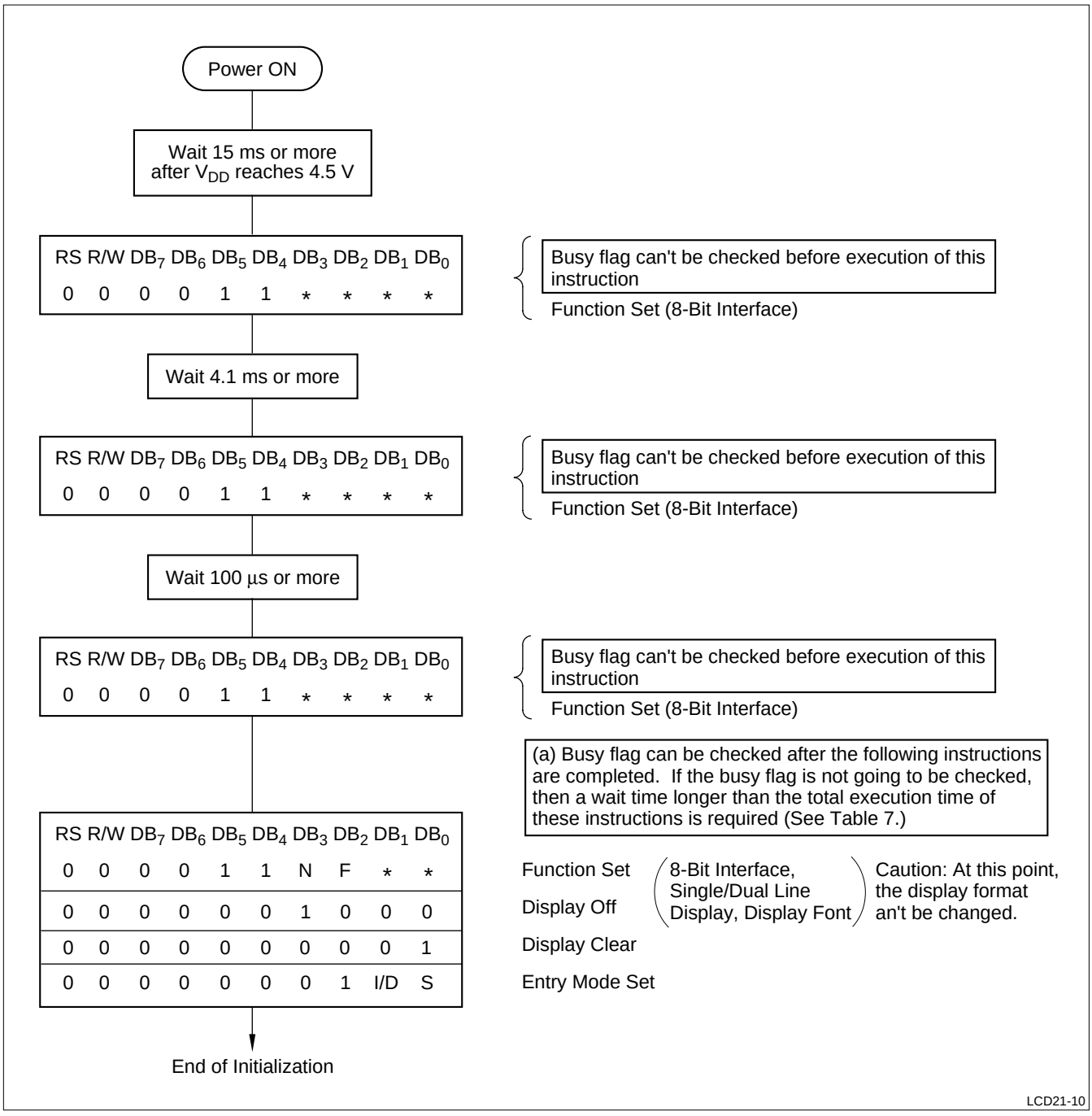


Figure 3. 8-Bit Interface

4-Bit Interface

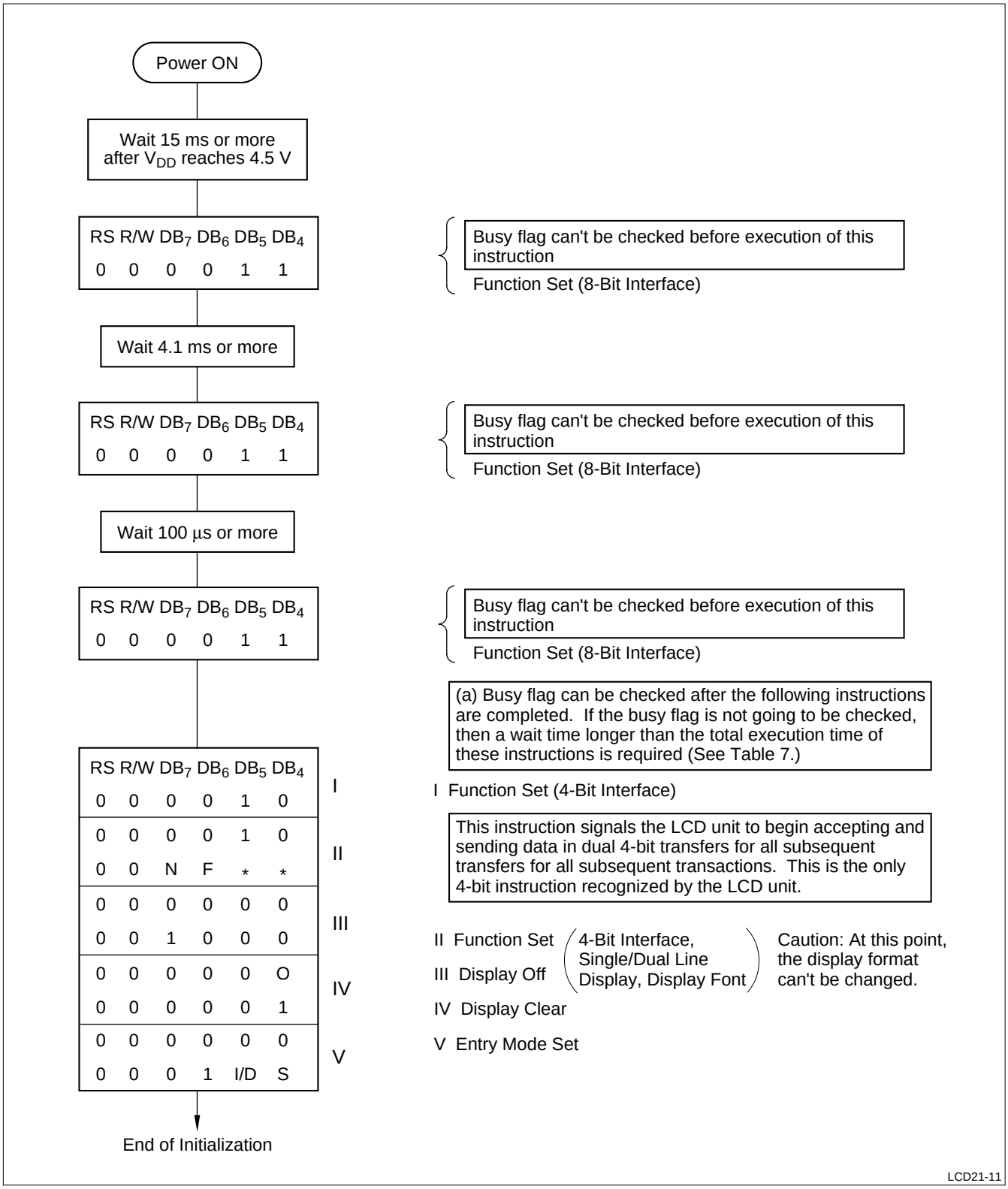


Figure 4. 4-Bit Interface

INSTRUCTIONS

General Information

When the LCD unit is controlled by an external microprocessor, the only registers which can be directly accessed by the microprocessor are the instruction register (IR) and data register (DR). Control information is buffered to allow the LCD unit to interface with various microprocessors and peripheral control devices with different operating speeds. The internal operation of the LCD unit is determined by the signals sent from the external microprocessor. These signals include the register select (RS) signal, the read/write (R/W) signal, and the data bus (DB_0 - DB_7) signals.

Table 7 lists the instructions available to the LCD unit, with their execution times. The instructions fall into the following four categories.

1. Instructions for setting LCD unit functions, such as display format and data length
2. Instructions for addressing the internal RAM's
3. Instructions for transferring data to or from the internal RAM's
4. Other instructions

In normal operation, instructions from category (3) are used most frequently. The internal RAM address may be incremented or decremented automatically after each data transaction, to reduce the programming requirements of the microprocessor. The display may also be shifted automatically after each display data write (see Sample Instruction Procedures section for examples). These features facilitate the construction of efficient systems.

During the internal execution of an instruction, no instruction other than the "busy flag/address counter read" instruction will be accepted. During internal operation the busy flag is set to "1". It is necessary for the microprocessor to check that the busy flag is reset to "0" before sending the next instruction.

NOTE

Either the microprocessor must check that the busy flag is not set to "1" before sending each instruction, or the interval waited before sending each instruction must be made sufficiently longer than the execution time of the previous instruction. For the execution time of each instruction, see Table 7.

Description of Instruction

Display Clear

	RS	R/W	DB_7						DB_0
CODE	0	0	0	0	0	0	0	0	1

The display data RAM is filled with the "space" code, 20_H. The address counter is reset to zero. If the display has been shifted, the original position is restored. By execution of this instruction, the display goes off, and the cursor and character blink functions, if activated, are moved to the upper, leftmost display position.

Display/Cursor Home

	RS	R/W	DB_7						DB_0
CODE	0	0	0	0	0	0	0	1	*

NOTE: * = Don't Care

The address counter is reset to zero. If the display has been shifted, the original position is restored. The content of the DD RAM is not affected. The cursor and character blink functions, if activated, are moved to the upper, leftmost display position.

Entry Mode Set

	RS	R/W	DB_7						DB_0
CODE	0	0	0	0	0	0	0	I/D	S

I/D: The address counter is incremented (I/D = 1) or decremented (I/D = 0) by one, following the reading or writing of each display data RAM character code. The cursor and character blink functions move one display position to the right (I/D = 1) or left (I/D = 0). The same operation takes place when data is written to or read from the character generator RAM.

S: When S = 1, the entire display is shifted one position to the left (I/D = 1) or right (I/D = 0) following the writing of a display data RAM character code. The cursor and character blink functions do not move relative to the display position. When S = 0, the display is not shifted. The display is not shifted when writing data to the character generator RAM.

Display ON/OFF

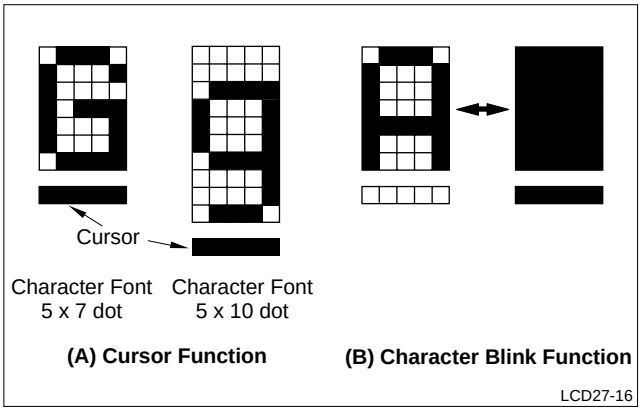
	RS	R/W	DB_7						DB_0
CODE	0	0	0	0	0	0	1	D	C	B

D: When D = 1, the display is turned on.

When D = 0, the display is turned off with the display data retained in the display data RAM.

C: When C = 1, the cursor is displayed in the position specified by the address counter. When C = 0, the cursor is not displayed. The cursor is made up of five dots displayed across the 8th display row, below the 5 × 7 dot-matrix character block. For 5 × 10 dot-matrix character blocks, 5 dots are displayed across the 11th row.

B: When B = 1, the character at the cursor position blinks on and off. When this function is activated, at fcp or fosc = 250 kHz, alternating between all dots black, and the display character, the character is alternately displayed for 409.6 ms and blanked for 409.6 ms. The cursor may be used simultaneously with the character blink function. (Blink frequency varies in proportion to the reciprocal of f_{CP} or f_{OSC}.
409.6 × 250/270 = 379.2 ms; f_{CP} = 270 kHz.)



Display/Cursor Shift

	RS	R/W	DB_7						DB_0
CODE	0	0	0	0	0	1	S/C	R/L	*	*

NOTE: * = Don't Care

The display and/or cursor are shifted to the right or left. For two-line displays, the cursor moves from the 40th position of the top line to the first position of the second line. From the 40th position of the second line, the cursor does not move back to the home position, but rather to the first position of the second line.

S/C	R/L	
0	0	Shift the cursor to the left (AC ← AC - 1).
0	1	Shift the cursor to the right (AC ← AC +1)
1	0	Shift the entire display, with the cursor, to the left.
1	1	Shift the entire display, with the cursor, to the right.

NOTE: When the display is shifted, the address counter is not affected.

Function Set

	RS	R/W	DB_7						DB_0
CODE	0	0	0	0	1	DL	N	0	*	*

NOTE: * = Don't Care

DL: Selects the interface data length. When DL = 1, 8-bit data transfers are used. When DL = 0, 4-bit data transfers are used.

NOTE

When using a 4-bit data length, two transfer operations are needed to transfer a complete data word to or from the external micoprocessor.

N: Selects display format (single or dual line). See Table 12 for the correct input value for each model.

CAUTION

The function set instruction must be executed at the beginning of the microprocessor program, before all other instructions except the busy flag/address counter read instruction. The function set instruction cannot be executed again except to change the interface data length. Once set, the display format cannot be changed.

CG RAM Address Set

	RS	R/W	DB_7							DB_0
CODE	0	0	0	1	A	A	A	A	A	A

The address counter is loaded with a character generator RAM address, expressed as a 6-digit binary number. Following the execution of this instruction, subsequent data transactions will be between the external microprocessor and the character generator RAM.

DD RAM Address Set

	RS	R/W	DB_7							DB_0
CODE	0	0	1	A	A	A	A	A	A	A

The address counter is loaded with a display data RAM address, expressed as a 7-digit binary number. Following the execution of this instruction, subsequent data transactions will be between the external microprocessor and the display data RAM. For N = 0 (single line display), the binary number, A_{DD} may have a value ranging from 00_H to $4F_H$. For N = 1 (dual line display), the binary number, A_{DD}, may have a value ranging from 00_H to 27_H for the first line, or 40_H to 67_H for the second line.

Busy Flag/Address Counter Read

	RS	R/W	DB_7							DB_0
CODE	0	1	BF	A	A	A	A	A	A	A1

The busy flag (BF) is read out, and indicates whether or not the LCD unit is still executing the previous instruction. BF = 1 indicates the busy state (internal operation), and the next instruction will not be accepted until BF = 0. This instruction also reads out the contents of the address counter, expressed as a 7-digit binary number. The address counter is used for accessing both the character generator RAM and the display data RAM. On read-out, the address counter will contain either a character generator RAM address or a display data RAM address, as determined by the most recently executed address set instruction.

CG RAM/DD RAM Data Write

	RS	R/W	DB_7							DB_0
CODE	1	0	D	D	D	D	D	D	D	D

An 8-bit data word is written into either the character generator RAM or display data RAM, as determined by the most recently executed address set instruciton. The data is written into the RAM location specified by the address counter. After the data is written into the RAM, the address counter is either incremented or decremented by one, as determined by the current entry mode. A display shift may also take place after the data is written.

CG RAM/DD RAM Data Read

	RS	R/W	DB_7							DB_0
CODE	1	1	D	D	D	D	D	D	D	D

An 8-bit data word is read from either the character generator RAM or display data RAM, as determined by a previously executed address set instruction. The data is read from the RAM location specified by the address counter.

This instruction must be immediately preceded by the CG RAM address set instruction, the DD RAM address set instruction, the cursor shift instruction, or a previous CG RAM/DD RAM data read instruction. Any other preceding instruction will cause invalid data to be read. The address set instructions cause the address counter to be loaded with a valid data read address.

The cursor shift command allows selected DD RAM data to be read without the necessity of resetting the DD RAM address. Following the cursor shift instruction, the CG RAM/DD RAM data read instruction will read data from the DD RAM.

After the execution of each data read instruction, the address counter is either incremented or decremented by one, as determined by the current entry mode. It is not necessary to reset the RAM address before the execution of subsequent data read instructions if the same RAM is to be read. The display is not shifted by the data read instruction.

NOTE

After the execution of the CG RAM/DD RAM data write instruction, the address counter is incremented or decremented automatically. However, the contents of the RAM location specified by the address counter cannot be read by a subsequent CG RAM/DD RAM data read instruction. The correct procedure for reading data from the CG RAM or DD RAM is to execute an address set or cursor shift instruction. Once a data read instruction has been executed, successive data read instructions may be executed, with no requirement for intervening instructions.

Table 7. Instruction Set

INSTRUCTION	CODE										FUNCTION	EXECUTION TIME (max) (f_{CP} or f_{OSC} = 250 kHz)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Display Clear	0	0	0	0	0	0	0	0	0	1	Clear enter display area, restore display from shift, and load address counter with DD RAM address 00_H.	1.64 ms
Display/Cursor Home	0	0	0	0	0	0	0	0	1	*	Restore display from shift and load address counter with DD RAM address 00_H.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Specify cursor advance direction and display shift mode. This operation takes place after each data transfer.	40 µs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specify activation of display (D), cursor (C), and blinking of character at cursor position (B).	40 µs
Display/Cursor Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shift display or move cursor.	40 µs
Function Set	0	0	0	0	1	DL	N	0	*	*	Set interface data length (DL) and number of display lines (N).	40 µs
CG RAM Address Set	0	0	0	1	A_{CG}						Load the address counter with a CG RAM address. Subsequent data is CG RAM data.	40 µs
DD RAM Address Set	0	0	1	A_{DD}							Load the address counter with a DD RAM address. Subsequent data is DD RAM data.	40 µs
Busy Flag/Address Counter Read	0	1	BF	AC							Read busy flag (BF) and contents of address counter (AC).	0 µs
CG RAM/DD RAM Data Write	1	0	Write data								Write data to CG RAM or DD RAM.	40 µs
CG RAM/DD RAM Data Read	1	1	Read data								Read data from CG RAM or DD RAM.	40 µs
	I/D = 1: Increment, I/D = 0: Decrement S = 1: Display Shift On S/C = 1: Shift Display, S/C = 0: Move Cursor R/L = 1: Shift Right, R/L = 0: Shift Left DL = 1: 8-Bit, DL = 0: 4-Bit N = 1: Dual Line, N = 0: Single Line BF = 1: Internal Operation, BF = 0: Ready for Instruction										DD RAM: Display Data RAM CG RAM: Character Generator RAM A_{CG}: Character Generator RAM Address A_{DD}: Display Data RAM Address AC: Address Counter	

NOTES:

1. Symbol "*" signifies a "don't care" bit.
2. Correct input value for "N" is predetermined for each model (see Table 12).

ELECTRICAL CHARACTERISTICS

Absolue Maximum Ratings

See the device specifications for each LCD unit model.

Electrical Characteristics

See the device specificiations for each LCD unit model. Some of the currently available specifications do not describe the test conditions for the high-level and low-level output voltages. These conditions are as follows:

Table 8.

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Output Voltage	H	V_{OH}	$-I_{OH}$ = 0.205 mA	2.4	—	V
	L	V_{OL}	I_{OL} = 1.2 mA	—	0.4	V

Timing Characteristics

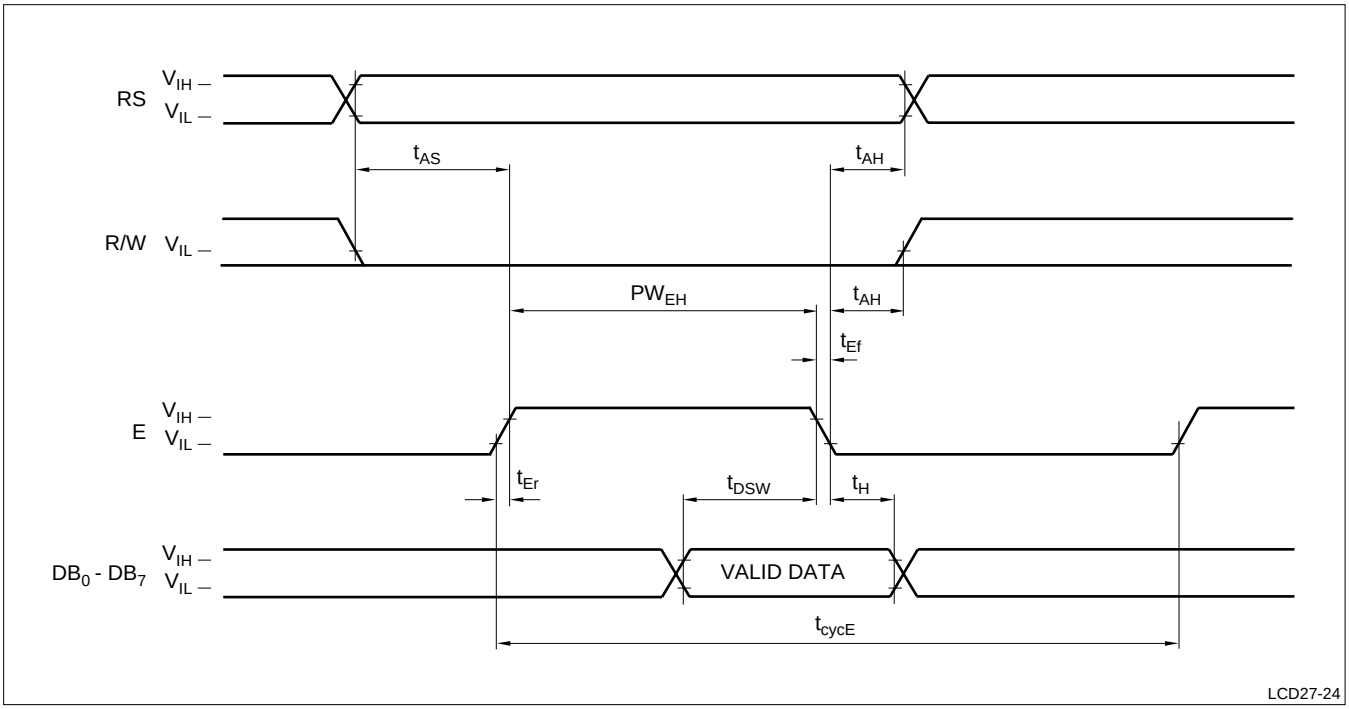


Figure 5. Write Operation Timing Diagram
(For data sent from the external microprocessor to the LCD unit)

Table 9. Write Operation Timing Characteristics
(V_{DD} = 5.0 ± 5%, V_{SS} = 0 V, T_A = 0 ~ 50°C)

PARAMETER		SYMBOL	VALUE		UNIT
			MIN.	MAX.	
Enable Cycle Time		$t_{CYC}E$	1000	—	ns
Enable Pulse Width	"High" Level	PW_{EH}	450	—	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns
Setup Time	RS, R/W-E	t_{AS}	140	—	ns
Address Hold Time		t_{AH}	10	—	ns
Data Setup Time		t_{DSW}	195	—	ns
Data Hold Time		t_H	10	—	ns

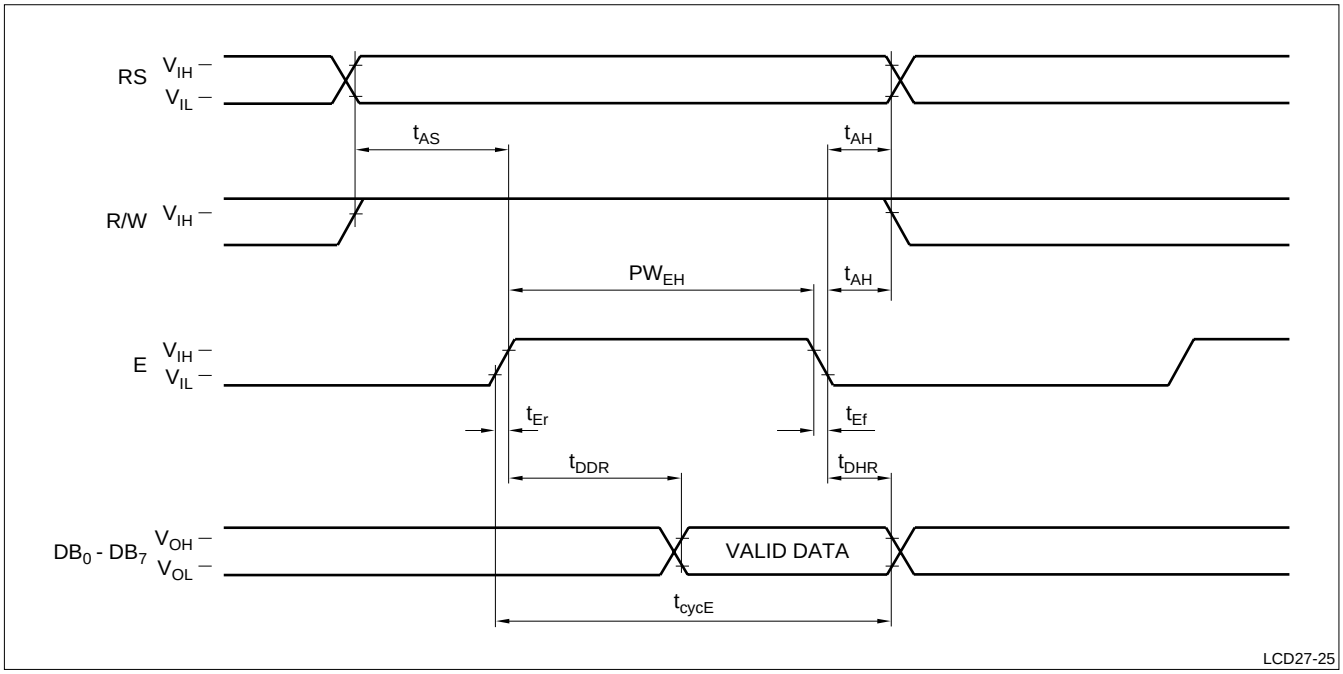


Figure 6. Read Operation Timing Diagram
(For data sent from the LCD unit to the external microprocessor)

Table 10. Read Operation Timing Characteristics
(V_{DD} = 5.0 ± 5%, V_{SS} = 0 V, Ta = 0 ~ 50°C)

PARAMETER		SYMBOL	VALUE		UNIT
			MIN.	MAX.	
Enable Cycle Time		$t_{cyc}E$	1000	—	ns
Enable Pulse Width	"High" Level	PW_{EH}	450	—	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns
Setup Time	RS, R/W-E	t_{AS}	140	—	ns
Address Hold Time		t_{AH}	10	—	ns
Data Delay Time		t_{DDR}	—	320	ns
Data Hold Time		t_{OHR}	20	—	ns

Table 11. Power Conditions for Internal Reset

PARAMETER	SYMBOL	VALUE			UNIT
		MIN.	TYP.	MAX.	
Voltage Build-Up Time	t_{rcc}	0.1	—	10	ms
Power-Off Period	t_{OFF}	1	—	—	ms

If the above conditions are not satisfied, the internal reset circuit will not operate normally. In such a case, the LCD unit must be initialized by executing a series of instructions (see the Execution by Instructions section).

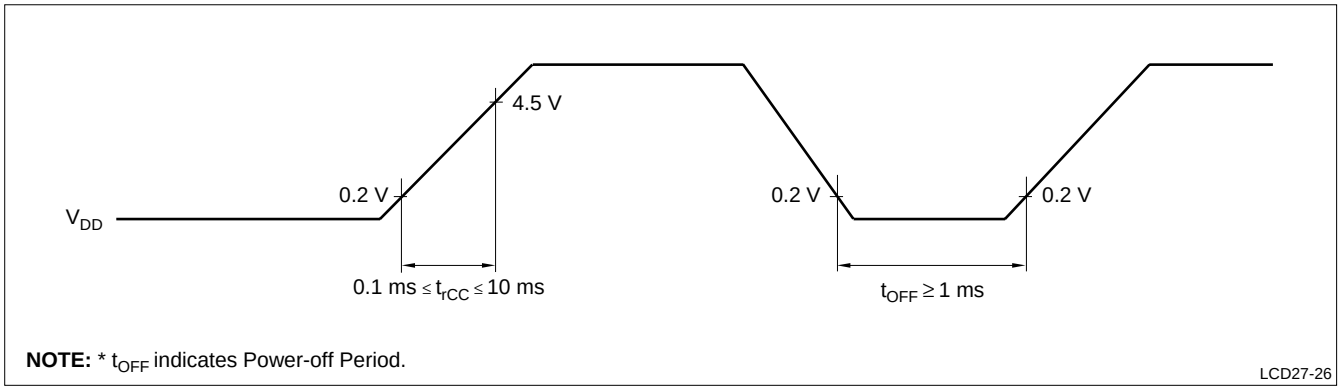


Figure 7.

LCD UNIT USAGE INSTRUCTIONS

Interface with External Microprocessor

1. 8-bit Microprocessor

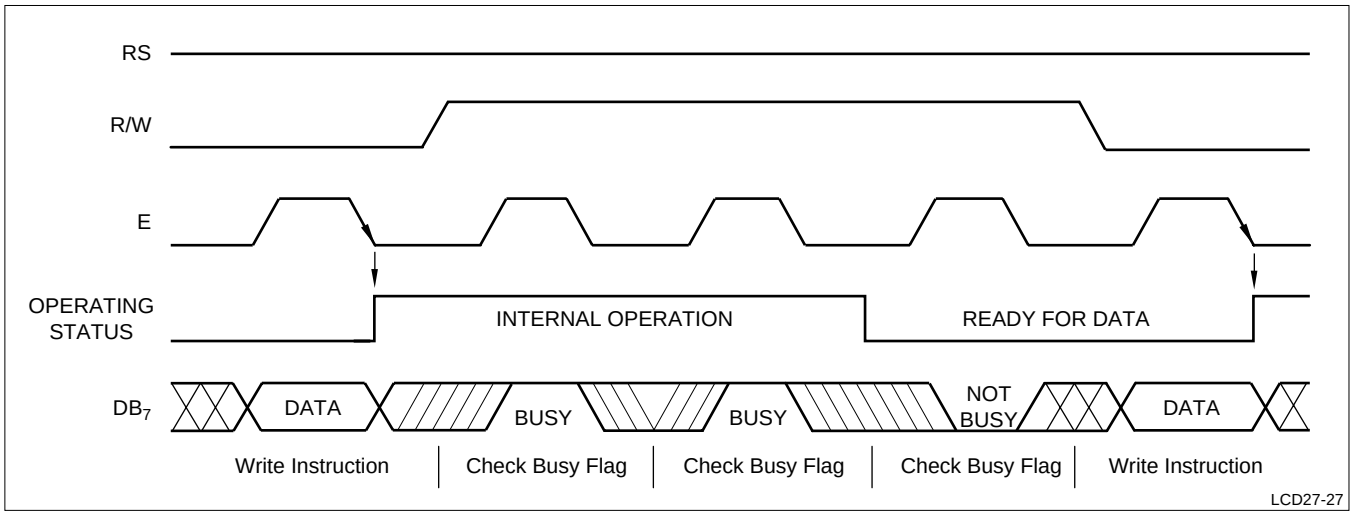
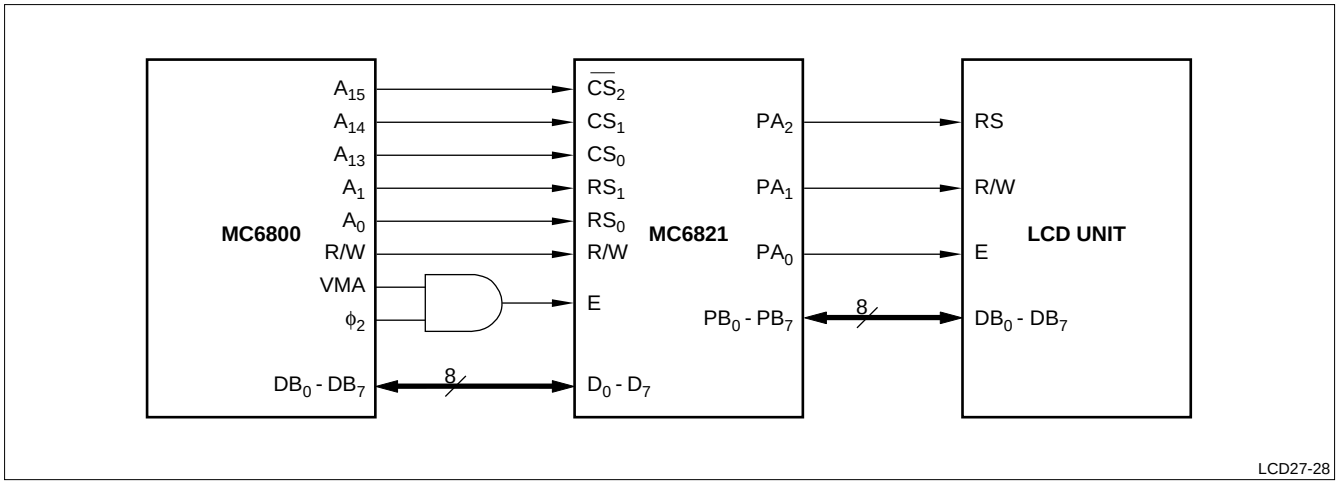


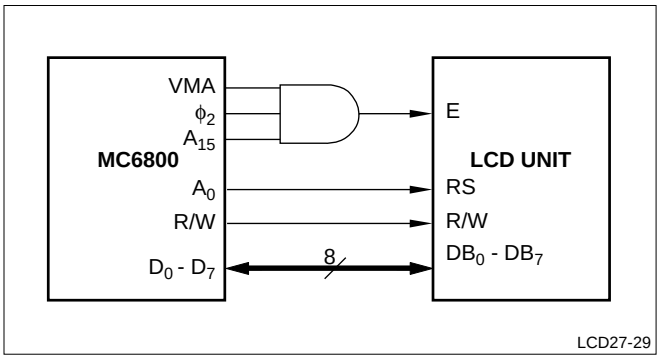
Figure 8. 8-Bit Interface Timing (Example)

a. Interface to 8-Bit Microprocessor via Peripheral Interface Adaptor (PIA). The following exemplifies the connection of the LCD unit to an 8-bit microprocessor chip through a PIA or I/0 port. The interface is TTL compatible. PB_0 - PB_7 of the interface device are connected to DB_0 - DB_7 of the LCD unit, and PA_0 - PA_2 are connected to E, R/W, and RS respectively.

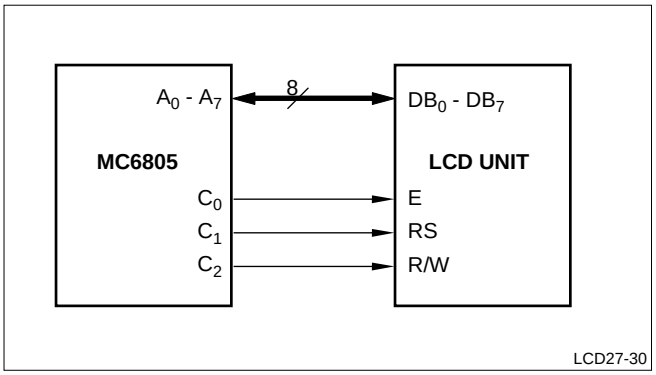
When the PIA is used, care must be taken to insure the proper relationship between the E signal and other signals when reading and writing data.



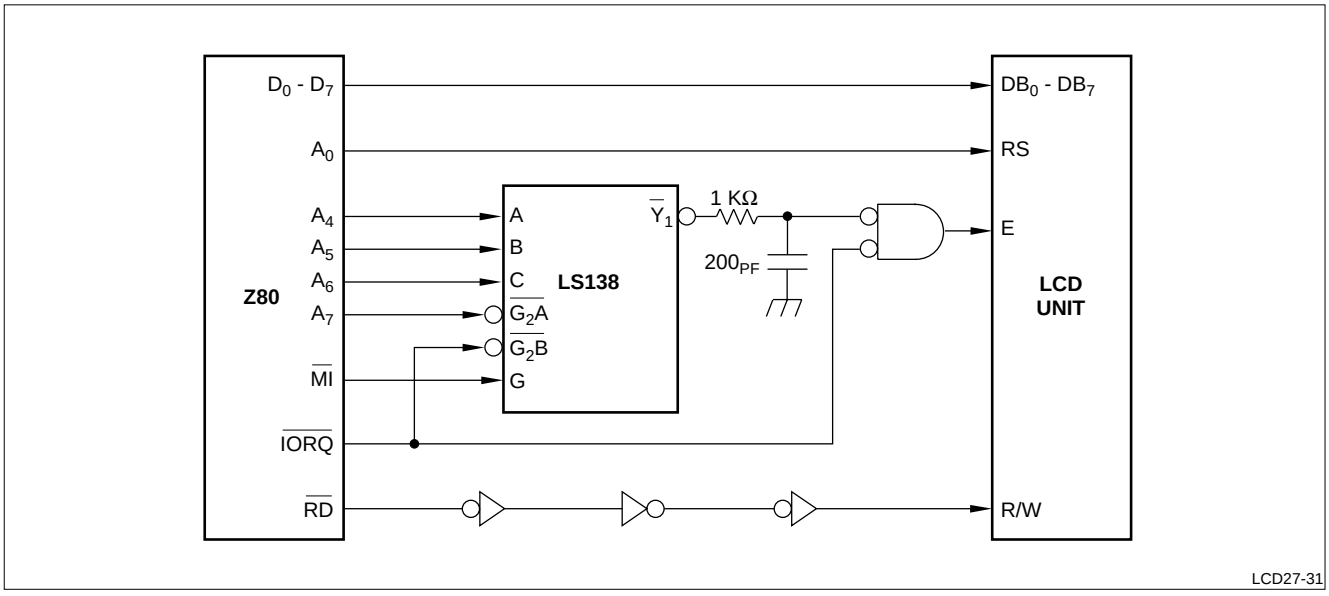
b. Direct Connection to 8-Bit Microprocessor



c. Interface with MC6805 Microprocessor



d. Interface with Z-80 Microprocessor



2. 4-Bit Data Transfer with a Single-Line, 16-Character Display (Using Internal Reset). Table 14 shows a sample operating procedure for an LCD unit in this mode. After power has been turned on, the 8-bit data transfer mode is in effect, and the first write operation is assumed to be an 8-bit data transfer.

   Since the data lines DB_0 - DB_3 are not connected, this data is not accepted and must be written again (i.e. the function set instruction must be written twice). Subsequent data transfers are completed in two 4-bit transfer operations (see Table 14).

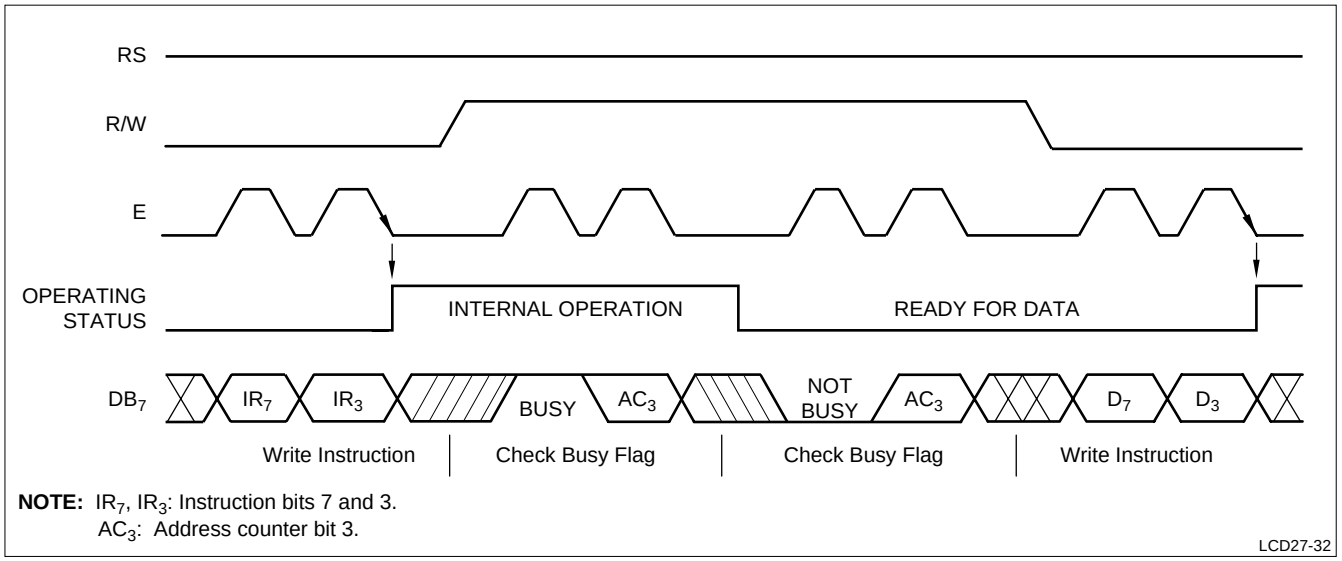


Figure 9. 4-Bit Interface Timing (Example)

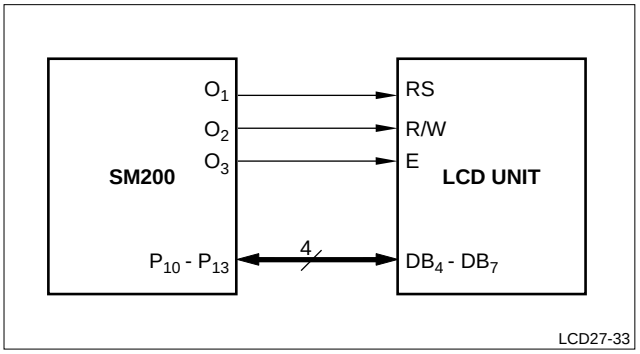


Figure 10. Connection to SM200

Contrast Control Voltage

The LCD unit has three power terminals, V_{DD}, V_{SS}, and V_0. A contrast control voltage is supplied to the terminal V_0. The panel is driven by the voltage difference between V_{DD} and V_O (i.e., V_{DD} - V_O). Figure 11 shows an example of the contrast control voltage supply circuit, in which VR is adjusted to obtain the best display quality.

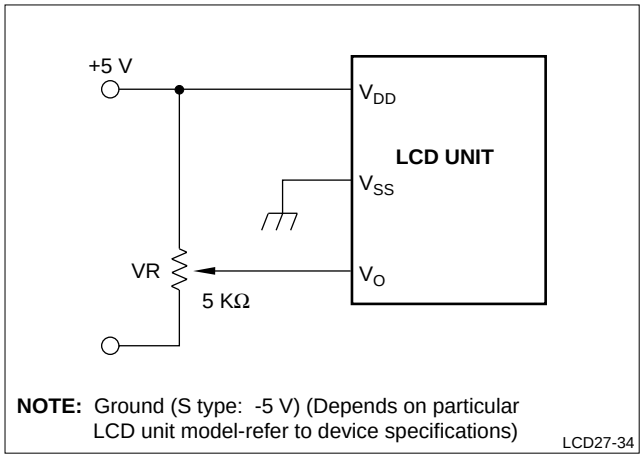


Figure 11. Contrast Adjustment Circuit

Sample Instruction Procedures

1. 8-Bit Data Transfer with a Single-Line, 16-Character Display (Using Internal Reset).

   Table 13 shows a sample operating procedure for an LCD unit in this mode. Initially, the function of the LCD unit must be selected by executing the function set instruction. Up to 80 characters may be stored in the display data RAM, and may be displayed by using the display shift operation. The contents of the display data RAM are not affected by the display shift operation, and the display/cursor home instruction enables the restoration of the initial display position.

2. 4-Bit Microprocessor

   The LCD unit can be connected to the I/O port of a 4-bit microprocessor. If the I/O port is not limited, 8-bit data may be transferred between the devices. Otherwise, 4-bit split data may be transferred in two operations, after selecting the 4-bit data length function. For the timing waveform, see Figure 9. Figure 10 shows a sample connection to an SM-200 microprocessor.

   It should be noted that the busy flag check requires a two-step operation.

3. 8-Bit Data Transfer with a Dual-Line, 16-Character Display (Using Internal Reset).

   Table 15 shows a sample operating procedure for an LCD unit in this mode. The cursor is automatically moved from the first line to the second line after column 40 of the first line has been written. In the example (Table 15), where only 16 characters are displayed on each line, the display data RAM address must be reset after the 16th character has been written. When a display shift is executed, both lines are shifted simultaneously. When the diplay shift operation is repeated, characters on one line are not moved to the other line, but rather are looped back onto the same line.

NOTE

To use the internal reset function, the power conditions must be satisfied. Otherwise, the LCD unit must be initialized by the execution of a series of instructions, as shown in the Initialization by Instructions section.

Table 13. 8-Bit Data Transfer with a Single-Line
(16-Character Display (Using Internal Reset))

NO.	INSTRUCTION	DISPLAY	OPERATION
1	Power ON (internal reset circuit is triggered).		The LCD unit is initialized. No display.
2	Function Set DS R/W DB_7 - DB_0 0 0 0 0 1 1 0 0 * *		Set for 8-bit data transfer and address type a.
3	Display ON/OFF 0 0 0 0 0 0 0 1 1 1 0		Turn on the display and cursor. After initialization, the DD RAM is filled with the "space"code.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Set the LCD unit to increment the address counter and shift the cursor to the right after each data transaction. The display does not shift.
5	CG RAM/DD RAM Data Write 1 0 0 1 0 1 0 0 1 1	S	Write "S" into the DD RAM. The cursor shifts to the right.
6	CG RAM/DD RAM Data Write 1 0 0 1 0 0 1 0 0 1	SH	Write "H" into the DD RAM.
7	⋮	⋮	⋮
8	CG RAM/DD RAM Data Write 1 0 0 0 1 0 0 0 0 0	SHARP LCD UNIT	Write "space" into the DD RAM.
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	SHARP LCD UNIT	Set display to shift after each data write.
10	CG RAM/DD RAM Data Write 1 0 0 1 0 0 1 1 0 0	HARP LCD UNIT L_	Write "L" into the DD RAM.
11	⋮	⋮	⋮
12	CG RAM/DD RAM Data Write 1 0 0 0 1 1 0 0 0 1	LCD UNIT LM171_	Write "1" into the DD RAM.
13	Display/Cursor Shift 0 0 0 0 0 1 0 0 * *	LCD UNIT LM171	Shift the cursor to the left.
14	Display/Cursor Shift 0 0 0 0 0 1 0 0 * *	LCD UNIT LM171	Shift the cursor to the left.
15	CG RAM/DD RAM Data Write 1 0 0 0 1 1 0 1 1 0	LCD UNIT LM161	Write "6" into the DD RAM.
16	Display/Cursor Shift 0 0 0 0 0 1 1 1 * *	LCD UNIT L161	Shift the display and cursor to the right.
17	Display/Cursor Shift 0 0 0 0 0 1 0 1 * *	LCD UNIT LM161_	Shift the cursor to the right.
18	CG RAM/DD RAM Data Write 1 0 0 0 1 1 0 1 0 1	LCD UNIT L1615_	Write "5" into the DD RAM.
19	⋮	⋮	⋮
20	Display/Cursor Home 0 0 0 0 0 0 0 0 1 0	SHARP LCD UNIT L	Restore the display and cursor to their initial positions.

Table 14. 4-Bit Data Transfer with Single Line

(16-Character Display (*Using Internal Reset))

NO.	INSTRUCTION	DISPLAY	OPERATION
1	Power ON (internal reset circuit is triggered).		The LCD unit is initialized. No display.
2	Function Set RS R/W DB_7 - DB_4 0 0 0 0 1 0		Set for 4-bit data transfer. This instruction is transferred in a single operation since up to this point the LCD unit is in the 8-bit mode.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Set for 4-bit data transfer and address type C. Data is transferred in two operations.
4	Display ON/OFF 0 0 0 0 0 0 0 0 1 1 1 0	_	Turn on the display and cursor. After initialization, the DD RAM is filled with the "space" code.
5	Entry Mode Set 0 0 0 0 0 0 0 0 1 1 1 0	_	Set the LCD unit to increment the address counter and shift the cursor to the right after each data transaction. The display does not shift.
6	CG RAM/DD RAM Data Write 1 0 0 1 0 1 1 0 0 0 1 1	S_	Write "S" into the DD RAM. The cursor shifts to the right.
7	:	:	:
8	CG RAM/DD RAM Data Write 1 0 0 0 1 0 1 1 0 0 0 0 0	SHARP_	Write "P" into the DD RAM.
9	DD RAM Address Set 0 0 1 1 0 0 0 0 0 0 0 0	SHARP _	Set DD RAM address to the first position on the right half of the display (character position 9).
10	CG RAM/DD RAM Data Write 1 0 0 1 0 0 1 0 1 1 0 0	SHARP L_	Write "L" into the DD RAM.
11	:	:	:
12	CG RAM/DD RAM Data Write 1 0 0 0 1 0 1 0 0 0 0 0	SHARP LCD _	Write "space" into the DD RAM.
13	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 1	SHARP LCD _	Set the display to shift after each data write.
14	CG RAM/DD RAM Data Write 1 0 0 1 0 1 1 0 0 1 0 1	HARP CD U_	Write "U" into the DD RAM. Right and left halves of display shift left one character.
15	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0	HARP CD U_	Set the LCD unit to increment the address counter and shift the cursor to the right after each data transaction. The display does not shift.
16	DD RAM Address Set 0 0 1 0 0 0 0 0 1 0 0 0	HARP _CD U	Set DD RAM address to the 9th position on the left half of the display (address 08H)
17	CG RAM/DD RAM Data Write 1 0 0 1 0 0 1 0 1 1 0 0	HARP LCD U	Write "L" into the DD RAM.
18	DD RAM Address Set 0 0 1 1 0 0 0 0 0 1 0 1	HARP LCD U_	Set DD RAM address to the 6th position on the right half of the display (address 45H)
19	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 1	HARP LCD U_	Set the display to shift after each data writer.
20	:	:	:
21	CG RAM/DD RAM Data Write 1 0 0 1 0 1 1 0 0 1 0 0	P LCD UNIT_	Write "T" into the DD RAM.
22	:	:	:
23	Display/Cursor Home 0 0 0 0 0 0 0 0 0 0 1 *	SHARP LCD UNIT	Restore the display and cursor to their initial positions.

Table 15. 8-Bit Data Transfer with Dual-Line
(16-Character Display (Using Internal Reset))

NO.	INSTRUCTION	DISPLAY	OPERATION
1	Power ON (Internal reset circuit is triggered).		The LCD unit is initialized. No display.
2	Fuction Set DD R/W DB_7 - DB_0 0 0 0 0 1 1 1 0 * *		Set for 8-bit data transfer and address type b.
3	Display ON/OFF 0 0 0 0 0 0 1 1 1 0		Turn on the display and cursor. After initialization, the DD RAM is filled with the "space" code.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Set the LCD unit to increment the address counter and shift the cursor to the right after each data transaction. The display does not shift.
5	CG RAM/DD RAM Data Write 1 0 0 1 0 1 0 0 1 1	S_	Write "S" into the DD RAM. The cursor shifts to the right.
6	⋮	⋮	⋮
7	CG RAM/DD RAM Data Write 1 0 0 0 1 0 0 0 0 0	SHARP LCD UNIT	Write "space" into the DD RAM.
8	DD RAM Address Set 0 0 1 1 0 0 0 0 0 0	SHARP LCD UNIT	Set DD RAM address to the first position of the second line.
9	CG RAM/DD RAM Data Write 1 0 0 1 0 0 1 1 0 0	SHARP LCD UNIT L	Write "L" into the DD RAM.
10	⋮	⋮	⋮
11	CG RAM/DD RAM Data Write 1 0 0 1 0 0 0 0 0 1	SHARP LCD UNIT LM16251 : 16CHA	Write "A" into the DD RAM.
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	SHARP LCD UNIT LM16251 : 16CHA	Set the display to shift after each data write.
13	CG RAM/DD RAM Data Write 1 0 0 1 0 1 1 0 0 1	SHARP LCD UNIT M16251 : 16CHAR	Write "R" into the DD RAM. Both lines shift to the left.
14	⋮	⋮	⋮
15	Display/Cursor Home 0 0 0 0 0 0 0 0 1 0	SHARP LCD UNIT M16251 : 16CHAR	Restrore the display and cursor to their initial positions.

HANDLING INSTRUCTIONS

1. Operate the LCD unit within the allowable ranges of temperature and power supply voltage. Avoid operating the LCD unit in high humidity. Avoid operating the LCD unit for extended periods under direct sunlight.

2. Mechanical shock and pressure on the glass LCD panel should be avoided. Care must be taken to insure that no torsional or compressive forces are applied to the LCD unit when it is mounted. If leakage of the liquid crystal material should occur, all contact with the material, particularly accidental ingestion, must be avoided. If the body or clothing become contaminated by the liquid crystal material, wash thoroughly with water and soap.

3. The reflector and polarizers attached to the LCD unit are made of soft materials. Care must be taken not to scratch these materials. To clean the display, use a soft, dry cloth. Do not use organic solvents or water. If dirt can not be removed by this method, a small amount of petroleum benzine may be used.

4. The LCD unit uses CMOS LSI's. Precautions must be taken to protect the unit from electrostatic charges.

5. Do not apply the power supply voltages to the LCD unit while the input signal terminals are open. Also, it is better if the input signal and LCD unit power supply voltages are switched on and off simultaneously.

6. The LCD unit should be stored in its original packing case at a temperature of 0 to 35°C and at a relative humidity of 60% or less. The LCD unit should be stored in a dark place, not exposed to direct sunlight or fluorescent lamps.

7. The following precautions should be taken when mounting the LCD unit.

a. The LCD unit may be mounted on either the inside or outside of a cabinet, as shown in Figure 12. To determine the optimum mounting angle, refer to the viewing angle range in the device specification for each model.

b. An acrylic sheet, or the like, may be used to protect the LCD panel. A spacing of 0.5 mm to 1.0 mm should be used between the protective plate and the LCD panel. (See Figure 13.)

   To prevent stress on the LCD panel, the unit should be mounted with a nominal height accuracy of ±0.1 mm.

c. An anti-glare (anti-reflection) sheet may be used in place of the protective acrylic sheet. The mounting considerations will be the same.

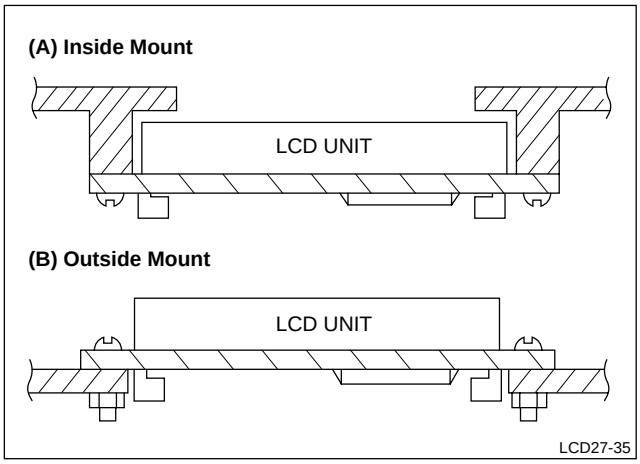


Figure 12. Mounting Diagrams

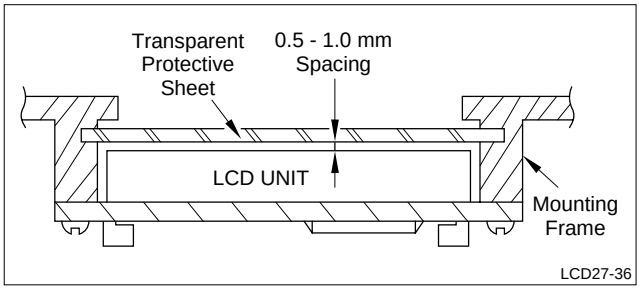


Figure 13. Sample Design

OPERATING RESTRICTIONS

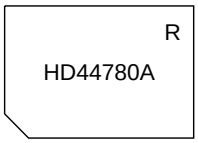
The LSI (HD44780AXX) used in the LCD units is reported to have the following defects:

HD44780AXX Defective Functions

1. When the display clear or display/cursor home instruction is executed when the display has been shifted from its original position, original display position may not be restored.
2. When the display/cursor home instruction is executed, the data in the following display data RAM locations may be lost.

To counteract these defects. The following restrictions should be followed (Table 16).

In the production facility, the LSI device in question is now being replaced with a modified version, HD44780RAXX. The above mentioned restrictions do not apply to products using the "RA" version of the LSI. The "RA" version devices have an "R" printed in the upper, right corner, as shown.



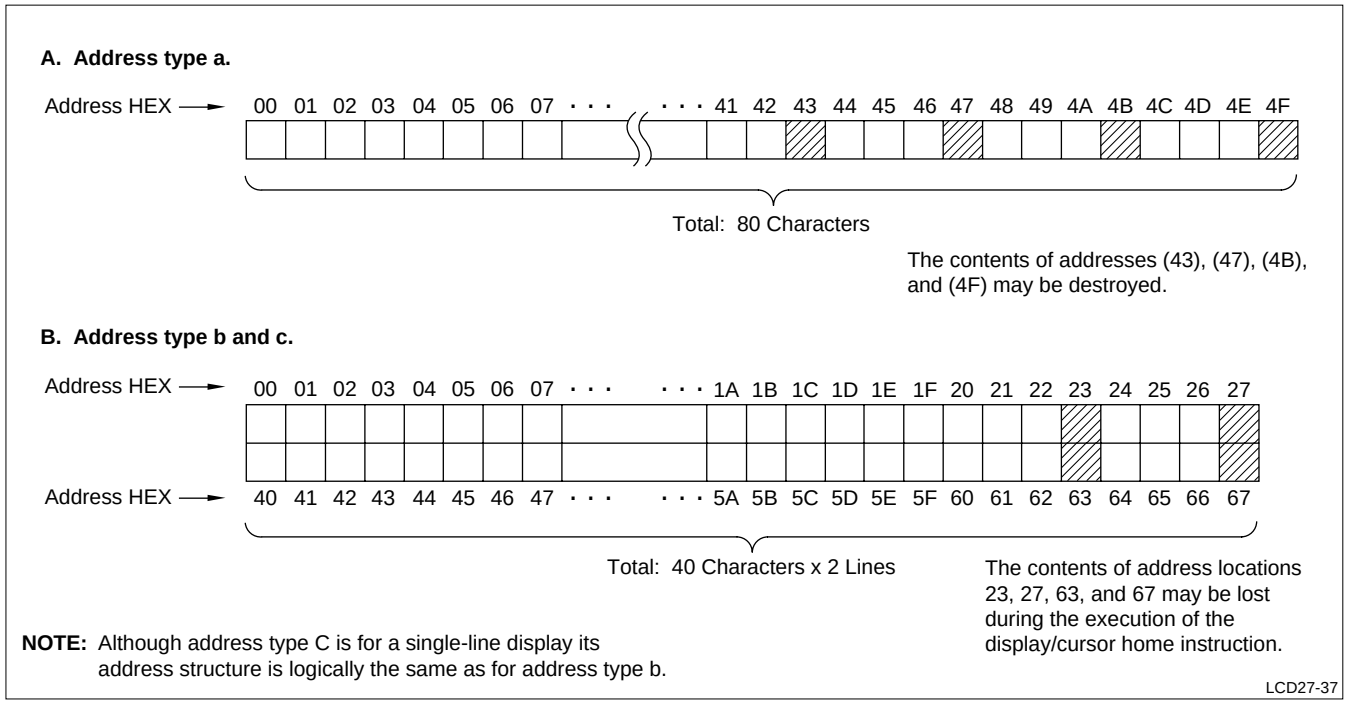


Table 16.

NO.	OPERATION		RESTRICTION
1	Execution of the display clear or display/cursor home instruction when the display has been shifted from its original position.		The display/cursor home instruction should be executed after the defective instruction, but after a time interval not equal to any multiple of 400/f_{OSC} (kHz) seconds. Since f_{OSC} = 250 kHz, the following timing intervals should be avoided: 1.6 seconds, 3.2 seconds, 4.8 seconds, etc.
2	Execution of the display/cursor home instruction.	In the case of address type a, when DD RAM address locations 43, 47, 4B, and 4F are in use.	Before executing the display/cursor home instruction, the data in the four address locations in question should be saved elsewhere by the microprocessor. After execution of the display/cursor home instruction, the data may be restored to the DD RAM.
		In the case of address types b and c, when DD RAM address locations 23, 27, 63, and 67 are in use.	

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