SL11H/T

USB Host/Slave Controllers

Technical Reference

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CONVENTIONS

1,2,3,4	**Numbers without annotations are decimals**
Dh, 1Fh, 39h	**Hexadecimal numbers are followed by an "h"**
0101b, 010101b	**Binary numbers are followed by a "b"**
bRequest, n	**Words in italics indicated terms defined by USB Specification or by this specification**

DEFINITIONS

USB	**Universal Serial Bus**
SL11H/T	**SL11H/T is a ScanLogic USB Host/Slave Controller, providing multiple functions on a single chip. The SL11H is available in both a 28-pin PLCC package, and a 48-pin LPQFP package (SL11HT).**
SL11H/T	**SL11H/T refers to both the SL11H and SL11HT.**
	Note: This chip does not include a CPU.

REFERENCES

[Ref 1] USB Specification 1.1: http://www.usb.org

REVISION HISTORY

Name and Version	Date Issue	Comments
First Draft	April 4, 1996	SL11H/T Specification Preliminary
Second Draft	May 25, 1996	Second SL11H/T Specification Preliminary
Rev 0.0 … 0.1	March 12, 1998	SL11H/TRev 0.0 to 0.1 (Internal Use)
Rev 0.2	May 27, 1998	Update from Rev 0.1
		Add Software application notes
Rev 0.3	July 20, 1998	Update from Rev 0.2
		Add 28-Pin PLCC chip dimension
Rev 1.12	March 25, 1999	Update from Rev 1.1
		Add 48 MHz crystal circuit
		Add 48-Pin LPQFP (SL11H/T) chip dimension
		Add 48-Pin description
		Add Software API Software Packet
Rev 1.14	August 31, 1999	Update from Rev 1.12
		Merged SL11 and SL11H/T Specification
Rev 1.15	January 24, 2000	3.3V power source
Rev 1.16	February 8, 2000	Update from Rev 1.15
Rev 1.17	February 17, 2000	Update from Rev 1.16

1. INTRODUCTION

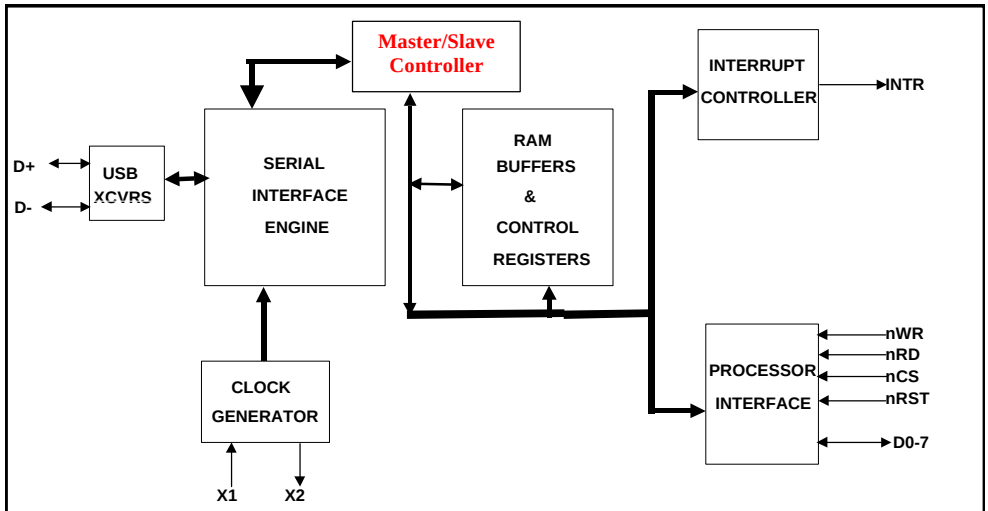
1.1 Overview

The SL11H/T is a single chip, USB embedded host/slave peripheral controller. The SL11H/T supports only full speed USB communication. In host mode, the SL11H/T acts as a USB Master or "host." In Host mode, a device becomes the host to other USB peripherals. One example of a host application is a Set-Top Box. The SL11H/T lets you attach a USB peripheral to the host to print an invoice or television program details. Another example is embedding the SL11H/T into a Personal Digital Assistant (PDA) allowing it to communicate with an external USB storage device, printer or scanner. In Slave mode, the peripheral becomes a slave device allowing it to communicate with a USB host PC. The SL11H/T includes built-in SIE and USB full-speed transceivers and runs at 12 Mbits/sec. The SL11H/T USB Host Controller is designed to conform to full-speed USB Specification 1.1

The SL11H/T can interface to any microprocessor, micro controller, or DSP. It can also interface directly to a variety of buses including ISA, PCMCIA and others through its 8-bit bi-directional Data port and through the following control signals - CS, WR, RD, INTR, and A0. Both INTEL and MOTOROLA buses, and others like them, are supported.

Internally, the SL11H/T contains a 256-byte RAM data buffer. It is used for the control registers and the data buffer. SL11H/T comes in two packages - 28-pin PLCC (SL11H) and 48-pin LPQFP. Both products can run at 3.3 or 5VDC. In both power requirements, the interface logic can run at either 3.3V or 5V.

1.2 Block Diagram



SL11H/HT USB Host Controller Functional Block Diagram

1.3 SL11H/T Host or Slave mode selection [Master/Slave mode]

The SL11H/T supports both Host and Slave mode. These modes are selectable by a single pin that can be permanently connected to the ground for the Host mode or left unconnected for the Slave mode. You also have the option to connect the pin to the GPIO pin of another CPU and have the software select the USB Host/Slave modes. This document describes the specifics of using SL11H in Host mode. For details on Slave mode, please refer to the SL11/T specification.

1.4 Features

- The only low cost USB host/slave controller for embedded systems. Available with 8-bit general-purpose interface and control signals; interfaces to any CPU, DSP or bus.
- Supports full speed (12Mbit/sec) USB transfers in both Host and Slave modes

USB Specification Compliance

- Conforms to USB Specification 1.1

CPU Interface

- Supports Host or Slave mode
- 256 x 8 SRAM "On-Chip" memory
- 8 bit Bi-directional Data Port, interfaces to any external Bus or CPU (Intel, Motorola, etc.)
- ALE Multiplexed bus support (optional)
- On-Chip full speed USB transceivers
- 3.3V (optional 5V) power source, CMOS Technology
- Logic interface 3 or 5 Volt tolerant
- Memory buffer includes Double buffer Ping Pong operation scheme
- Single 48MHz crystal.
- Auto Address increment mode to simplify memory access and improve performance
- Available in 28 Pin PLCC or 48 TPQFP packages

1.5 Data Port, Interface to external Micro-Processor

The SL11H/T Data Port interface provides an 8-bit bi-directional data path with appropriate control signals such as CS, RD, WR, A0 and INTR lines. This feature enables it to interface to any external processor or controller (INTEL, Motorola, TI, Analog Devices, etc.). The control Read and Write signals, Chip Select and a single address line A0, with the 8-bit data bus, support both programmed I/O or Memory mapped I/O designs.

Access to the memory and control register space is a simple two step process, requiring an address write with A0 set to '0' followed by a register/memory read or write cycle with address line A0 set to '1'.

The SL11H write or read operation terminates when either nWR or nCS becomes inactive. For devices interfacing to the SL11H/T that deactivate the Chip Select nCS before the write nWR, the data hold timing should be measured from the nCS and will be the same value as specified. Thus both Intel and Motorola type CPUs work well with SL11H/T without any external glue logic required.

In applications where multiplexed address/data bus support is required, the SL11H/T utilizes an ALE (Address Latch Enable) control input to de-multiplex the data bus by latching the register/memory address from the 8 bit data bus when the ALE input strobe is high. Data is written to, or read from the SL11H/T with chip select and the appropriate control strobe asserted. In multiplexed applications A0 is not used and must be tied to VCC. Data transfers from/to the CPU bus can be accessed at above 10 Mbytes/sec rate.

1.6 Interrupt Controller

The SL11H/T interrupt controller provides a single output signal. The INTR can be activated by a number of events that may occur as result of an USB activity. Control and status registers are provided to allow you to select single or multiple events that will generate an interrupt (assert INTR), and provides a means of viewing the interrupt status. The interrupt can be cleared by writing to the Status Register located in the internal register space at address 0x0d.

1.7 Buffer Memory

The SL11H/T contains 256 bytes of internal buffer memory. The first 16 bytes of memory represent control and status registers for programmed I/O operations. The remaining memory locations are used for data buffering (max 240 Bytes).

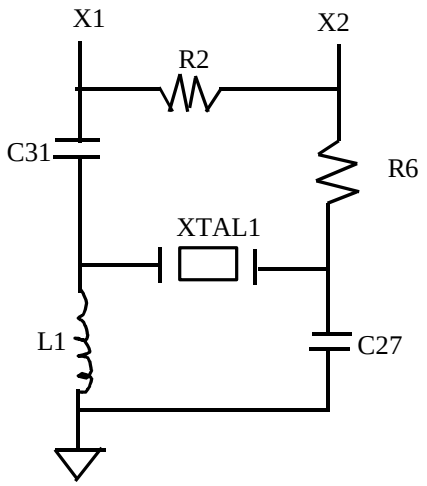
Access to the registers and data memory is done by an external microprocessor through the 8-bit data bus. This can be in either of two addressing modes; indexed or direct access, if used with multiplexed address/data bus interfaces. With indexed addressing, the address is first written into the device with the A0 address line low, then

the following cycle with A0 address line high is directed to the specified address. In multiplexed address/data bus applications, a single cycle beginning with ALE asserted high latches the address internally, then the read or write strobe accesses the specified location. Address A0 is not used in multiplexed address/data bus interfaces and must be tied to VCC. USB transactions are automatically routed to the memory buffer. Control registers are provided, so that you have the ability to set up pointers and block sizes in buffer memory.

1.8 PLL Clock Generator

A 48 MHz external crystal can be used with the SL11H/T. Two pins, X1 and X2, are provided to connect a low cost crystal circuit to the device, refer to Fig 2. If an external 48 MHz clock source is available in the application, it may be used instead of the crystal circuit by connecting directly to the X1 input pin.

Full-Speed 48MHz Crystal Circuit



Resistors and capacitor value:

- R2 = 1Mega Ohms
- R6 = 100 Ohms
- C31 = 0.01 uF
- C27 = 20pF
- L1 = 3.3 uH
- XTAL1 = 48Mhz, series, 20pF load capacitance.

1.9 USB Transceiver

The SL11H/T has a built-in transceiver, which meets USB Specification 1.1. The transceiver is capable of transmitting and receiving serial data at the USB full speed (12 Mbits/sec) data rate. The driver portion of the transceiver is differential, while the receiver section is a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the SIE logic. Externally the transceiver connects to the physical layer of the USB.

1.10 SL11H/T Registers

You operate the SL11H/T through the SL11H/T 16 internal registers. A portion of the internal RAM is devoted to the register space and access, which is accessible through the microprocessor interface. The registers provide control and status information for transactions on the USB, microprocessor interface and interrupts.

Register Name SL11H	SL11H (hex) Address
USB Host Control Register	00H
USB Host Base Address	01H
USB Host Base Length	02H
USB Host PID, Device Endpoint (Write)/USB Status (Read)	03H
USB Host Device Address (Write)/Transfer Count (Read)	04H
Control Register1	05H
Interrupt Enable Register	06H
Reserved Register	07H
Reserved Register	Reserved
Reserved Register	Reserved
Reserved Register	Reserved
Reserved Register	Reserved
Reserved Register	Reserved
Status Register	0DH
Revision Register (Read)	0EH
Reserved Register	Reserved
Memory Buffer	10H-FFH

1.11 Auto Address Increment Mode

The SL111H supports auto increment mode to reduce read and write memory cycles. In this mode, the Micro Controller needs to setup the address only once. Whenever any subsequent DATA is accessed, the internal address counter will advance to the next DATA set.

Once the address of the starting location has been set the write operations will write the data bytes in consecutive locations. For example, assume the value Index1 was written into the Address register of SL11H during the Address cycle (with the A0 input set low). Then the write operations in the data cycle (with A0 input set high) will write the data bytes into the sequential internal memory locations Index1, Index1 + 1, Index1 + 2 and so on. The Auto increment mode also works on the read from SL11H operations. After setting the address of the starting location once the read operations will read the subsequent internal memory locations.

For example

Write 0x10 to SL11H/T in address cycle (A0 is set low)

Write 0x55 to SL11H/T in data cycle (A0 is set high) -> write 0x55 to location 0x10

Write 0xaa to SL11H/T in data cycle (A0 is set high) -> write 0xaa to location 0x11

Write 0xbb to SL11H/T in data cycle (A0 is set high) -> write 0xbb to location 0x12

The auto increment mode decreases the total time needed to transfer the block of data into or from the internal memory of the SL11H controller. It eliminates the need to set the address fo4r each byte to be transferred. The advantage of this mode is that it reduces the memory read or write cycles.

For example, transferring 64 bytes of data to or from SL11H will be reduced by 80ns*63. The total time will be 1 address cycle + 64 Data cycles. Without auto increment mode it will be 64 address cycles + 64 data cycles. This time saving is because the address write cycle to the SL11H/T chip is skipped.

2. SL11H/T REGISTERS

The registers in the SL11H/T are divided into two major groups. The first group contains USB control registers. They control USB control transactions and data flow. The second group is the primary SL11H memory interface to external Micro Controller registers that provides the control and status information for all other operations.

2.1 USB Control Registers

The USB Control registers control communication and data flow on the USB. These uniquely identifiable entities are the terminals of communication flow between a USB host and USB devices. Each USB device/slave is composed of a collection of independently operating endpoints. Each endpoint has a unique identifier, which is the Endpoint Number. For more details about USB endpoints please refer to the USB Specification 1.1. Section 5.3.1.

The SL11H/T can communicate to any USB Device with any type of configuration or functions including any specific endpoints via the USB control registers. The SL11H/SL11T can address up to 127 devices and 16 endpoints.

The SL11H/T has five registers, which are mapped in the SL11H/T memory. These registers are described in the table below:

Register Name SL11H/HT	SL11H/HT (hex) Address
USB Host Control Register	00H
USB Host Base Address	01H
USB Host Base Length	02H
USB Host PID, Device Endpoint (Write)/USB Status (Read)	03H
USB Host Device Address (Write)/Transfer Count (Read)	04H

2.2 CRC5 and SOF

The USB Specification 1.1 requires a host controller to generate a Start of Frame (SOF) token at regular timed intervals, nominally every 1 millisecond. SOF packets consist of PID, an eleven-bit frame number, and a 5-bit CRC. For the details please refer to the Section 8.4.2 of USB Specification 1.1. The USB Hub specification Section 11.2.2 applies to external Hubs, and not to a host, but does expect that the host generates SOF within the specified limits set in Section 8.4.2.

The SL11H USB Host Controller requires an external micro controller to generate and track SOF frame number. Since the SOF frequency specification requires a SOF token to be generated every 1 msec (+/- 500 nsec), the micro controller timer should be used to generate an interrupt at a 1-millisecond interval. The timer interrupt should be set as the highest priority interrupt.

The execution of the interrupt service routine will always be constant, so the critical time is the interrupt latency of the particular micro controller in the application. Interrupt latency time is typically much lower than the +/- tolerance specified for SOF generation. Setting the timer value to interrupt at the minimum of the SOF time specification will give the user a maximum interrupt latency of 1 microsecond.

All our present customers currently using the SL11H in many and various applications have no difficulty in meeting this USB Specification 1.1 timing requirement.

2.2.1 SL11H/T SOF and CRC5 Software Generation by External CPU

The SL11H SOF generation requires the user to maintain and update the SOF Frame Number and calculate CRC5 value in the target micro controller. To make the fastest interrupt service routine possible, the Frame number and CRC for the next frame can be pre-calculated so that the service routine is only required to write the new values to the SL11H.

When SOF is not send to a device within 3msec the external peripheral might place itself in to suspend mode. If this happens, it is the host's responsibility to wake this peripheral. You need to select a CPU that has Interrupt latency response within 1.5usec.

Note: Latency is defined as the time from interrupt was received from the SL11H until the time the first instruction on an external CPU is executed. The USB Specification for a hub defines that this time can be 9x83x2=1494nsec or 1.5usec.

2.2.2 Next Generation of SL11H/T family

The new chip for SL11H/T will be the SL811H/SL811HT. It generates both CRC5 and SOF internally. You will not need to generate Software CRCs or SOF. Furthermore the SL8111H/SL811HT chip is pin and functionally backward compatible with the current SL11H/SL811HT. The SL811H/SL811HT has no limitations on interrupt latency, so the speed of the external CPU is irrelevant. The SL811H/SL811HT also includes support for the Master/Slave modes for both low speed and full-speed devices. Please contact ScanLogic for additional information about the SL811H.

2.2.3 USB Host Control Register [00X]

Each USB transaction has a control register.

Bit Position	Bit Name	Function
0	Arm	Allows enabled transfers when set ='1'. Cleared to '0' when transfer is complete.
1	Enable	When set = '1' allows transfers to this endpoint. When set "0 USB transactions are ignored. If Enable = '1' and Arm = '0' the endpoint will return NAK's to USB transmissions.
2	Direction	When set = '1' transmit to Host. When '0' receive from Host.
3	Reserved	
4	ISO	When set to '1' allows Isochronous mode for this endpoint.
5	Reserved	
6	Sequence	Sequence Bit. '0' if DATA0, '1' if DATA1.
7	Reserved	

- **SL11H/T initiate USB packet transfer:**

  One byte PID and two bytes for CRC5 need to be included in the memory buffer. For example, using the SL11H memory setup:

40h	PID
41h	CRC5 low byte (These two CRC5 bytes contain information of Device Endpoints and Device Address)
42h	CRC5 high byte
43h-82h	USB Data, depend on the PID.

  CRC5 must be pre-computed by software. See the sample code

  The memory data can be pre-copied prior to the setup of the ARM bit on this register. Users can use the Ping-Pong scheme by reserving additional memory locations before the transfer. The USB Host "Base Address " and USB Host "Base Length" can be reprogrammed to adapt the Ping-Pong operation. See the code example.

Examples of PID:

PID_SETUP	2DH
PID_SOF	A5H
PID_IN	69H
PID_OUT	E1H
PID_PRE	3CH
PID_NAK	5AH
PID_STALL	1EH
PID_DATA0	C3H
PID_DATA1	4BH

2.3 Example - USB transaction to transfer 128-bytes of data to a Peripheral:

SL11H/SL11T memory allocation

10H-52H is buffer A
Where:

10h	PID=E1
11h	CRC5 low byte (These two CRC5 bytes contain information of Device Endpoints and Device Address)
12h	CRC5 high byte
13h-52h	64-byte of USB Data, depend on the PID.

53H-95H is buffer A
Where:

53h	PID=E1
54h	CRC5 low byte (These two CRC5 bytes contain information of Device Endpoints and Device Address)
55h	CRC5 high byte
56h-95h	64-byte of USB Data, depend on the PID.

2.3.1 USB Host Base Address [01H]

The USB Base Address is a Pointer to the SL11H/T memory buffer location for USB reads and writes. To transfer data OUT (Host to Device) the data to be transferred must be pointed to the base address location and it can be copied prior to setting the ARM bit on the USB Host Control register. For more details please refer to the application source code example.

2.3.2 USB Host Base Length [02H]

There is a maximum transfer packet size of data between the SL11/SL11HT and other slave USB devices (this designates the largest packet size that can be transferred by the SL11H/T). For Transfers to/from an external USB slave device, the Base Length register designates the size of data packet to be sent. For example, in Bulk mode, the maximum packet length size is 64-bytes. In ISO mode, the maximum packet length is 1023. The maximum packet size for the SL11H/T ISO mode is 240 bytes (256 bytes minus 16 bytes). When the Host Base Length is set to zero, then a Zero-Length packet will be transferred.

2.3.3 USB Host Packet Status READ [03H]

The packet status contains information about the packet that has been received or transmitted.

Bit Position	Bit Name	Function
0	ACK	Transmission Acknowledge.
1	Error	Error detected in transmission.
2	Time-out	Time-out occurred.
3	Sequence	Sequence Bit. '0' if DATA0, '1' if DATA1.
4	Setup	'1' indicates Setup Packet
5	Overflow	Overflow condition - maximum length exceeded during receives.
6	NAK	Slave returns NAK
7	STALL	Slave set STALL bit

2.3.4 USB Host Transfer Count Register [04H]

Software should set this register to zero before the ARM bit is set in the USB Host Control register. This register will return the actual number of bytes transferred from/to the host.

2.4 SL11H/T other Control/Status Registers

In addition to the USB Host Control Registers, the SL11H/T contains a number of other registers which provide control and status functions.

2.5 Register Address Assignments

Register Name	Address (in Hex)
Control Register	05 H
Interrupt Enable Register	06 H
USB Address Register	07 H
Interrupt Status Register	0D H
Current Data Set Register	0E H

The SL11H/T primary interface to external CPU and internal memory buffer includes 5 control registers that provide the control and status information for all other operations of the SL11H/T, and memory allocation 10H to FFH.

2.5.1 Control Register, Address [05H]

The Control Register enables/disables USB transfers operation with control bits.

Bit Position	Bit Name	Function
0	USB Enable	Overall Enable for transfers. '1' enables, '0' disables.
3	USB Engine Reset	USB Engine reset = '1'. Normal set '0'
1-2,4-7	Reserved	Reserved bits - all must be set to '0' 's.

Note: Bit-0 should be set '1' to allow USB communication. The default is zero on power up

2.5.2 Interrupt Enable Register, Address [06H]

The SL11H/T provides an Interrupt Request Output, which can activate on a number of conditions. The Interrupt Enable Register allows the user to select activities that will generate the Interrupt Request. A separate Interrupt Status Register is provided. It can be polled in order to determine the condition, which initiated the interrupt. (See Interrupt Status Register description). When a bit is set to '1' the corresponding interrupt is enabled.

Bit Position	Bit Name	Function
0	USB Done	USB transfer done
1	Reserved	
2	Reserved	
3	Reserved	
4	Reserved	
5	Reserved	
6	USB Reset	USB Reset received interrupt.
7	Reserved	

2.5.3 USB Address Register, Address [07H]

This is a reserved register.

2.5.4 Interrupt Status Register, Address [0DH]

This Read/Write register serves as an interrupt status register when it is read, and an Interrupt clear register when it is written. To clear an interrupt bit, the register must be written with the appropriate bit set to '1'. Writing a '0' has no affect on the status.

Bit Position	Bit Name	Function
0	USB Done	USB transfer done
1	Reserved	
2	Reserved	
3	Reserved	
4	Reserved	
5	Reserved	
6	USB Reset	USB Reset received interrupt.
7	Reserved	

2.5.5 Current Data Set Register/Revision Register, Address [0EH]

This read-only register indicates currently selected data set for each endpoint.

Bit Position	Bit Name	Function
0	USB Data toggle pin	Reflection of the DATA0 or DATA1
1	Reserved	
2	Reserved	
3	Reserved	
4-7	Revision	Return zero value

3. SL11H / SL11HT PHYSICAL CONNECTION

The diagrams below indicate pin assignments for the SL11H 28-pin PLCC Package.

3.1 SL11H Pin Layout

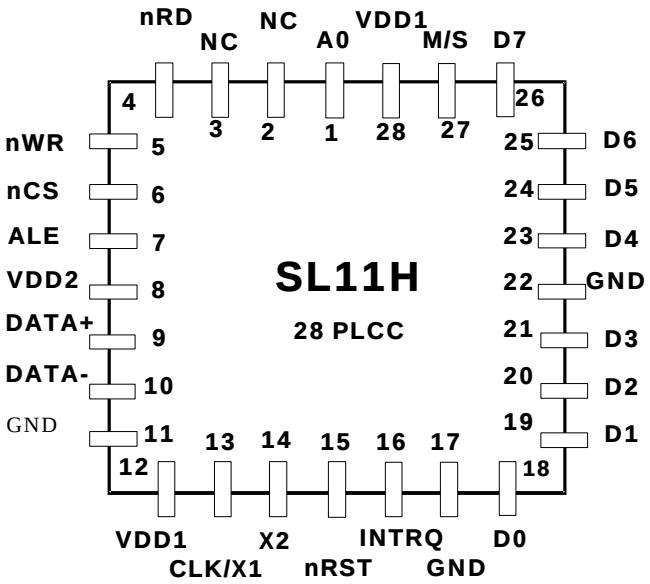
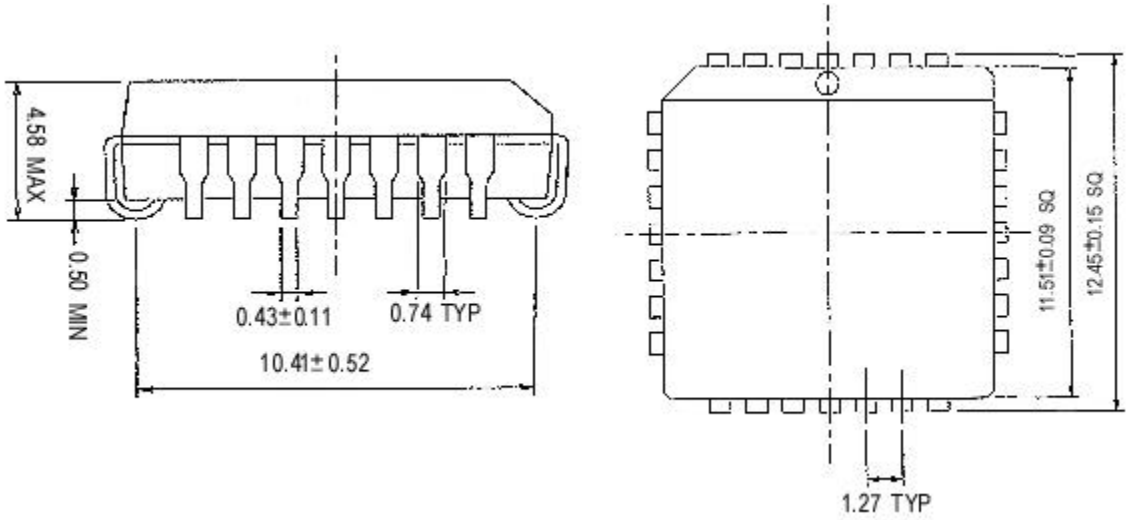


Figure 1 SL11H USB Host Controller - Pin layout

3.2 28-PIN PLCC Mechanical Dimensions



3.3 SL11H USB Host Controller Pins Description

The SL11H package is a 28-pin PLCC. The device requires a 3.3VDC (optional +5 VDC on VDD1) power supply, and a +3.3 VDC (VDD2) power supply for the USB transceiver. Average typical current consumption is less than 22 mA for 3.3V. The SL11H requires an external 48 MHz crystal or Clock.

Pin No.	Pin Type	Pin Name	Pin Description
1	IN	A0	A0 = '0'. Selects Address Pointer. Reg. Write Only. Note[1] A0 = '1'. Selects Data Buffer or Register. R/W. In Multiplexed address applications, AO should be tied to VDD1.
2	IN	NC	Pin must be left unconnected
3	OUT	NC	Pin must be left unconnected
4	IN	nRD	Read Strobe Input. An active low input used with nCS to read registers/data memory.
5	IN	nWR	Write Strobe Input. An active low input used with nCS to write to registers/data memory.
6	IN	nCS	Active low SL11H Chip select. Used with nRD and nWD when accessing SL11H.
7	IN	ALE	Address Latch Enable. Used to De-Multiplex 8 bit Address/Data Bus. Note [2]
8	VDD2	3.3 VDC	Power for USB Transceivers. VDD2 may be derived from VDD1. Note [3]
9	BIDIR	DATA +	USB Differential Data Signal High Side.
10	BIDIR	DATA -	USB Differential Data Signal Low Side.
11	GND	USB GND	Ground Connection for USB.
12	VDD1	3.3V or 5 VDC	SL11H Device VDD Power.
13	IN	CLK/X1	48 MHz Clock or External Crystal X1 connection.
14	OUT	X2	External Crystal X2 connection.
15	IN	nRST	SL11H Device active low reset input.
16	OUT	INTRQ	Active high Interrupt Request output to external controller.
17	GND	GND	SL11H Device Ground
18	BIDIR	D0	Data 0. Microprocessor Data/(Address) Bus. [3]
19	BIDIR	D1	Data 1. Microprocessor Data/(Address) Bus. [3]
20	BIDIR	D2	Data 2. Microprocessor Data/(Address) Bus. [3]
21	BIDIR	D3	Data 3. Microprocessor Data/(Address) Bus. [3]
22	GND	GND	SL11H Device Ground.
23	BIDIR	D4	Data 4. Microprocessor Data/(Address) Bus. [3]
24	BIDIR	D5	Data 5. Microprocessor Data/(Address) Bus. [3]
25	BIDIR	D6	Data 6. Microprocessor Data/(Address) Bus. [3]
26	BIDIR	D7	Data 7. Microprocessor Data/(Address) Bus. [3]
27	M/S	Host/Slave	Host="0", Slave = "1" configuration pin.
28	VDD1	3.3V or 5 VDC	SL11H Device VDD Power.

Notes:

1- The A0 Address bit is used to access address register or data registers in I/O Mapped or Memory Mapped applications. If the SL11H is interfaced to a multiplexed address/data bus, A0 should be tied to VDD1.

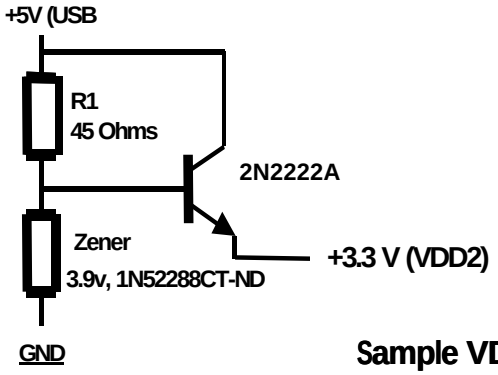
2- Only use the ALE Address Latch Enable signal with micro controller buses which require de-multiplexing Address and Data from a single 8 Bit bus. It must normally be tied low.

3- D0 - D7 normally is a data bus, but in applications, which utilize a multiplexed address/data bus, the bus will contain an address when ALE is set high.

4- VDD2 can be derived from a USB supply with a few additional components. The diagram below illustrates a simple method that provides 3.3V/22mA. Another option is to use a Torex Semiconductor 3.3V SMD regulator P/N XC62HR3302MR

5 X1/X2 Clock requires external 48MHz matching crystal or clock source.

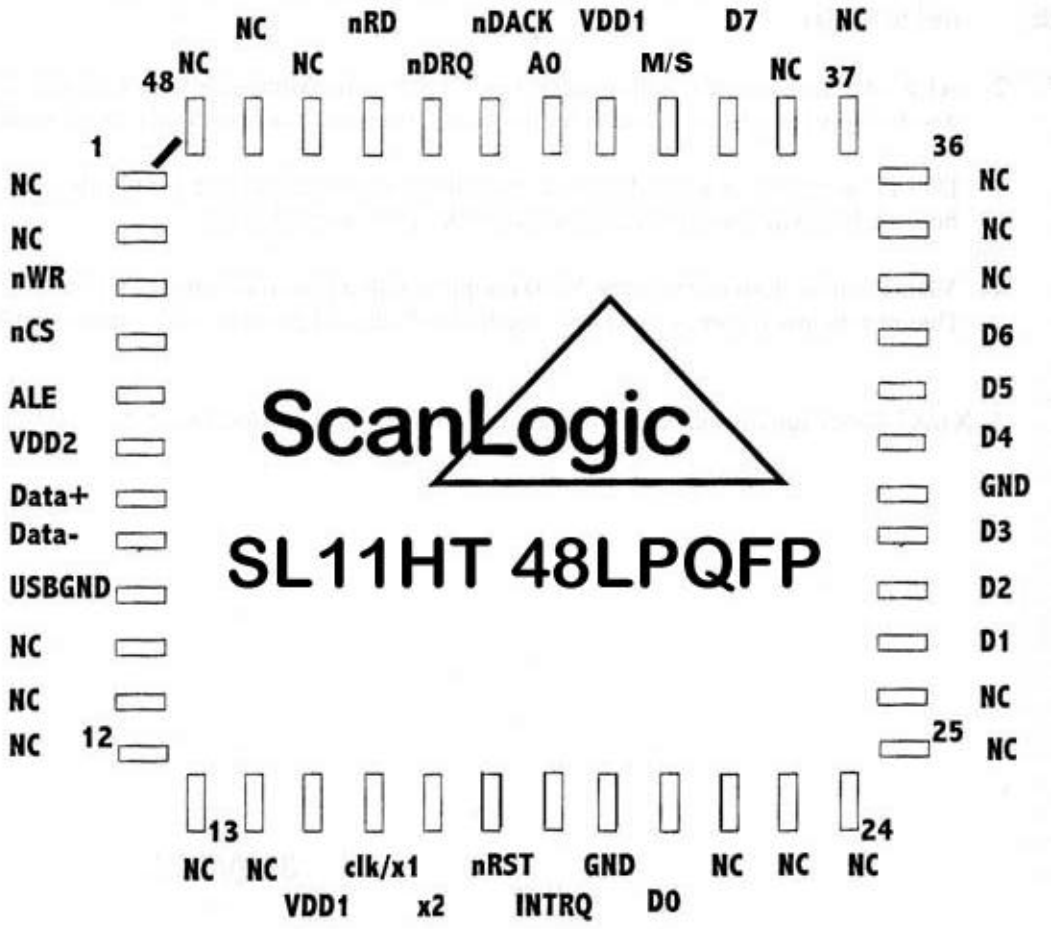
A simple 3.3V Voltage source



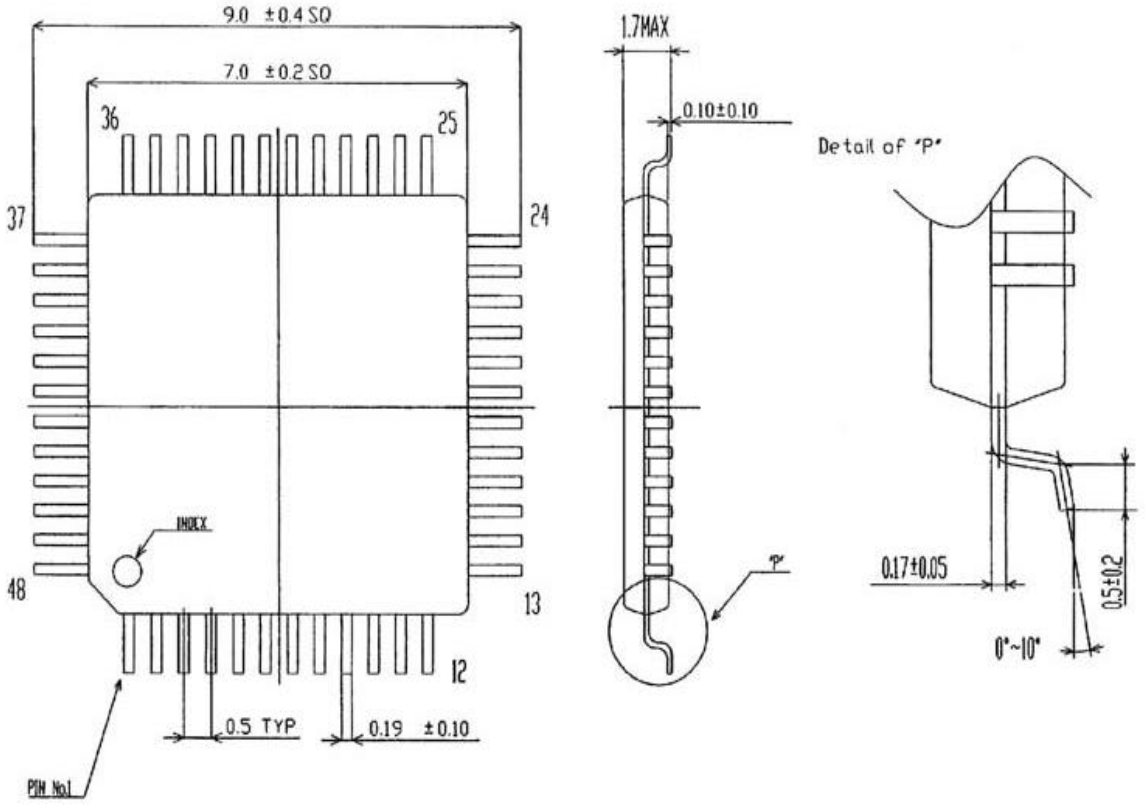
Sample VDD2 Generator

3.4 SL11HT Pin Layout

The diagrams below show the pin assignments for SL11HT 48-pin LPQFP Package.



3.5 SL11HT 48-Pin LPQFP Mechanical Dimensions



3.6 SL11HT USB Host Controller Pins Description

The SL11HT is packaged in a 48 Pin LPQFP. The device requires either 3.3VDC or +5VDC (VDD1) and a +3.3 VDC (VDD2) power supply. Average typical current consumption is less than 22 mA for 3.3V. The SL11HT requires an external 48 MHz crystal or Clock.

Pin No.	Pin Type	Pin Name	Pin Description
1	NC	NC	NC
2	NC	NC	NC
3	IN	nWR	Write Strobe Input. An active low input used with nCS to write to registers/data memory.
4	IN	nCS	Active low SL11HT Chip select. Used with nRD and nWR when accessing SL11HT.
5	IN	ALE	Address Latch Enable. Used to De-Multiplex 8 bit Address/Data Bus. Note 2
6	VDD2	3.3 VDC	Power for USB Transceivers. VDD2 may be derived from VDD1. Note 4
7	BIDIR	DATA +	USB Differential Data Signal High Side.
8	BIDIR	DATA -	USB Differential Data Signal Low Side.
9	GND	USB GND	Ground Connection for USB.
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	NC	NC	NC
14	NC	NC	NC
15	VDD1	3.3 or 5 VDC	SL11HT Device VDD Power.
16	IN	CLK/X1	48 MHz Clock or External Crystal X1 connection.
17	OUT	X2	External Crystal X2 connection.
18	IN	nRST	SL11HT Device active low reset input.
19	OUT	INTRQ	Active high Interrupt Request output to external controller.
20	GND	GND	SL11HT Device Ground.
21	BIDIR	D0	Data 0. Microprocessor Data/(Address) Bus. 3
22	NC	NC	NC
23	NC	NC	NC
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	BIDIR	D1	Data 1. Microprocessor Data/(Address) Bus. Note 3

28	BIDIR	D2	Data 2. Microprocessor Data/(Address) Bus. Note 3
29	BIDIR	D3	Data 3. Microprocessor Data/(Address) Bus. Note 3
30	GND	GND	SL11HT Device Ground.
31	BIDIR	D4	Data 4. Microprocessor Data/(Address) Bus. Note 3
32	BIDIR	D5	Data 5. Microprocessor Data/(Address) Bus. Note 3
33	BIDIR	D6	Data 6. Microprocessor Data/(Address) Bus. Note 3
34	NC	NC	NC
35	NC	NC	NC
36	NC	NC	NC
37	NC	NC	NC
38	NC	NC	NC
39	BIDIR	D7	Data 7. Microprocessor Data/(Address) Bus. 3
40	M/S	Host/Slave	Host="0", Slave = "1" configuration pin.
41	VDD1	3.3 or 5 VDC	SL11HT Device VDD Power.
42	IN	A0	A0 = '0'. Selects Addr. Pointer. Reg. Write Only. Note 1 A0 = '1'. Selects Data Buffer or Register. R/W. In Multiplexed address applications, AO should be tied to VDD1.
43	IN	NC	Pin must be left unconnected
44	OUT	NC	Pin must be left unconnected
45	IN	nRD	Read Strobe Input. An active low input used with nCS to read registers/data memory.
46	NC	NC	NC
47	NC	NC	NC
48	NC	NC	NC

Notes:

5- The A0 Address bit is used to access address register or data registers in I/O Mapped or Memory Mapped applications. If the SL11HT is interfaced to a multiplexed address/data bus, A0 should be tied to VDD1.

6- The ALE Address Latch Enable signal is used only with micro-controller buses which require de-multiplexing Address and Data from a single 8 Bit bus. It normally must be tied low.

7- D0 - D7 normally is a data bus, but in applications that utilize a multiplexed address/data bus, the bus will contain an address when ALE is set high.

8- VDD2 can be derived from the USB supply with a few additional components. The diagram below the notes in section 3.3 illustrates a simple method that provides 3.3V/22mA. Another option is to use a Torex Semiconductor 3.3V SMD regulator P/N XC62HR3302MR

9- The X1/X2 Clock requires an external 48MHz matching crystal or clock source.

4. ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

This section lists the absolute maximum ratings of the SL11H/T. Conditions outside the listed ranges can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can affect device operation and reliability.

Items	Min	Max
Storage Temperature	-40 °C	125 °C
Voltage on any pin with respect to ground	3.3V – 10%	5V +10%
Power Supply Voltage (VDD1)	3.3 V – 5%	5 V + 10%
Power Supply Voltage (VDD2)	3.3V ± 10%	3.3V ± 10%
Lead Temperature (10 seconds)	180 ^{0}C	

4.2 Recommended Operating Conditions

Parameter	Min.	Typical	Max
Power Supply Voltage, VDD1	4.75 V		5.25 V
Or, Power Supply Voltage, VDD1	3.15 V		5.25 V
Power Supply Voltage, VDD2	3.0 V		3.6 V
Operating Temperature	0°C		65°C

4.3 Crystal Requirement

Crystal Requirements, (X1, X2)	Min.	Typical	Max
Operating Temperature Range	0°C		70°C
Series Resonant Frequency		48 MHz	
Frequency Drift over Temperature			± 20 PPM
Frequency Stability, ref 25 ^{0}C			± 50 PPM: 0 ^{0}C - +70 ^{0}C
Accuracy of Adjustment			± 30 PPM
Series Resistance			100 ohms
Shunt Capacitance	3pf		6pf
Load Capacitance		20pF	
Driver Level	20microWatt		5miliWatt
Mode of Vibration 3rd overtone			

4.4 External Clock Input Characteristics (X1)

Oscillator Requirement	Min.	Typical	Max
Operating Temperature Range	0°C		70°C
Clock Input Voltage @ X1 (X2 will be Open)	4.5V		5.5V
Clock Frequency		48MHz	
Frequency Stability, ref 25 ^{0}C	- 100 PPM		+ 100 PPM

4.5 DC Characteristics

Symbol	Parameter	Min.	Typical	Max
IL	Input Voltage LOW	-0.5 V		0.8 V
V_{IH}	Input Voltage HIGH	2.0V		VDD+ 0.3V
V_{OL}	Output Voltage LOW (IoL=4ma)			0.6 V
V_{OH}	Output Voltage HIGH (IoH=-4ma)	2.4 V		
I_{OH}	Output Current HIGH	4 ma		
I_{OL}	Output Current LOW	4 ma		
C_{IN}	Input Capacitance			20 pF
I_{CC}	Supply Current (VDD1) at 48Mhz including USB	2mA		< 15mA
I_{USB}	Supply Current (VDD1)			< 10mA

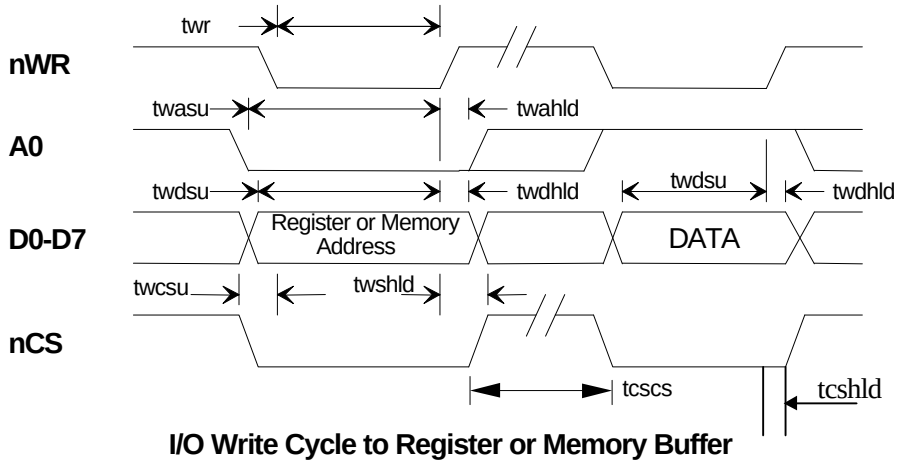
4.6 USB Host Transceiver Characteristics

Symbol	Parameter	Min.	Typical	Max
V_{IHYS}	Hysteresis On Input (Data+, Data-)	0.1 V		200 mV
V_{USBIH}	USB Input Voltage HIGH		1.5 V	2.0 V
V_{USBIL}	USB Input Voltage LOW	0.8 V	1.3 V	
V_{USBOH}	USB Output Voltage HIGH	2.2 V		
V_{USBOL}	USB Output Voltage LOW			0.7 V
Z_{USBH}	Output Impedance HIGH STATE	28 Ohms		43Ohms
Z_{USBL}	Output Impedance LOW STATE	28 Ohms		43 Ohms
I_{USB}	Transceiver Supply p-p Current (3.3V)	100mA		

Notes: 1. All typical values are VDD2 = 3.3 V and TAMB= 250 ^{0} C.
2. Z_{USBX} Impedance Values includes an external resistor of 28-43 Ohms $\pm$ 1%.

4.7 Bus Interface Timing Requirements

4.7.1 I/O Write Cycle



I/O Write Cycle to Register or Memory Buffer

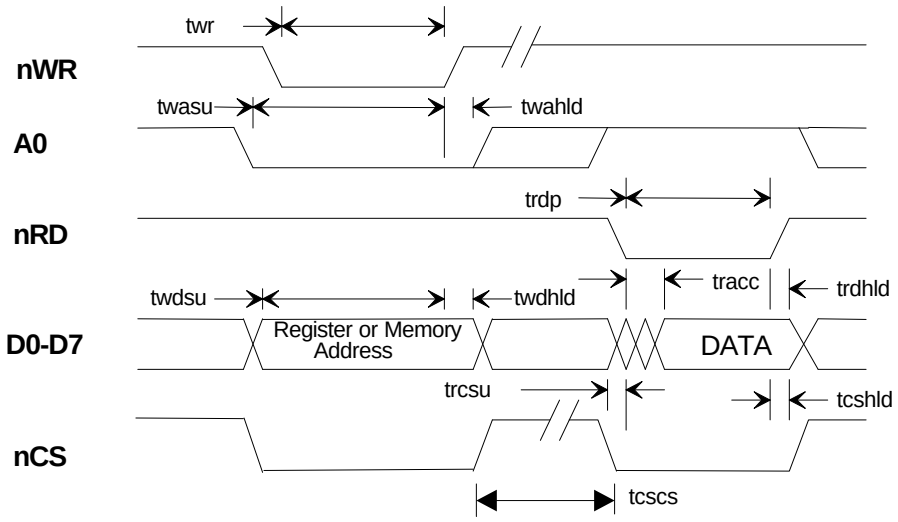
The diagram above shows the I/O Timing diagram for an I/O Write Cycle It shows the Data Hold time (twdhld) specified from the trailing edge of the Write Signal (nWR) and a Chip select nCS being removed after the write has been deactivated. The Sl11H write operation terminates when either nWR or nCS goes inactive. For devices interfacing to the SL11H that deactivate the Chip Select nCS before the write nWR, the data hold timing should be measured from the nCS and will be the same value as specified.

The end of cycle operation also applies to IO Read Cycles. That is, the cycle ends when either nRD or nCS is deactivated.

This type of timing supports Intel and Motorola CPUs, as well as DSPs from TI, Analog devices, etc.

Symbol	Parameter	Min.	Typical	Max
twr	Write pulse width	65 nsec		
twcsu	Chip select setup to nWR	10 nsec		
twshld	Chip select hold time	10 nsec		
twasu	A0 address setup time	65 nsec		
twahld	A0 address hold time	10 nsec		
twdsu	Data to write low setup time	5 nsec		
twdhld	Data hold time after write high	10 nsec		
tcsdhld	Chip select hold after write high	10 nsec		
tcscs	nCS inactive to nCS asserted	85 nsec		

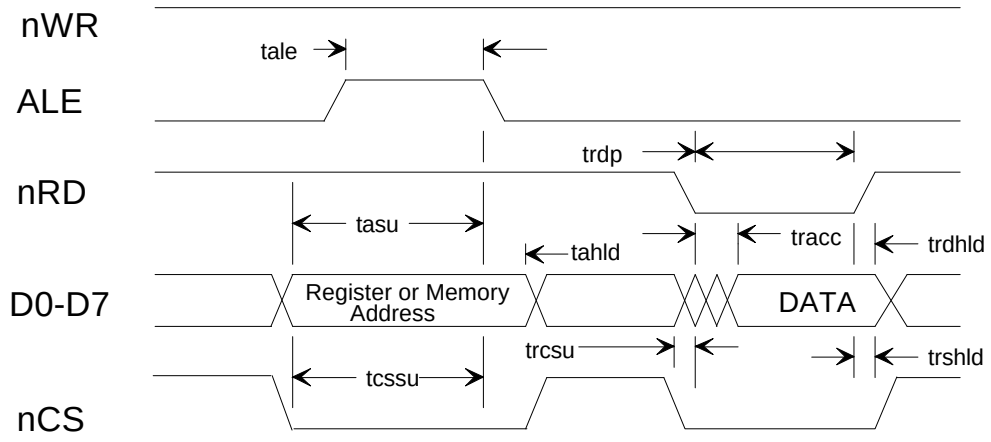
4.7.2 I/O Read Cycle



I/O Read Cycle from Register or Memory Buffer

Symbol	Parameter	Min.	Typical	Max
twr	Write pulse width	65 nsec		
trd	Read pulse width	65 nsec		
twasu	Chip select setup to nWR	10 nsec		
twasu	A0 address setup time	75 nsec		
twahld	A0 address hold time	10 nsec		
twdsu	Data to write high setup time	5 nsec		
twdhld	Data hold time after write high	10 nsec		
tracc	Data valid after read low	20 nsec		25 nsec
trdhld	Data hold after read high	5 nsec		
trcsu	Chip select low to read low	10 nsec		
trcshld	Chip select hold after read high	10 nsec		
tcscs	nCS inactive to nCS asseted	85 nsec		

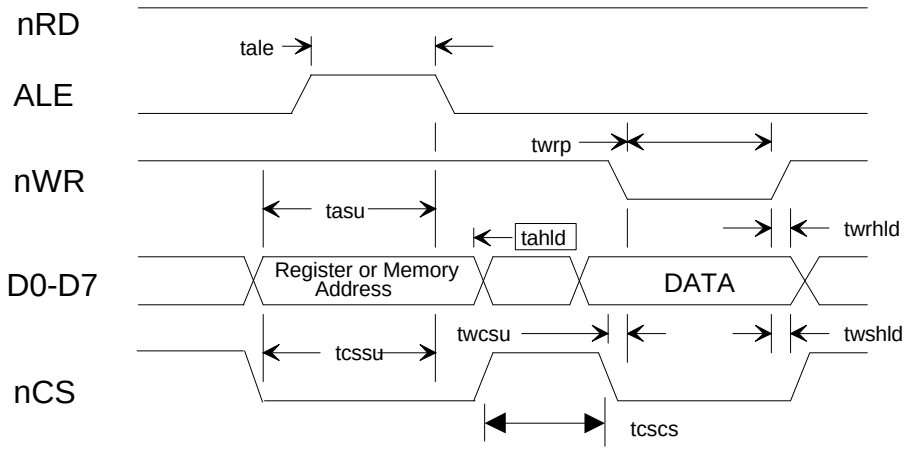
4.7.3 Multiplexed Address/Data Bus Read Cycle



Multiplexed Address I/O Read

Symbol	Parameter	Min.	Typical	Max
tale	ALE pulse width	65 nsec		
trdp	nRd low pulse width	65 nsec		
tasu	Address setup to ALE low	65 nsec		
tahld	Address hold after ALE low	10 nsec		
tracc	Data access after nRD low	20 nsec		80 nsec
trdhld	Data hold after nRD high	5 nsec		
tcssu	nCS low setup to ALE low	15 nsec		
trcsu	nCS low to nRD low	10 nsec		
tcshld	nCS hold after nRD high	10 nsec		

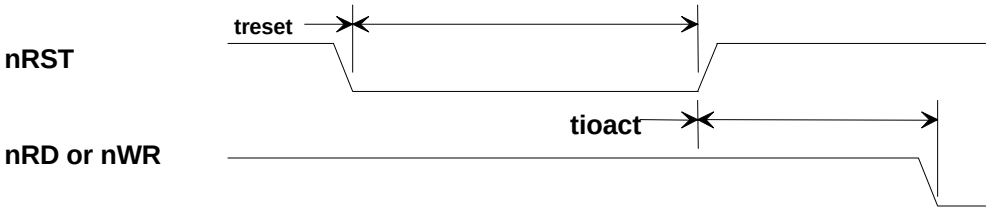
4.7.4 Multiplexed Address/Data Bus Write Cycle



Multiplexed Address I/O Write

Symbol	Parameter	Min.	Typical	Max
tale	ALE pulse width	65 nsec		
twrp	nWR low pulse width	65 nsec		
tasu	Address setup to ALE low	65 nsec		
tahld	Address hold after ALE low	10 nsec		
tdsetup	Data valid to nWR low	5 nsec		
twrhld	Data hold after nWR high	10 nsec		
tcssu	nCS low setup to ALE low	15 nsec		
twcsu	nCS low to nWR low	10 nsec		
twshld	nCS hold after nWR high	10 nsec		
tcscs	nCS inactive to nCS asserted	85 nsec		

4.7.5 Reset Timing

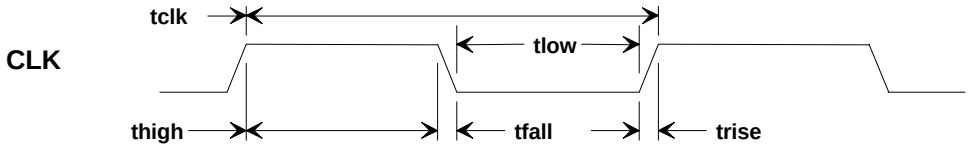


RESET TIMING

Symbol	Parameter	Min.	Typical	Max
treset	nRst Pulse width	16 clocks		
tioact	nRst high to nRD or nWR active	16 clocks		

Note: Clock is 48 MHz nominal.

4.7.6 Clock Timing Specifications



CLOCK TIMING

Symbol	Parameter	Min.	Typical	Max
tclk	Clock period (48 MHz)	20.0 nsec	20.8 nsec	
thigh	Clock high time	9 nsec		11 nsec
tlow	Clock low time	9 nsec		11 nsec
trise	Clock rise time			5.0 nsec
tfall	Clock fall time			5.0 nsec
	Duty Cycle	-5%		+5%