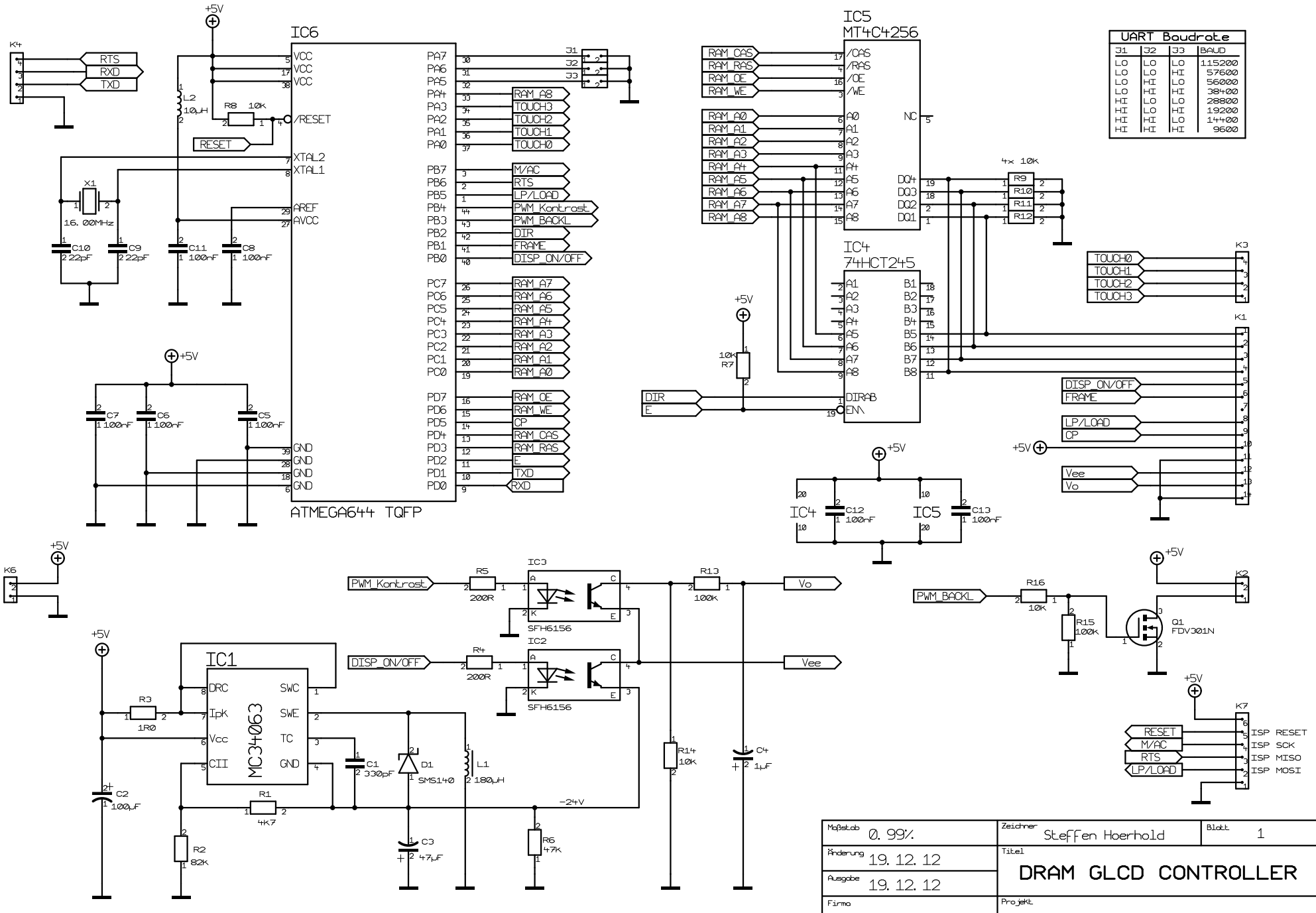
IC6
ATMEGA644 TQFP
IC5
MT4C4256
IC4
74HCT245
IC1
MC34063
IC2
IC3
SFH6156
SFH6156
Q1
FDV301N
D1
SMS140
UART Baudrate
J1 J2 J3 BAUD
LO LO LO 115200
LO LO HI 57600
LO HI LO 56000
LO HI HI 38400
HI LO LO 28800
HI LO HI 19200
HI HI LO 14400
HI HI HI 9600
RTS
RXD
TXD
RESET
/RESET
16.00MHz
RAM_CAS
RAM_RAS
RAM_OE
RAM_WE
RAM_A0
RAM_A1
RAM_A2
RAM_A3
RAM_A4
RAM_A5
RAM_A6
RAM_A7
RAM_A8
TOUCH0
TOUCH1
TOUCH2
TOUCH3
M/AC
LP/LOAD
PWM_Kontrast
PWM_BACKL
DIR
FRAME
DISP_ON/OFF
CP
E
TXD
RXD
Vee
Vo
+5V
-24V
4x 10K
ISP RESET
ISP SCK
ISP MISO
ISP MOSI
Maßstab 0.99%
Änderung 19.12.12
Ausgabe 19.12.12
Firma
Zeichner Steffen Hoerhold
Blatt 1
Titel
DRAM GLCD CONTROLLER
Projekt