PIC18FXXK80

PIC18FXX80 to PIC18FXXK80 Migration Guide

INTRODUCTION

The PIC18F66K80 family is a lower cost extension of Microchip's PIC18F8680, PIC18F4680 and PIC18F4580 Enhanced CAN families of products. With an operating voltage range of 1.8V-5.5V, the PIC18F66K80 is well-suited for the automotive and industrial applications.

Differentiating features of the newer device include:

- Extended operating voltage range
- nanoWatt XLP technology
- A Charge Time Measurement Unit (CTMU)
- A configurable 12-bit Analog-to-Digital (A/D) Converter
- An increased number of Capture/Compare/PWM modules (CCPs)

This migration document highlights the similarities and differences between the PIC18FXX80 and PIC18FXXK80 device families and shows the general principles for migrating PIC18FXX80 applications to PIC18FXXK80 devices.

The document is structured like data sheets, as shown at right, with each section focusing on a peripheral or major feature. Each section contains the following information, as applicable:

- A table comparison of PIC18FXXK80 and PIC18FXX80 peripheral features
- A table comparing bit names for each function
- A list of new PIC18FXXK80 features
- A list of unsupported PIC18FXX80 features
- A summary of migration considerations

Users are encouraged to review the PIC18FXXK80 device data sheet for information on the new modules and how they may be used in applications that are candidates for migration. (See **"References" on page 27**).

DEVICE OVERVIEW

The PIC18F66K80 is a new device family with ECAN technology, 12-bit A/D and nanoWatt XLP technology. Available in 28-pin, 40/44-pin and 64-pin packages, this family is largely pin compatible with other PIC18 families, such as the PIC18F4580, PIC18F4680 and PIC18F8680 families, allowing for easy migration.

Some additional features and improvements on existing features are available for the PIC18F66K80 device family. Table 1 compares feature differences between the 28-pin and 40/44-pin devices of the PIC18F4680 and PIC18F66K80 device families. Table 2 compares 64-pin devices of the PIC18F8680 and PIC18F66K80 device families.

TABLE 1: COMPARISON: PIC18FXX80 AND PIC18FXXK80 28, 40 AND 44-PIN DEVICES

Feature Description	PIC18FXX80	PIC18FXXK80
Maximum Operating Frequency	40 MHz	64 MHz
Maximum Program Memory	64 Kbytes	64 Kbytes
Maximum Data Memory (bytes)	3,328	3,648
Data EEPROM (bytes)	1,204	1,204
CTMU	No	Yes
SOSC Oscillator Options	No	Low-power oscillator option for SOSC
T1CKI	No	Yes
INTOSC	Up to 8 MHz	Up to 16 MHz
REFO	No	Yes
SPI/I^2C	One	One
Timers	One 8-bit Three 16-bit	Two 8-bit Three 16-bit
Timer Gates	None	Two
ECCP	28-pin devices – None 40/44-pin devices – One	All devices – One
CCP	One	Four
WDT Prescaler Options	Sixteen	Twenty-two
Maximum V_{DD}	5.5V	PIC18FXXK80 Devices – 5.5V operation PIC18LFXXK80 Devices – 3.6V operation
nanoWatt XLP	No	Yes
Internal Regulator	No	PIC18FXXK80 only
Low-Power BOR	No	Yes
Power-Saving Module Disable	No	Yes
Parallel Slave Port	40/44-pin devices	40/44-pin devices
A/D Converter	10-bit	12-bit, signed differential
A/D Channels	28-pin devices – 8 channels 40 and 44-pin devices – 11 channels	28-pin devices – 8 channels 40 and 44-pin devices – 15 channels
A/D Registers	A/D Result High Register (ADRESH) A/D Result Low Register (ADRESL) A/D Control Register 0 (ADCON0) A/D Port Configuration Register 1 (ADCON1) A/D Control Register 2 (ADCON2)	A/D Result High Register (ADRESH) A/D Result Low Register (ADRESL) A/D Control Register 0 (ADCON0) A/D Control Register 1 (ADCON1) A/D Control Register 2 (ADCON2) A/D Port Configuration Register 1 (ANCON0) A/D Port Configuration Register 2 (ANCON1)
EUSART	One	Two
Comparators	28-pin devices – None 40 and 44-pin devices – Two	All devices – Two
Oscillator Options	Nine	Fourteen
Ultra Low-Power Wake-up (ULPWU)	No	Yes
Adjustable Slew Rate for I/O	No	Yes
Open-Drain Option for I/O	Yes	Yes
Internal Weak Pull-up	PORTB	PORTB, PORTD, PORTE
Interrupt-on-Change	Yes	Yes
PLL (x4)	Available only for high-speed crystal and internal oscillators	Available for all oscillator options

TABLE 2: COMPARISON BETWEEN PIC18FXX80 AND PIC18FXXK80 64-PIN DEVICES

Feature Description	PIC18F6x80	PIC18F6xK80
Maximum Operating Frequency	40 MHz	64 MHz
Maximum Program Memory	64 Kbytes	64 Kbytes
Maximum Data Memory (bytes)	3,328	3,648
Data EEPROM (bytes)	1,204	1,204
CTMU	No	Yes
SOSC Oscillator Options	One	Two
T1CKI	No	Yes
INTOSC	No	Up to 16 MHz
REFO	No	Yes
SPI/I^2C	One	One
Timers	Two 8-bit Three 16-bit	Two 8-bit Three 16-bit
Timer Gates	None	Two
ECCP	One	One
CCP	One	Four
WDT Prescaler Options	Sixteen	Twenty-two
Maximum V_{DD}	5.5V	PIC18FXXK80 devices – 5.5V operation PIC18LFXXK80 devices – 3.6V operation
nanoWatt XLP	No	Yes
Regulator	No	Regulator for PIC18FXXK80 parts No Regulator for PIC18LFXXK80 parts
Low-Power BOR	No	Yes
Power-Saving Module Disable	No	Yes
Parallel Slave Port	Yes	Yes
A/D Converter	10-bit	12-bit, signed differential
A/D Channels	64-pin devices – 12 channels	64-pin devices – 11 channels
A/D Registers	A/D Result High Register (ADRESH) A/D Result Low Register (ADRESL) A/D Control Register 0 (ADCON0) A/D Port Configuration Register 1 (ADCON1) A/D Control Register 2 (ADCON2)	A/D Result High Register (ADRESH) A/D Result Low Register (ADRESL) A/D Control Register 0 (ADCON0) A/D Control Register 1 (ADCON1) A/D Control Register 2 (ADCON2) A/D Port Configuration Register 1 (ANCON0) A/D Port Configuration Register 2 (ANCON1)
EUSART	One	Two
Comparators	Two	Two
Oscillator Options	Seven	Fourteen
Ultra Low-Power Wake-up (ULPWU)	No	Yes
Adjustable Slew Rate for I/O	No	Yes
Open-Drain Option for I/O	Yes	Yes
Internal Weak Pull-up	PORTB	PORTB, PORTD, PORTE, PORTF, PORTG
Interrupt-on-Change	Yes	Yes
PLL (x4)	Available only for high-speed crystal and external oscillators	Available for all oscillator options
Data Signal Modulator	No	Yes

New PIC18FXXK80 Features

In addition to the rich feature set of the PIC18FXX80 device families, the following new features are available to improve flexibility and reduce CPU overhead:

- Data Signal Modulator (DSM) – This feature, only available on the 64-pin devices, allows two signals: a carrier signal and a modulator signal, to be modulated together to reduce emitted radiation.
- Adjustable Slew Rate – This feature allows a 10% adjusted slew rate on port outputs to reduce emitted radiation.
- Oscillator Options – There are new oscillator options that allow three different power levels for external oscillators and two power levels for high-speed crystals, with speeds of up to 64 MHz.
- Enhanced USART – One additional EUSART module is available for all pin count devices.
- Charge Time Measurement Unit (CTMU) – The capacitor time measurement unit interfaced with the A/D module allows for many applications, such as capacitive touch buttons and sliders.
- A/D Converter – This module has been improved with 12 bits of resolution as well as allowing a differential input mode and up to 15 analog ports.
- Low-Power BOR – The Brown-out Reset module has a range of four power-saving options.
- Watchdog Prescaler Options – The Watchdog Timer has six additional prescaler options, allowing periods of up to 4,194s (approximately 70 minutes).
- Internal Oscillator – The internal oscillator block now has three power options and is capable of up to 16 MHz operation.
- Capture/Compare/PWM Module – Three additional CCP modules have been added.
- Reference Clock Output – The device clock with configurable prescaler is available for output to eliminate additional oscillators for other components.
- Ultra Low-Power Wake-up (ULPWU) – A low-power Sleep mode using a slow falling voltage on an analog pin to trigger a wake-up.
- Timer Gates – Functionality enabling the 16-bit timers to increment based on either of the comparator outputs, when TMR2 matches PR2, or an external pin input.
- Open-Drain Output – The output pins for several peripherals can be configured as open-drain outputs, enabling external digital logic with other devices operating at higher voltages without using level translators.
- Internal Pull-up Resistors – All port pins have internal, weak pull-up resistors that can be enabled and PORTB can enable them individually per pin.
- Interrupt-on-Change – This feature exists on PIC18FXX80 devices, but PIC18FXXK80 devices can enable and disable each pin on PORTB, individually.
- On-Chip Regulator – The PIC18FXXK80 “F” parts have on-chip regulators that allow the peripherals to operate at a higher voltage than the CPU core. (Not available on “LF” parts).
- Secondary Oscillator – The secondary oscillator allows for a High-Power mode, Low-Power mode and a Digital Input mode.

Unsupported PIC18FXX80 Features

Each section contains a subsection with this heading that specifies which of its features are supported by the PIC18FXX80, but not by the PIC18FXXK80.

Migration Considerations

While migrating from PIC18FXX80 to PIC18FXXK80, users should consider:

- PIC18FXXK80 devices require a 10 µF, low-ESR capacitor on V_{CAP}. PIC18LFXXK80 devices do not require an external capacitor.
- When using “LF” parts, 5V operation is not supported. The maximum allowed voltage is 3.6V.
- Low-Voltage Programming (LVP) is enabled differently for the PIC18FXXK80, so the PGM external pin is not available.
- Bit 4 of PORTA is unavailable and T0CKI has been moved to RG4 because the RA4 pin has been replaced with the V_{DDCORE}/V_{CAP} pin.
- Some changes were made to the Special Function Registers (SFR) memory map, so bank selects must be reconsidered when porting assembly firmware.
- PIC18FXXK80 devices have the same packages as PIC18FXX80 devices, plus the following new ones:
- 28-pin QFN
- 28-pin SSOP
- 64-pin QFN
- 64-pin TQFP

Due to the additional features on these devices, some PIC18FXXK80 pins may have more functions than comparable PIC18FXX80 pins.

POWER-MANAGED MODES/ OSCILLATOR CONFIGURATIONS

New oscillator features have been added to the PIC18FXXK80 family which increase the system clock frequency and clock options while reducing power consumption.

Maximum system clock frequency has increased from 40 MHz for the PIC18FXX80 to 64 MHz for the PIC18FXXK80. New power modes are introduced in INTOSC and EC Oscillator modes.

An Ultra Low-Power Wake-up, an inexpensive feature that provides extended Sleep intervals, is supported.

TABLE 3: COMPARISON OF PIC18F4680 AND PIC18F46K80 POWER-MANAGED MODES/ OSCILLATOR CONFIGURATIONS

Feature Description	PIC18F4680	PIC18F46K80
Maximum Operating Frequency	40 MHz	64 MHz
Internal Oscillators	Two	Three
External Clock Power Modes	One	Three
Secondary Oscillator Power Modes	One	Two
HS Oscillator Power Modes	One	Two
PLL Input Frequency Range	4 MHz to 10 MHz	4 MHz to 16 MHz
INTOSC Tuning bits	Five	Six
INTOSC+ PLL Frequency Range	16 MHz 32 MHz	16 MHz 32 MHz 64 MHz
LP Operating Frequency	5 kHz to 200 kHz	32 kHz
EC Operating Frequency	0 to 40 MHz	0 to 64 MHz
Default INTOSC Frequency	1 MHz	8 MHz

TABLE 4: POWER-MANAGED MODES/OSCILLATOR CONFIGURATIONS BIT NAMING CONVENTION AND FUNCTIONALITY

Functionality	PIC18FXX80	PIC18F46K80
INTOSC Stable	IOFS (OSCCON<2>)	HFIOFS (OSCCON<2>)
Secondary Oscillator Status	T1RUN (T1CON<6>)	SOSCRUN (OSCCON2<7>)
Secondary Oscillator Drive Strength	T1OSCEN (T1CON<3>)	SOSCDRV (OSCCON2<4>)
INTOSC Frequency Tuning (1)	TUN<4:0> (OSCTUNE<4:0>)	TUN<5:0> (OSCTUNE<5:0>)
Oscillator Frequency Value IRCF<2:0> (OSCCON<6:4>)	000 (31 kHz)	000 (31 kHz)
	001 (125 kHz)	001 (250 kHz)
	010 (250 kHz)	010 (500 kHz)
	011 (500 kHz)	011 (1 MHz)
	100 (1 MHz)	100 (2 MHz)
	101 (2 MHz)	101 (4 MHz)
	110 (4 MHz)	110 (8 MHz)
	111 (8 MHz)	111 (16 MHz)
Secondary Oscillator Enable	T1OSCEN (T1CON<3>)	SOSCEN (T1CON<3>)
External Clock Mode (CONFIG1H<3:0>)	FOSC = 1101	FOSC = 0101 (High) FOSC = 1010 (Medium) FOSC = 1100 (Low)
External Clock Mode with CLKOUT	FOSC = 101x	FOSC = 0100 (High) FOSC = 1010 (Medium) FOSC = 1101 (Low)
High-Speed Crystal Mode	FOSC = 0101 (HS) FOSC = 0110 (HSPLL)	FOSC = 0010 (High) FOSC = 0011 (Medium)
Medium Speed (XT) Crystal Mode	FOSC = 0001	FOSC = 0001
Low-Power (LP) Crystal Mode	FOSC = 0000	FOSC = 0000
External RC Oscillator Mode	FOSC = 0111	FOSC = 0111
External RC Oscillator Mode with CLKOUT	FOSC = 0110	FOSC = 0110
Internal Oscillator Mode(1)	FOSC = 1000	FOSC = 1000
Internal Oscillator Mode(1) with CLKOUT	FOSC = 1001	FOSC = 1001
External Oscillator PLL Enable	N/A	PLLCFG (CONFIG1H<4>)
Internal Oscillator PLL Enable	PLLEN (OSCTUNE<6>)	PLLEN (OSCTUNE<6>)

Note 1: Not available on the PIC18F8680 family.

New PIC18F46K80 Features

The following new features are available on the PIC18FXXK80 to optimize the power consumption and increase system clock flexibility:

- Maximum operation frequency increased from 40 MHz to 64 MHz
- External clock oscillator has three power modes:
  - Low-Power mode (FOSC ≤ 160 kHz)
  - Medium Power mode (160 kHz ≤ FOSC ≤ 16 MHz)
  - High-Power mode (16 MHz ≤ FOSC ≤ 64 MHz)
- Internal oscillator has three sources with the following frequency ranges:
  - Low-Power LF-INTOSC (32 kHz)
  - Medium Power MF-INTOSC (31.25 kHz to 500 kHz)
  - High-Accuracy HF-INTOSC (500 kHz to 16 MHz)

The Ultra Low-Power Wake-up feature provides an inexpensive solution for extended wake-up times using an external capacitor.

A dedicated PLL enable bit is available for all clock sources capable of 4 MHz operation.

Multiple Secondary Oscillator Input Buffer modes including:

- Digital
- High Gain
- Low Power

Unsupported PIC18FXX80 Features

All PIC18FXX80 oscillator features and power-managed modes are supported by the PIC18FXXK80 family.

Migration Considerations

While migrating from PIC18FXX80 to PIC18FXXK80, users should consider:

- New bit and register locations for primary and secondary oscillator features
- New low-power modes to reduce power consumption
- Increased number of INTOSC tuning bits
- Changes made to supported crystal mode frequency ranges
- New default internal oscillator frequency

RESETS

The PIC18FXXK80 family of devices supports Configuration Mismatch ($\overline{CM}$) Reset and VDDCORE supply Brown-out Reset, in addition to all of the PIC18FXX80 resets.

TABLE 5: COMPARISON OF RESETS

Feature Description	PIC18FXX80	PIC18FXXK80
Configuration Mismatch ($\overline{CM}$) Reset	No	Yes
VDDCORE Supply Brown-out Reset	No	Yes
Power-on Reset (POR)	Yes	Yes
$\overline{MCLR}$ During Run Mode	Yes	Yes
$\overline{MCLR}$ During Power-Managed Mode	Yes	Yes
WDT Reset	Yes	Yes
Programmable BOR	Yes	Yes
RESET Instruction	Yes	Yes
Stack Full/Empty Reset	Yes	Yes
BOR Trip Voltages (V)	2.1 2.8 4.3 4.6	1.8 2.0 2.7 3.0
Number of BOR Power Levels	One	Four

TABLE 6: RESETS BIT NAMING CONVENTION AND FUNCTIONALITY

Functionality	PIC18FXX80	PIC18FXXK80
Configuration Mismatch ($\overline{CM}$) Reset Detection Flag	N/A	$\overline{CM}$ (RCON<5>)
BOR Trip Point Selection	BORV<1:0> (CONFIG2L<4:3>)	BORV<1:0> (CONFIG2L<4:3>)
BOR Enable	BOREN<1:0> (CONFIG2L<2:1>)	BOREN<1:0> (CONFIG2L<2:1>)
Power-up Timer Enable	$\overline{PWRTEN}$ (CONFIG2L<0>)	$\overline{PWRTEN}$ (CONFIG2L<0>)
BOR Software Enable	SBOREN (RCON<6>)	SBOREN (RCON<6>)
Reset Status Register	RCON	RCON
Stack Error Reset Enable	STVREN (CONFIG4L<0>)	STVREN (CONFIG4L<0>)

New PIC18FXXK80 Features

The Configuration Mismatch ($\overline{CM}$) Reset is a new feature of the PIC18FXXK80 family that is designed to detect and attempt to recover from random, memory corrupting events. These include Electrostatic Discharge (ESD) events that can cause widespread, single bit changes throughout the device and result in catastrophic failure.

In PIC18FXXK80 family devices, the device Configuration registers (located in the configuration memory space) are continuously monitored during operation by comparing their values to complimentary shadow registers. If a mismatch is detected between the two sets of registers, a $\overline{CM}$ Reset automatically occurs.

These events are captured by the $\overline{CM}$ bit (RCON<5>). The state of the bit is set to '0' whenever a $\overline{CM}$ event occurs. The bit does not change for any other Reset event.

The affect of a $\overline{CM}$ Reset is similar to a $\overline{MCLR}$ Reset, RESET instruction, WDT time-out or Stack Event Resets. These and Power-on Reset events cause the Configuration Words' shadow registers to be reloaded from the programmed Configuration Word locations.

Note that the V_{DDCORE} supply Brown-out Reset is only available when V_{REG} is enabled for the PIC18FXXK80. Since the PIC18FXXK80 devices do have an internal regulator option, the BOR feature is not available on these devices.

Unsupported PIC18FXX80 Features

All PIC18FXX80 Reset functions are supported by the PIC18FXXK80 family.

Migration Considerations

Though all PIC18FXX80 Reset features are supported by the PIC18FXXK80, changes made in the BOR Reset trip point should be considered. These values have been modified to support the PIC18FXXK80's lower voltage operation.

MEMORY ORGANIZATION

Because PIC18FXXK80 devices have more peripherals than PIC18FXX80 devices, additional registers are necessary. The memory map for the ECAN module, however, keeps associated registers contiguous to optimize memory utilization and reduce memory bank changes.

The result is a total user RAM area of 3,648 bytes, 320 bytes more than the PIC18FXX80 devices.

TABLE 7: COMPARISON OF MEMORY ORGANIZATION

Feature Description	PIC18FXX80	PIC18FXXK80
Total User RAM (bytes)	3,328(1)	3,648
Number of SFR Banks	3	2

Note 1: PIC18F4580 has 1536 bytes of user RAM.

New PIC18FXXK80 Registers

Table 8 lists the new registers on the PIC18FXXK80.

TABLE 8: NEW REGISTERS AVAILABLE ON PIC18FXXK80

OSCCON2	PIE4	CCP3CON
BAUDCON2	IPR5	CCPR4H
TXSTA2	PIR5	CCPR4L
RCSTA2	PIE5	CCP4CON
RCREG2	CM2CON	CCPR5H
TXREG2	ANCON1	CCPR5L
SPBRGH2	ANCON2	CCP5CON
SPBRG2	WPUB	PSPCON
REFOCON	IOCB	MDCON(†)
T1GCON	PMD1	MDSRC(†)
T3GCON	PMD2	MDCARH(†)
CCPTMRS	PMD3	MDCARL(†)
ODCON	CTMUCONH	TRISG(†)
SLRCON	CTMUCONL	TRISF(†)
T4CON	CTMUICONH	LATG(†)
TMR4	PADCFG1	LATF(†)
PR4	PSTR1CON	PORTG(†)
IPR4	CCPR3H	PORTF(†)
PIR3	CCPR3L	

† Register available only on 64-pin devices.

Table 9 lists the PIC18FXX80 registers that have been renamed on the PIC18FXXK80 devices. Old names will be backwards compatible and both names will be supported by the tool chain.

These differences will only be evident in the data sheet. (See **"References" on page 27**).

TABLE 9: COMPARISON OF REGISTER NAMES

PIC18FXX80 Name	PIC18FXXK80 Name
BAUDCON	BAUDCON1
SPBRGH	SPBRGH1
SPBRG	SPBRG1
RCREG	RCREG1
TXREG	TXREG1
TXSTA	TXSTA1
RCSTA	RCSTA1
CMCON	CM1CON
CCPR1H	CCPR2H
CCPR1L	CCPR2L
CCP1CON	CCP2CON

Migration Considerations

When migrating from the PIC18FXX80 family to the PIC18FXXK80 family, some backward compatibility issues should be considered.

Since the PIC18FXXK80 has a different memory organization, some registers will be in different banks. This is only a concern if the firmware is in assembly, since a C compiler handles bank select changes.

The memory reorganization also results in some registers being renamed. For all firmware using the CCP module, the PIC18FXX80's register names must be changed, as shown in Table 9. All other registers that are renamed will be backwards-compatible with the register names used in the PIC18FXX80.

FLASH PROGRAM MEMORY/DATA EEPROM MEMORY

The differences between the PIC18FXXK80 and PIC18FXX80 devices are the SRAM size and a few interrupt flag bit locations. The sizes of the program memory and data EEPROM are the same in both device families.

TABLE 10: FLASH PROGRAM/DATA EEPROM BIT NAME COMPARISON

Functionality	PIC18FXX80	PIC18FXXK80
Data EEDATA/Flash Write Operation Interrupt Enable	EEIE (PIE2<4>)	EEIE (PIE4<6>)
EE Interrupt Priority	EEIP (IPR2<4>)	EEIP (IPR4<6>)
Data EEDATA/Flash Write Operation Interrupt Flag	EEIF (PIR2<4>)	EEIF (PIR4<6>)

New PIC18FXXK80 Features

The PIC18F4580 has a selectable 1-Kbyte or 2-Kbyte boot block option and the PIC18F4680 has a selectable 1-Kbyte, 2-Kbyte or 4-Kbyte boot block option. For the PIC18F4580/4680, this option is selected by the BBSIZ0 bit (CONFIG4L<4>) in the Configuration register. The PIC18F8680 does not have the selectable boot block option.

Unsupported PIC18FXX80 Features

All PIC18FXX80 Flash program and data EEPROM features are supported by the PIC18FXXK80 family.

Migration Considerations

While migrating from PIC18FXX80 to PIC18FXXK80, the changed register locations and new positions of the EEIE, EEIP and EEIF bits must be addressed. Since the register locations have changed, this will require a code change for both assembler and compiler development tools.

8x8 HARDWARE MULTIPLIER

There are no differences between the PIC18FXX80 and the PIC18FXXK80 hardware multiplier.

INTERRUPTS

PIC18FXXK80 devices have increased the number of interrupts for better control of peripherals and external events through the port pins. (See the bold text in Table 11). There are some changes in bit names of interrupt control and status SFRs.

This section covers interrupts associated with the core functions. For information on specific peripheral interrupts, see the section for the peripheral of interest.

TABLE 11: INTERRUPTS COMPARISON

Feature Description	PIC18FXX80	PIC18FXXK80
Interrupt Flag Registers	PIR1, PIR2, PIR3	PIR1, PIR2, PIR3, **PIR4**, **PIR5**
Interrupt Enable Registers	PIE1, PIE2, PIE3	PIE1, PIE2, PIE3, **PIE4**, **PIE5**
Interrupt Priority Registers	IPR1, IPR2, IPR3	IPR1, IPR2, IPR3, **IPR4**, **IPR5**

New PIC18FXXK80 Features

External Interrupt 3 has been added to the PIC18FXXK80 core interrupt suite. For more information, see the PIC18FXXK80 data sheet. (See **"References" on page 27**).

Unsupported PIC18FXX80 Features

All PIC18FXX80 interrupt features are supported by the PIC18FXXK80 family.

Migration Considerations

Software migration, from the PIC18FXX80 to the PIC18FXXK80 family, will be affected by changes in the PIC18FXXK80 family. A few interrupt control/status SFRs have been added and some bits may have changed their associated registers.

Also, some registers and bit names have changes for peripheral interrupts. Source code must be modified to use the new bit names of the PIC18FXXK80 device family.

I/O PORTS

The PIC18FXXK80 is nearly pin compatible with the PIC18FXXK80 for easy migration across the various package sizes.

TABLE 12: USART COMPARISON

Feature Description	PIC18FXX80	PIC18FXXK80
Number of I/O (28-pin)	24 + 1 input only	23 + 1 input only
Number of I/O (64-pin)	52 + 1 input only	53 + 1 input only
Number of I/O (40/44-pin)	35 + 1 input only	34 + 1 input only
Peripherals with Open-drain Option	1^2C™	ECCP1 • CCPx EUSARTx • SPI1 • 1^2C
Ports with Internal Pull-up Option	PORTB	PORTB • PORTD PORTE
AVDD/AVSS Pins on 44-Pin and 64-Pin TQFP	Yes on 44-pin QFN only, Yes on 64-pin	No on 44-pin, Yes on 64-pin
Individual Analog/Digit Input Pin Selects	No	Yes

TABLE 13: PORT BIT NAMING CONVENTION AND FUNCTIONALITY

Feature Description	PIC18FXX80	PIC18FXXK80
Port Data	PORTA<7:0> PORTB<7:0> PORTC<7:0> PORTD<7:0> PORTE<3:0>	PORTA<7:5,3:0> PORTB<7:0> PORTC<7:0> PORTD<7:0> PORTE<3:0>
Port Latch	LATA<7:0> LATB<7:0> LATC<7:0> LATD<7:0> LATE<3:0>	LATA<7:5,3:0> LATB<7:0> LATC<7:0> LATD<7:0> LATE<3:0>
Port Direction	TRISA<7:0> TRISB<7:0> TRISC<7:0> TRISD<7:0> TRISE<2:0>	TRISA<7:5,3:0> TRISB<7:0> TRISC<7:0> TRISD<7:0> TRISE<2:0>
Pull-up Enables	$\overline{\text{RBPU}}$ (INTCON2<7>)	$\overline{\text{RBPU}}$ (INTCON2<7>) $\overline{\text{RDPU}}$ (PADCFG1<7>) REPU (PADCFG1<6>)
Analog/ Digital Select Register	ADCON1	ANCON0 ANCON1
PSP Control Register	TRISE	PSPCON

New PIC18FXXK80 Features

- PIC18FXXK80 pins with analog functions can be configured individually as analog or digital. This is done through the ANSEL bits in the ANCON1 and ANCON0 registers. The PIC18FXX80 PCFG bits in the ADCON1 register configure pins based on a table of predefined analog/digital combinations.
- PORTB, PORTD and PORTE have an internal pull-up option. (PIC18FXX80 devices have pull-ups only on PORTB).
- Open-drain outputs on USARTs, the MSSP module (in SPI mode) and the CCP.

Unsupported PIC18FXXK80 Features

PORTA<4> is available on PIC18FXX80 devices, but it is not available on PIC18FXXK80 devices.

Migration Considerations

The few items to be considered in migrating ports from PIC18FXX80 to PIC18FXXK80 include:

- PSP control registers moved from TRISE to PSPCON
- RA4 is not available as an I/O pin for PIC18FXXK80
- Analog/digital pin Configuration bits are spread across the ANCON1 and ANCON2 registers

TIMERS

PIC18FXXK80 devices have two 8-bit timers and three 16-bit timers, while PIC18FXX80 devices have only one 8-bit timer and three 16-bit timers. These differences and other features, that facilitate enhanced performance and flexibility, include:

- Gated Timer mode to support event-triggered counting
- Comparator, timer and gate pin available as event trigger for Timer1/3
- Multiple clock sources
- Individual secondary oscillator enable control for Timer1 and Timer3
- Additional flexibility in timer selection for CCP modules

TABLE 14: TIMER COMPARISON

Feature Description	PIC18FXX80	PIC18FXXK80
Timer Modules	Four	Five
8-Bit Timers	One(1)	Two
16-Bit Timers	Three	Three
Associated CCP Modules	Two	Five
Timer1 Gated Option	No	Yes
Timer3 Gated Option	No	Yes
Source of Clock for Timer1/3	Instruction Clock (FOSC/4) External Clock (T1/3CKI or SOSC)	Instruction Clock (FOSC/4) External Clock (T1/3CKI or SOSC) System Clock (FOSC)
Individual Secondary Oscillator Enables	No	Yes
Secondary Oscillator Clock Status	T1RUN (T1CON< 6>)	SOSCRUN (OSCCON2<6>)
Timer Gate Source for Timer1/3	N/A	Gate pin Timer2/PR2 match Comparator 1 event Comparator 2 event
Gated Timers Modes	N/A	Toggle Single Shot/Pulse Single Shot/Pulse Toggle
Resetting Timers	A/D Converter Special Event Trigger from ECCP will reset Timer1	ECCP event can reset Timer3 A/D Converter Special Event Trigger from ECCP will reset Timer1
Gated Interrupts	No	Yes
Gate Input Pins	No	Yes

Note 1: PIC18F6680 has two 8-bit timers,

TABLE 15: TIMER BIT NAMING CONVENTION AND FUNCTIONALITY COMPARISON

Functionality	PIC18FXX80	PIC18FXXK80
Timer1 Clock Source Select	TMR1CS (T1CON<1>)	TMR1CS<1:0> (T1CON<7:6>)
T1CON<3> Secondary Oscillator Enable	T1OSCEN	SOSCEN
Secondary Oscillator System Clock Status	T1RUN (T1CON<6>)	SOSCRUN (OSCCON2<6>)
T1CON<RD16>: 16-Bit Read/Write Enable	T1CON<7>	T1CON<1>
Timer3 Clock Source Select	TMR3CS (T3CON<1>)	TMR3CS<1:0> (T3CON<7:6>)
T3CON Secondary Oscillator Enable	N/A	SOSCEN (T3CON<3>)
T3CON<RD16>: 16-Bit Read/Write Enable	T3CON<7>	T3CON<1>
CCP Timer Source Selection	T3ECCP<1:0> (T3CON<6,3>)	CxTSEL CCPTMRS<4:0>)

New PIC18FXXK80 Features

- The PIC18FXXK80 devices have five timers overall: three 16-bit timers and two 8-bit timers
- Two of the 16-bit timers, Timer1 and Timer3, come with the enhanced features for multiple clock sources and a configurable gated timer feature to control counting with event triggers
- Timer1 and Timer3 can derive its clock from one of the following sources:
  - System Clock (FOSC): Timer counts four times faster than the instruction cycle supporting highest available precision over a shorter interval of time.
  - Instruction Clock (FOSC/4): Timer counts at the same rate that the instructions will be executed. This is the legacy feature supported by the PIC18FXX80 family.
  - External Clock Source/Secondary Oscillator: Counter from the external signal on the TxCKI pin or timer from the external 32 kHz oscillator.
- Timer1 and Timer3 together can derive its clock from a 32 kHz oscillator with the Secondary Oscillator Enable bit (SOSCEN). The SOSCEN bit is available individually in the Timer Configuration registers, T1CON<3> and T3CON<3> (in PIC18FXX80 devices, Timer1 and Timer3 share this bit).
- Timer1 and Timer3 Gated mode is an event triggered timer enable, in which an external trigger source controls the timer count and sets the interrupt flag. The polarity of the trigger is selectable with the gate signal polarity bit, T1GPOL (T1GCON<6>). The gate triggers are software selectable and can be one of the following:
  - External signal on T1G pin
  - TMR2/PR2 match
  - Comparator 1 or Comparator 2 transition
- Three Gated modes are available and can be combined. The modes are:
  - Toggle Mode – Measures the period of a Timer1 gate signal
  - Single Pulse Mode – Captures the single high or low time of the gate trigger
  - Toggle Single Pulse Mode – Measures the single period time of gate source signal
- Gated timer interrupts can be enabled to indicate gated timer count completion
- CCP modules have greater flexibility for multiple timer sources, being selectable in the CCPTMRS registers associated with each of the five CCP modules

Unsupported PIC18FXX80 Features

All PIC18FXX80 timer features are supported by the PIC18FXXK80 devices.

Migration Considerations

PIC18FXXK80 devices allow clock speeds up to 64 MHz, compared to PIC18FXX80 devices top speed of 40 MHz. This means higher clock rates and improved resolution are supported.

CAPTURE/COMPARE/PWM (CCP)

The CCP module of the PIC18FXX80 and PIC18FXXK80 devices are very similar. Table 16 shows the major differences between the controllers.

TABLE 16: CAPTURE MODE COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
Number of Modules	One	Four
Name of the Modules	CCP1	CCP2-CCP5
Associated I/O Pin	RC2	RC2 • RC6 RC7 • RB5
Clock Sources	Timer1 • Timer3	Timer1 • Timer3
Timer Size	16 bits	16 bits
Interrupt Flags	CCP1IF (PIR1<2>)	CCP2IF (PIR3<2>) CCP3IF (PIR4<0>) CCP4IF (PIR4<1>) CCP5IF (PIR<2>)
Capture Modes for CCPx Pin and CAN Message	Every falling edge Every rising edge Every CAN message Every 4th edge Every 4th CAN message Every 16th edge Every 16th CAN message	Every falling edge Every rising edge Every CAN message (CCP2 only) Every 4th edge Every 4th CAN message (CCP2 only) Every 16th edge Every 16th CAN message (CCP2 only)

TABLE 17: COMPARE MODE COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
Number of Modules	One	Four
Name of the Modules	CCP1	CCP2-CCP5
Associated I/O Pin	RC2	RC2 • RC6 RC7 • RB5
Clock Sources	Timer1 • Timer3	Timer1 • Timer3
Timer Size	16 bits	16 bits
Interrupt Flags	CCP1IF (PIR1<2>)	CCP2IF (PIR3<2>) CCP3IF (PIR4<0>) CCP4IF (PIR4<1>) CCP5IF (PIR<2>)
Compare Match Response (In Addition to CCPxIF Set and Timer Reset)	CCPx Pin High to Low CCPx Pin Low to High CCPx Pin Toggle Special Event Trigger (A/D start)	CCPx Pin High-to-Low CCPx Pin Low-to-High CCPx Pin Toggle Special Event Trigger (A/D start)

TABLE 18: PWM MODE COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
Number of Modules	One	Four
Name of the Modules	CCP1	CCP2-CCP5
Associated I/O Pin	RC2	RC2 • RC6 RC7 • RB5
Clock Sources	Timer2	Timer2 • Timer4
Timer Select Register	T3CON	CCPTMRS
Timer Size	8	8
Minimum Duty Cycle	25 ns at 40 MHz (TOSC)	15.6 ns at 64 MHz (TOSC)
Minimum Period	100 ns at 40 MHz (TCY)	62.5 ns at 64 MHz (TCY)

New PIC18FXXK80 Features

New features include:

- Faster clock speed for high-resolution capture, compare and PWM functions
- Time-stamp option for CAN messages
- More CCP peripherals
- Two clock source options for the PWM peripheral

Unsupported PIC18FXX80 Features

There are no unsupported PIC18FXX80 features.

Migration Considerations

With the similarity of the PIC18FXX80 and PIC18FXXK80 families CCP modules, the main considerations are how the new device selects a PWM timer and the module to perform CAN time-stamps.

PIC18FXXK80 devices use the CCPTMRS register's CxTSEL bits to select timers (PIC18FXX80 devices select timers using T3CON). PIC18FXXK80 devices moved the time-stamp function from CCP1 to CCP2.

All other CCP module functions require no software modifications when migrating from the PIC18FXX80 to the PIC18FXXK80.

ENHANCED CAPTURE/COMPARE/ PWM (ECCP)

The Enhanced Capture/Compare/PWM module is very similar between PIC18FXX80 and PIC18FXXK80 devices. Significant differences include the method for timer selection and the addition of Pulse Steering mode.

ECCP1 capture and compare functionality is identical to that of the CCP modules. For more information on these functions, see the CCP section of the PIC18FXXK80 data sheet. (See **"References" on page 27**).

TABLE 19: ENHANCED CAPTURE COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
Number of Modules (40+ pins)	One	One
Number of Modules (28 pins)	None	One
Name of the Modules	ECCP1	ECCP1
Associated I/O Pins	RC4 • RC5 RD6 • RD7	RC4 • RC5 RD6 • RD7
Open-Drain Option	No	Yes
Clock Sources	Timer2	Timer2 • Timer4
Timer Select Register	T3CON	CCPTMRS
Timer Size	8 bits	8 bits
Pulse Steering Mode	No	Yes
ECCP Modes	Single | Half-Bridge | Full-Bridge, Forward | Full-Bridge, Reverse	Single | Half-Bridge | Full-Bridge, Forward | Full-Bridge, Reverse
Auto-Shutdown	Yes	Yes
Auto-Shutdown Sources	FLT0 pin • Comparator 1 Comparator 2 • ECCPxASE	FLT0 pin • Comparator 1 Comparator 2 • ECCPxASE
Minimum Duty Cycle	25 ns at 40 MHz (T_{OSC})	15.6 ns at 64 MHz (T_{OSC})
Minimum Period	100 ns at 40 MHz (T_{CY})	62.5 ns at 64 MHz (T_{CY})

New PIC18FXXK80 Features

- Faster clock speed for high-resolution capture, compare and PWM functions
- Two clock source options for the PWM peripheral
- Pulse Steering Mode

Unsupported PIC18FXX80 Features

All PIC18FXX80 ECCP features can be supported by the PIC18FXXK80 product family.

Migration Considerations

The only significant migration consideration is how the PWM timer selection is made. The selection has been moved from the T3CON register to a new register, CCPTMRS, using the CxTSEL bits.

All other ECCP functionality is the same when migrating from the PIC18FXX80 to the PIC18FXXK80.

MASTER SYNCHRONOUS SERIAL PORT (MSSP) – I²C™

PIC18FXXK80 devices support the address masking feature in I²C slave operation. This feature allows the I²C slave to respond to a range of addresses by masking the corresponding bits of the incoming address.

PIC18FXXK80 devices also support the power-saving Peripheral Module Disable (PMD) feature in the MSSP module. Setting the PMD bit of the MSSP module disables all clock sources to the module, reducing its power consumption to an absolute minimum.

TABLE 20: I²C™ COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
7-Bit Address Masking Mode	No	Yes
5-Bit Address Masking Mode	No	Yes
MSSP Module Peripheral Module Disable (PMD)	No	Yes

New PIC18FXXK80 Features

ADDRESS MASKING

The PIC18FXXK80 family of devices is capable of using two different Address Masking modes in I²C slave operation: 5-Bit Address Masking and 7-Bit Address Masking.

The masking mode is selected at device configuration using the MSSPMSK Configuration bit (CONFIG3H<3>). The default device configuration is 7-Bit Address Masking mode.

Masking an address bit causes the bit to become a “don’t care.” When one address bit is masked, two addresses will be Acknowledged and cause an interrupt. It is possible to mask more than one address bit at a time, which greatly expands the number of addresses Acknowledged.

The I²C slave behaves the same way, whether address masking is used or not, but when address masking is used, the I²C slave can Acknowledge multiple addresses and cause interrupts. When this occurs, it is necessary to determine which address caused the interrupt by checking the SSPBUF.

Both masking modes, in turn, support address masking of 7-bit and 10-bit addresses. The combination of masking modes and addresses provides different ranges of Acknowledgeable addresses for each combination.

While both masking modes function in roughly the same manner, the way they use address masks are different.

MSSP MODULE PMD

Disabling the MSSP module by clearing the SSPEN bit disables the module’s functionality, but leaves its registers available to be read and written to. This reduces power consumption, but not by as much as the PMD alternative.

Setting the SSPMD (PMD0<0>) for MSSP module, disables all clock sources to the module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the MSSP peripheral are disabled, so writes to those registers have no effect and read zero values similar to unimplemented registers.

Unsupported PIC18FXX80 Features

All PIC18FXX80 I²C features can be supported by the PIC18FXXK80 product family.

Migration Considerations

If the MSSP (I²C) module is used in an application, the address masking and PMD features need to be considered when migrating from PIC18FXX80 to PIC18FXXK80 devices. These features are not available in the PIC18FXX80, but are supported in the PIC18FXXK80.

MASTER SYNCHRONOUS SERIAL PORT (MSSP) – SPI

Both the PIC18FXX80 and PIC18FXXK80 families have one MSSP (SPI) module. Both families support all four SPI modes of operation and are similar in performance.

TABLE 21: SPI COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
SPI Modules	1	1
Maximum Clock Speed	10 MHz (40 MHz/4)	16 MHz (64 MHz/4)
Open-Drain Peripheral Outputs	No	Yes (SCK and SDO can be configured as open-drain outputs)
Peripheral Module Disable	No	Yes

Note 1: The 16 MHz SPI frequency may be reduced to meet data setup and hold times.

New PIC18FXXK80 Features

The following new features are available on the PIC18FXXK80:

- Increased MIPS operation enabling higher data transmission rates, up to 16 MHz
- Additional FOSC/8 option for SPI Master Mode
- Open-drain ability on outputs (SCK and SDO) enabling to be interfaced with different voltage levels, using an external pull-up

  To enable the open-drain outputs capability, the SPIOD bit (ODCON<7>) must be set
- To reduce power consumption, the MSSP module can be shut off through the SPI module disable bit, SPIMD (PMD0<0>)

  By default, on POR, the module is enabled.

Unsupported PIC18FXX80 Features

All PIC18FXX80 MSSP/SPI features can be supported by PIC18FXXK80 devices.

Migration Considerations

There have been some minor changes in the control and status registers and bits names, so care must be taken while accessing them.

Both PIC18FXX80 and PIC18FXXK80 devices multiplex all four peripheral signals (SCK, SDI, SDO and $\overline{SS}$) with the same port pins. Therefore, no hardware changes are required.

Both device families can also make the $\overline{SS}$ signal (multiplexed with AN4) digital. But this is configured differently for the two families of devices:

- PIC18FXX80 devices – The A/D port configuration bits, PCFG<3:0> (ADCON1<3:0>), are used
- PIC18FXXK80 devices – The ANSEL4 bit (ANCON0<4>) must be cleared

ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

PIC18FXXK80 devices have two EUSART modules and PIC18FXX80 devices have one EUSART module. The PIC18FXXK80 family also has additional control features for supporting a wider variety of data formats.

TABLE 22: EUSART COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
EUSART Modules	One	Two
Open-Drain Option	No	Yes
LIN/J2602 Bus Support	Yes	Yes
Wake-up on Reception	Yes	Yes
Auto-Baud	Yes	Yes
12-Bit Break Character	Yes	Yes
Synchronous Modes	Yes	Yes
Data/Receive Polarity Select	No	Yes

TABLE 23: EUSART BIT NAMING CONVENTION AND FUNCTIONALITY

Functionality	PIC18FXX80	PIC18FXXK80
Transmit Status/Control	TXSTA	TXSTA<2:1>
Receive Status/Control	RCSTA	RCSTA<2:1>
EUSART1 Baud Rate Generator Register High Byte	SPBRGH	SPBRGH1
EUSART1 Baud Rate Generator Register	SPBRG	SPBRG1
EUSART2 Baud Rate Generator Register High Byte	N/A	SPBRGH2
EUSART2 Baud Rate Generator Register	N/A	SPBRG2
Baud Rate Control Registers	BAUDCON	BAUDCON<2:1>
Auto-Baud Detect Enable	ABDEN (BAUDCON<0>)	ABDEN (BAUDCONx<0>)
Wake-up Enable	WUE (BAUDCON<1>)	WUE (BAUDCONx<1>)
16-Bit Baud Rate Register Enable	BRGH (BAUDCON<3>)	BRGH (BAUDCONx<3>)
Synchronous Clock Polarity Select	SCKP (BAUDCON<4>)	TXCKP (BAUDCONx<4>)
Data/Receive Polarity Select	N/A	RXDTP (BAUDCONx<5>)
Receive Operation Idle Status	RCIDL (BAUDCON<6>)	RCIDL (BAUDCONx<6>)
Auto-Baud Acquisition Rollover Status	ABDOVF (BAUDCON<7>)	ABDOVF (BAUDCONx<7>)

Note 1: PIC18FXXK80 bits associated with EUSART1 have a second definition in the tool chain for PIC18FXX80 bit names for backward compatibility.

New PIC18FXXK80 Features

- The PIC18FXXK80 device has two EUSART modules
- The Data/Receive Polarity Select bit RXDTP (BAUDCONx<5>) is available and the polarity of the RX pin (Asynchronous mode) and DT pin (Synchronous mode) can be configured
- The Synchronous Clock Polarity Select bit, TXCKP (BAUDCONx<4>), is applicable in Asynchronous mode

Unsupported PIC18FXX80 Features

All of the PIC18FXX80 EUSART features are supported by PIC18FXXK80 devices.

Migration Considerations

With higher baud rates of up to 64 MHz supported, PIC18FXXK80 devices clock speeds of up to 64 MHz (PIC18FXX80 devices clock speeds go up to 40 MHz). All of the PIC18FXX80 devices baud rates are supported by PIC18FXX80 devices, which also provide configurations to reduce the baud rate error percentage.

12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D)

PIC18FXX80 devices have a 10-bit A/D Converter, while PIC18FXXK80 devices have a 12-bits with a sign bit A/D Converter.

The converter in PIC18FXXK80 devices is a differential A/D Converter (with two inputs), while PIC18FXX80 devices have a single input. The PIC18FXXK80 devices differential A/D Converter can be configured as a single input A/D Converter by connecting the negative input internally to AVSS.

TABLE 24: A/D CONVERTER COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
A/D Resolution	10-bit	12-bit plus one sign bit
Number of Analog Channels (28-pin)	Eight	Eight
Number of Analog Channels (40-pin)	11	11
Number of Analog Channels (64-pin)	12	11
Modes of Operation	Single input	Differential
A/D Trigger Sources	One	Four
Operation During Sleep	Yes	Yes

TABLE 25: A/D CONVERTER BIT NAMING CONVENTION AND FUNCTIONALITY

Functionality	PIC18FXX80	PIC18FXXK80
Channel Select	CHS<3:0> (ADCON0<5:2>)	CHS<4:0> (ADCON0<6:2>) CHSN<2:0> (ADCON1<2:0>)
Port Configuration Bits	PCFG<3:0> (ADCON1<3:0>)	ANSEL<14:0> (ANCON1<6:0>, ANCON0<7:0>)
A/D Reference Voltage Select Bits	VCFG<1:0> (ADCON1<5:4>)	VCFG<1:0> (ADCON1<5:4>)
Trigger Selection Bits	CCP1M<3:0> (CCP1CON<3:0>)	TRIGSEL<1:0> (ADCON1<7:6>)
A/D Result Registers	ADRESH, ADRESL	ADRESH, ADRESL

New PIC18FXXK80 Features

PIC18FXXK80 devices have the following new features:

- A differential A/D Converter capable of measuring the differential voltage between two channels
- Increased resolution that enables more accurate digital values of corresponding analog signals and a sign bit that indicates A/D results polarity
- VDDCORE and band gap voltages that can be measured by selecting the appropriate channel
- Channel connections that are internal to the source, so no external connections are required and five Channel Select bits, CHS<4:0>, for accessing more channels
- Increased A/D trigger sources, so the module can be triggered from four different sources: ECCP1, CCP2, TIMER1 and CTMU

  (PIC18FXX80 devices have only one trigger source, ECCP1).
- Two internal A/D VREF+ sources (2.05V, typical and 4.10V, typical), in addition to the external VREF and AVDD, that can be used as VREF+
- The ability to reduce power consumption by shutting off the module through the disable bit, PMD_ADC (PMD2<5>)

  The module is enabled by default on POR.

Unsupported PIC18FXX80 Features

PORTB has three Analog Channels, AN8, AN9 and AN10. By default, on POR, these channels are analog.

PIC18FXX80 devices can change the POR value of these PORTB pins to digital by clearing their A/D enable bit, PBADEN (CONFIG3H<1>). PIC18FXXK80 devices do not have this ability through the Configuration Word, requiring the change be made through the ANCON2 register.

Migration Considerations

PIC18FXX80 and PIC18FXXK80 devices multiplex all analog channels and external VREF signals with the same ports pins, so no hardware changes are required.

PIC18FXX80 devices select the port configuration through the PCFG<3:0> bits (ADCON1<3:0>). PIC18FXXK80 devices do this through the individual port pins corresponding ANSELx bits of the ANCON1 and ANCON2 registers.

PIC18FXXK80 devices have changed the bit names and functionality of ADCON1 register, so care must be taken in configuring that register.

COMPARATOR MODULE

This module has two input comparators. These inputs can be configured to use any one of multiple pin inputs, as well as a voltage reference input from the Comparator Voltage Reference Generator (CV_{REF}).

Benefits of the PIC18FXXK80 comparator module:

- Each comparator has a dedicated Configuration bit (CMxCON<7>) to enable or disable the module
- Each comparator has its own Comparator Output Enable bit, COE (CMxCON<6>), that makes the output available on the CMPxOUT pin
- Trigger/interrupt polarity can be selected for individual comparators and configured for low-to-high or high-to-low transitions, or any change of the comparator output

TABLE 26: COMPARATOR COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
Number of Comparators (28-pin)	0	2
Number of Comparators (40/44/64-pin)	2	2
Internal Band Gap Reference Option	No	Yes
Selectable Interrupt Edge	No	Yes
Individual Comparator Interrupts	No	Yes

TABLE 27: COMPARATOR BIT NAMING CONVENTION AND FUNCTIONALITY

Functionality	PIC18FXX80	PIC18FXXK80
Comparator Output	CxOUT (CMCON<7:6>)	CMPxOUT (CMSTAT<7:6>)
Comparator Output Polarity	CxINV (CMCON<5:4>)	CPOL (CM1CON<5>, CM2CON<5>)
Comparator Mode	CIS (CMCON<3>) CM<2:0> (CMCON<2:0>)	CCH<1:0> (CMxCON<1:0>)

New PIC18FXXK80 Comparator Features

PIC18FXXK80 devices have the following new features for improving flexibility and reducing CPU overhead.

- Separate CMCON registers for each comparator, providing flexibility to individually configure each comparator
- Individual interrupts for each comparator
- The ability to configure individual comparator interrupts for any of the following occurrences using the EVPOL<1:0> bits:
  - Low-to-high transition of the comparator output
  - High-to-low transition of the comparator output
  - Any change in the comparator output
- Fixed internal reference voltage on the inverting terminal, if desired

Unsupported PIC18FXX80 Features

PIC18FXX80 devices have no comparator functions that are unsupported by the PIC18FXXK80.

Migration Considerations

All PIC18FXX80 comparator functions can be supported with PIC18FXXK80 devices. However, migration requires a source code rewrite, due to changes in the control registers, CMxCON and CMSTAT.

There are no migration considerations for PIC18F2X80 devices since they do not have comparators.

COMPARATOR VOLTAGE REFERENCE MODULE

The comparator voltage reference module is a resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it may also be used independently of them.

The comparator voltage reference module is controlled through the CVRCON register.

The comparator reference supply voltage can come from either AVDD and AVSS, or the external VREF+ and VREF- inputs, as specified by the CVRSS bit (CVRCON<5>).

TABLE 28: CVREF COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
Available in 28-Pin Device?	No	Yes
Available in 40/64-Pin Device?	Yes	Yes
Number of Taps	16	32
Range Selection?	Yes	No

TABLE 29: CVREF BIT NAMING CONVENTION AND FUNCTIONALITY

Functionality	PIC18FXX80	PIC18FXXK80
Reference Enable	CVREN (CVRCON<7>)	CVREN (CVRCON<7>)
Output Enable	CVROE (CVRCON<6>)	CVROE (CVRCON<6>)
Range Selection	CVRR (CVRCON<5>)	N/A
Source Selection	CVRSS (CVRCON<4>)	CVRSS (CVRCON<5>)
Value Selection	CVR3:0 (CVRCON<3:0>)	CVR<3:0> (CVRCON<3:0>)

Unsupported PIC18FXX80 Features

PIC18FXX80 devices have no CVREF functions that are unsupported by the PIC18FXXK80.

New PIC18FXXK80 Features

PIC18FXXK80 devices have a single voltage range with improved resolution and range. For information on the available voltages, range and functionality, see the PIC18FXXK80 data sheet. (See **“References” on page 27**).

Migration Considerations

The following changes to the CVREF module need to be considered when migrating from the PIC18FXX80 to PIC18FXXK80:

- There is no Comparator VREF Range Selection bit (CVRR) in PIC18FXXK80 devices, meaning those devices will have a single, expanded range
- For PIC18FXXK80 devices, the CVREF voltage resolution is based on 32 levels, unlike PIC18FXX80 devices’ 16 or 32 levels

  The PIC18FXX80 voltage reference provides two ranges of output voltage, each with 16 distinct levels. The range is selected by the CVRR bit (CVRCON<5>).

HIGH/LOW-VOLTAGE DETECT (HLVD)

Both PIC18FXXK80 and PIC18FXX80 devices have one HLVD module.

TABLE 30: HLVD COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
HLVD Modules	1(1)	1
Programmable Level and Direction?	Yes	Yes
16 Configurable Voltage Detection?	Yes	Yes
External Reference?	Yes	Yes
Band Gap Reference Stable Status?	Yes	Yes

Note 1: PIC18F6680 has an LVD module and can only detect dropping voltages. Refer to the *PIC18F6585/8585/6680/8680 Family Data Sheet* (DS30491) for details.

TABLE 31: HLVD BIT NAMING CONVENTION AND FUNCTIONALITY

Functionality	PIC18FXX80	PIC18FXXK80
Band Gap Reference Voltages Stable Status Flag	IRVST (HLVDCON<5>)	BGVST (HLVDCON<6>)

New PIC18FXXK80 Features

PIC18FXXK80 devices have no new features on the HLVD module.

Unsupported PIC18FXX80 Features

All PIC18FXX80 HLVD features are supported by the PIC18FXXK80.

Migration Considerations

No other migration considerations are needed.

ENHANCED CAN MODULE (ECAN)

The PIC18FXXK80 ECAN peripheral has not changed significantly from the PIC18FXX80 implementation.

Many of the PIC18FXX80 control, status and control bits have corresponding PIC18FXXK80 bits. Both implementations support six selectable RX/TX CAN buffers, in addition to two dedicated receive buffers and three dedicated transmit buffers, CAN message time-stamping and wake-up on received CAN messages.

The PIC18FXXK80 family, however, allows relocation of the CAN pins to alternate locations, providing greater flexibility of pin/peripheral assignments.

TABLE 32: ENHANCED CAN COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
Number of RX Buffers	Two	Two
Number of TX Buffers	Three	Three
Number of TX/RX Buffers	Six	Six
DeviceNet™ Support?	Yes	Yes
CAN Pin Relocation?	No	Yes
CAN Message Time Stamp?	Yes	Yes

TABLE 33: ECAN BIT NAMING CONVENTION AND FUNCTIONALITY

Feature Description	PIC18FXX80	PIC18FXXK80
Enhanced CAN Control Register	ECANCON	ECANCON
FIFO High Watermark	FIFOWM (ECANCON<5>)	FIFOWM (ECANCON<5>)
Communication Status Register	COMSTAT	COMSTAT
CAN I/O Control Register	CIOCON	CIOCON
CAN TX2 Data Source (64-pin only)	N/A	TX2SRC (CIOCON<7>)
CAN TX3 Enable (64-pin only)	N/A	TX2EN (CIOCON<6>)
CAN Control Register	CANCON	CANCON
CAN Status Register	CANSTAT	CANSTAT
Receive Buffer Data Register *n* = <0,1>, *m* = <0-7>	RXBnDm	RXBnDm
Receive Buffer Data Length Code Register *n* = <0,1>	RXBnDLC	RXBnDLC
Receive Buffer Extended Identifier Low *n* = <0,1>	RXBnEIDL	RXBnEIDL
Receive Buffer Extended Identifier High *n* = <0,1>	RXBnEIDH	RXBnEIDH
Receive Buffer Standard Identifier Low *n* = <0,1>	RXBnSIDL	RXBnSIDL
Receive Buffer Standard Identifier High *n* = <0,1>	RXBnSIDH	RXBnSIDH
Receive Buffer Control Register *n* = <0,1>	RXBnCON	RXBnCON
Transmit Buffer Data Register *n* = <0-2>, *m* = <0-7>	TXBnDm	TXBnDm
Transmit Buffer Data Length Code Register *n* = <0-2>	TXBnDLC	TXBnDLC
Transmit Buffer Extended Identifier Low *n* = <0-2>	TXBnEIDL	TXBnEIDL
Transmit Buffer Extended Identifier High *n* = <0-2>	TXBnEIDH	TXBnEIDH
Transmit Buffer Standard Identifier Low *n* = <0-2>	TXBnSIDL	TXBnSIDL
Substitute Remote Request Bit	N/A	SRR (RXBnSIDL<4>)
Transmit Buffer Standard Identifier High *n* = <0-2>	TXBnSIDH	TXBnSIDH
Transmit Buffer Control Register *n* = <0-2>	TXBnCON	TXBnCON
Receive Mask Extended Identifier Low *n* = <0,1>	RXMnEIDL	RXMnEIDL
Receive Mask Extended Identifier High *n* = <0,1>	RXMnEIDH	RXMnEIDH
Receive Mask Standard Identifier Low *n* = <0,1>	RXMnSIDL	RXMnSIDL
Substitute Remote Request	N/A	SRR (RXMnSIDL<4>)
Receive Mask Standard Identifier High *n* = <0,1>	RXMnSIDH	RXMnSIDH
Receive Filter Extended Identifier Low *n* = <0-15>	RXFnEIDL	RXFnEIDL
Receive Filter Extended Identifier High *n* = <0-15>	RXFnEIDH	RXFnEIDH
Receive Filter Standard Identifier Low *n* = <0-15>	RXFnSIDL	RXFnSIDL
Substitute Remote Request		
n = <0-15>	N/A	SRR (RXFnSIDL<4>)
Receive Filter Standard Identifier High *n* = <0-15>	RXFnSIDH	RXFnSIDH
Peripheral Interrupt Priority Register	IPR3	IPR5
Peripheral Interrupt Request Register	PIR3	PIR5
Peripheral Interrupt Enable Register	PIE3	PIE5
Receive Filter Enable Register 1	RXFCON1	RXFCON1
Receive Filter Enable Register 0	RXFCON0	RXFCON0
Baud Rate Control	BRGCON3	BRGCON3
Baud Rate Control	BRGCON2	BRGCON2
Baud Rate Control	BRGCON1	BRGCON1
Transmit Error Count	TXERRCNT	TXERRCNT
Receive Error Count	RXERRCNT	RXERRCNT

TABLE 33: ECAN BIT NAMING CONVENTION AND FUNCTIONALITY (CONTINUED)

Feature Description	PIC18FXX80	PIC18FXXK80
TX/RX Buffer Data Register	BnDm	BnDm
TX/RX Buffer Data Length Code	BnDLC	BnDLC
TX/RX Buffer Extended Identifier Low	BnEIDL	BnEIDL
TX/RX Buffer Extended Identifier High	BnEIDH	BnEIDH
TX/RX Buffer Standard Identifier Low	BnSIDL	BnSIDL
Substitute Remote Request	N/A	SRR (BnSIDL<4>)
TX/RX Buffer Standard Identifier High	BnSIDH	BnSIDH
TX/RX Buffer Control Register	BnCON	BnCON
Buffer Select Register	BSEL0	BSEL0
Device Net Count Register	SDFLC	SDFLC
Receive Filter Buffer Control Register *x* = <0-7>, *n* = <1,3,5,7,9,11,13,15>, *m* = <0,2,4,6,8,10,12,14>	RXFBCONx	RXFBCONx
Mask Select Register *n* = <0-3>	MSELn	MSELn
Transmit Buffer Interrupt Enable	TXBIE	TXBIE
Buffer Interrupt Enable	BIE0	BIE0

New PIC18FXXK80 Features

ECAN pins relocation is a new feature available on the PIC18FXXK80 to improve the flexibility of application implementation.

PIC18FXXK80 devices have a CTMU peripheral that shares the RB2/RB3 pins with the ECAN peripheral. To allow use of the CTMU and ECAN simultaneously, the ECAN pins can be moved to alternate I/O pins with the CANMX bit (CONFIG3H<0>). The alternate location on the 40/44LD and 28LD devices is RC6/RC7. On the 64LD device, the alternate location is RE4/RE5.

Unsupported PIC18FXX80 Features

All of the PIC18FXX80 ECAN features are supported on the PIC18FXXK80.

Migration Considerations

The only significant issue with migrating is that the maximum input oscillator frequency, in HS mode, is reduced from 25 MHz on PIC18FXX80 devices to 16 MHz on PIC18FXXK80 devices.

For more details, see the oscillator section of the PIC18FXXK80 data sheet. (See **"References" on page 27**).

VREG

PIC18FXXK80 devices have an on-chip voltage regulator while PIC18FXX80 devices do not.

With the internal regulator, an external LDO is not required to provide the separate core supply. It also permits the device to run at a higher VDD. It requires a 10 µF, low Equivalent Series Resistance (ESR) capacitor, like ceramic or tantalum, on the VCAP pin.

A second regulator is available to reduce power consumption in Sleep modes. This option permits the main LDO to be disabled and uses a low-power regulator to maintain data memory and port logic levels in these modes.

TABLE 34: VREG COMPARISONS

Feature Description	PIC18FXX80	PIC18FXXK80
On-Chip Voltage Regulator	No	Yes(1)

Note 1: PIC18LFXXK80 devices do not have an on-chip voltage regulator.

New PIC18FXXK80 Features

The on-chip voltage regulator powers the core digital logic at a nominal 3.3V. For designs that are required to operate at a higher typical voltage, such as 5V, all family devices incorporate two on-chip regulators that allow the device to run its core logic from VDD.

Those regulators are:

- Normal On-Chip Regulator (for Run mode)
- Ultra Low-Power On-Chip Regulator (for Sleep mode)

Unsupported PIC18FXX80 Features

There are no VREG features on the PIC18FXX80 that are unsupported by the PIC18FXXK80.

Migration Considerations

PIC18FXXK80 devices require that a 10 µF, low-ESR external capacitor, such as ceramic or tantalum, be connected on the VCAP pin. This regulator is present only on the "F" versions of the PIC18FXXK80 family, not on the "LF" devices.

PACKAGE INFORMATION

PIC18FXX80 and PIC18FXXK80 devices share the same packages, which permits easier migration and minimal hardware change from existing designs.

PIC18FXXK80 devices also offer four additional packages. A comparison of the two families is shown in Table 35.

TABLE 35: AVAILABLE PACKAGE COMPARISON

Package	PIC18FXX80	PIC18FXXK80
28-Pin PDIP	Yes	Yes
28-Pin SOIC	Yes	Yes
28-Pin SSOP	No	Yes
28-Pin QFN	No	Yes
40-Pin PDIP	Yes	Yes
44-Pin TQFP	Yes	Yes
44-Pin QFN	Yes	Yes
64-Pin TQFP	Yes	Yes
64-Pin QFN	No	Yes

New PIC18FXXK80 Packages

The following are descriptions of the *new* packages available on the PIC18FXXK80:

- 28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length
- 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]
- 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
- 64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

For specific package information, see the “Package Specification” document (DS00049) on the Microchip web site:

www.microchip.com

Shared PIC18FXXK80 Packages

The following are descriptions of the packages that PIC18FXXK80 devices *share* with PIC18FXX80 devices:

- 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]
- 28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]
- 40-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]
- 44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm Footprint [TQFP]
- 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

For additional package information, see the “Packaging Information” section of the PIC18FXXK80 data sheet. (See **“References” on page 27**).

Migration Considerations

When migrating to a shared package, there are a couple of changes that have to be considered with regards to the hardware design.

Because the RA4/T0CKI pin has been replaced by the V_{CAP}/V_{DDCORE} pin, the pin is no longer used as an I/O. Instead, it is directly connected to the voltage input to the CPU core and either the voltage regulator output (for “F” devices) or the supply voltage (for “LF” devices). Although not required, it is good design practice to have sufficient decoupling capacitors on this pin.

The input for the T0 clock, which was previously on the RA4 pin, is now available on one of two pins with a multiplex Configuration bit that specifies either pin RG4 or RB5. Because PORTG is unimplemented for 28 and 40/44-pin devices, this pin selection feature is only available for 64-pin devices. For 28 and 40/44-pin devices, the T0 clock input is only available on RB5.

SUMMARY

The preceding sections present the most important considerations in moving a PIC18FXX80 application to a PIC18FXXK80 device. Although it is impractical to list every possible code to hardware implementation, this document has provided a checklist of the most important differences and similarities.

Additional features, such as Charge Time Measurement Unit, 1.8V operation and 12-bit A/D, provide new applications for the PIC18FXXK80 family that were not possible with previous device families. Ultimately, users must review their application designs and implementations to decide how their code and hardware design must be changed for the new PIC18FXXK80 device family.

REFERENCES

For more specific information on the device families referenced in this document, see the following data sheets:

- *PIC18F66K80 Family Data Sheet* (DS39977)
- *PIC18F2480/2580/4480/4580 Data Sheet* (DS39637)
- *PIC18F2585/2680/4585/4680 Data Sheet* (DS39625)
- *PIC18F6585/8585/6680/8680 Family Data Sheet* (DS30491)

Detailed information on oscillator design and trouble-shooting for PIC® microcontroller applications are provided in these Microchip application notes:

- Steven Bible, AN826, *"Crystal Oscillator Basics and Crystal Selection for rfPIC® and PICmicro® Devices"* (DS00826), Microchip Technology Inc., 2002.
- Brett Duane, AN949, *"Making Your Oscillator Work"* (DS00949), Microchip Technology Inc., 2004.
- Ruan Lourens, AN943, *"Practical PICmicro® Oscillator Analysis and Design"* (DS00943), Microchip Technology Inc., 2004.
- Dan Mathews, AN849, *"Basic PICmicro® Oscillator Design"* (DS00849), Microchip Technology Inc., 2002.

Microchip has other data sheets and reference materials for PIC18F, PIC18FXXJ Flash and PIC24F devices that may be helpful in planning the migration of an application. For a complete listing of available materials, visit the Microchip corporate web site at:

www.microchip.com

DOCUMENT REVISION HISTORY

Rev A Document (8/2010)

The original release of this document with the introduction of the PIC18FXXK80 family and the details on migrating from the PIC18FXX80 family.

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