Description of Design:

MCLK --> 55.55MHz (Global Clock)
P_sel1 --> asynchron external reset
P_data_int --> enable signal for p_data (internal signal)
P_data --> Output pin

VHDL-Code:

```
--/////////Start Process p_data/////////////////

Out_p_data : Process (MCLK,p_sel1)

        --Counter Variable
        type Count is range 0 to 1;
        variable Count_p_data : Count;

begin

if p_sel1 = Low then

        p_data_int <= Low;
        Count_p_data := 0;

 elsif MCLK'event then

                case Count_p_data is

                        when 0 => Count_p_data := 1;
                                  p_data_int <= high;

                        when 1 => Count_p_data := 0;
                                  p_data_int <= low;

                end case;

end if;


end process Out_p_data;

--///////////End Process p_data/////////////
```

```
--////Start Process Sync p_data//////////////////
Sync_p_data : Process (MCLK,p_sel1, p_data_int)


begin

if p_sel1 = Low then

  p_data <= Low;

-elsif MCLK'event then

    if p_data_int = High then

                                        p_data <= High;

                        else
                                        p_data <= Low;


     end if;
end if;


end process Sync_p_data;

--////////End Process Sync p_data//////////////////
```

Timing Report:

1) Timing Constraint Summary:

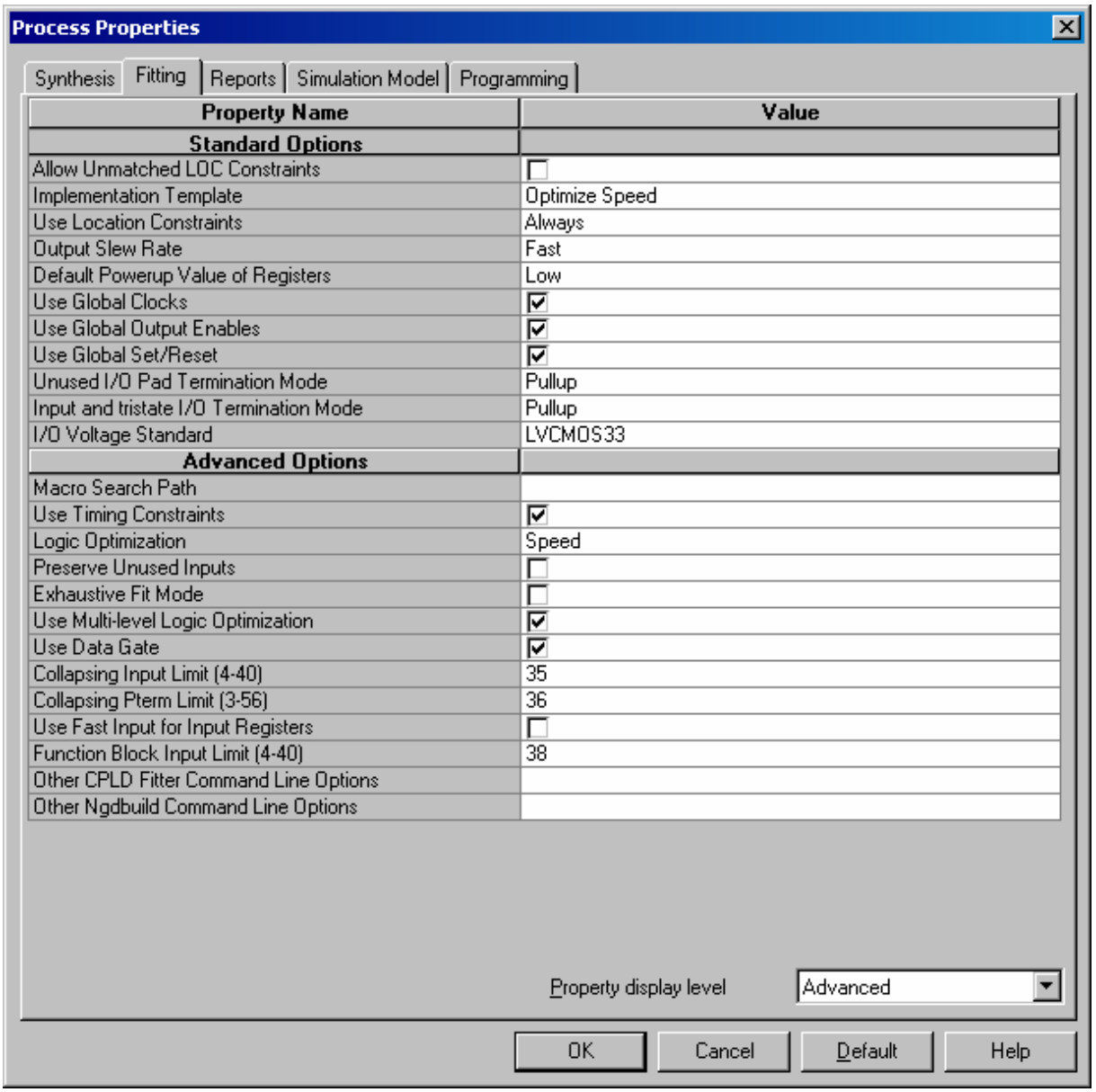
TS_MCLK=PERIOD:MCLK:18.000nS:HIGH:9.000nS Met

2) Clock Pad to Output Pad (tCO) (nsec)

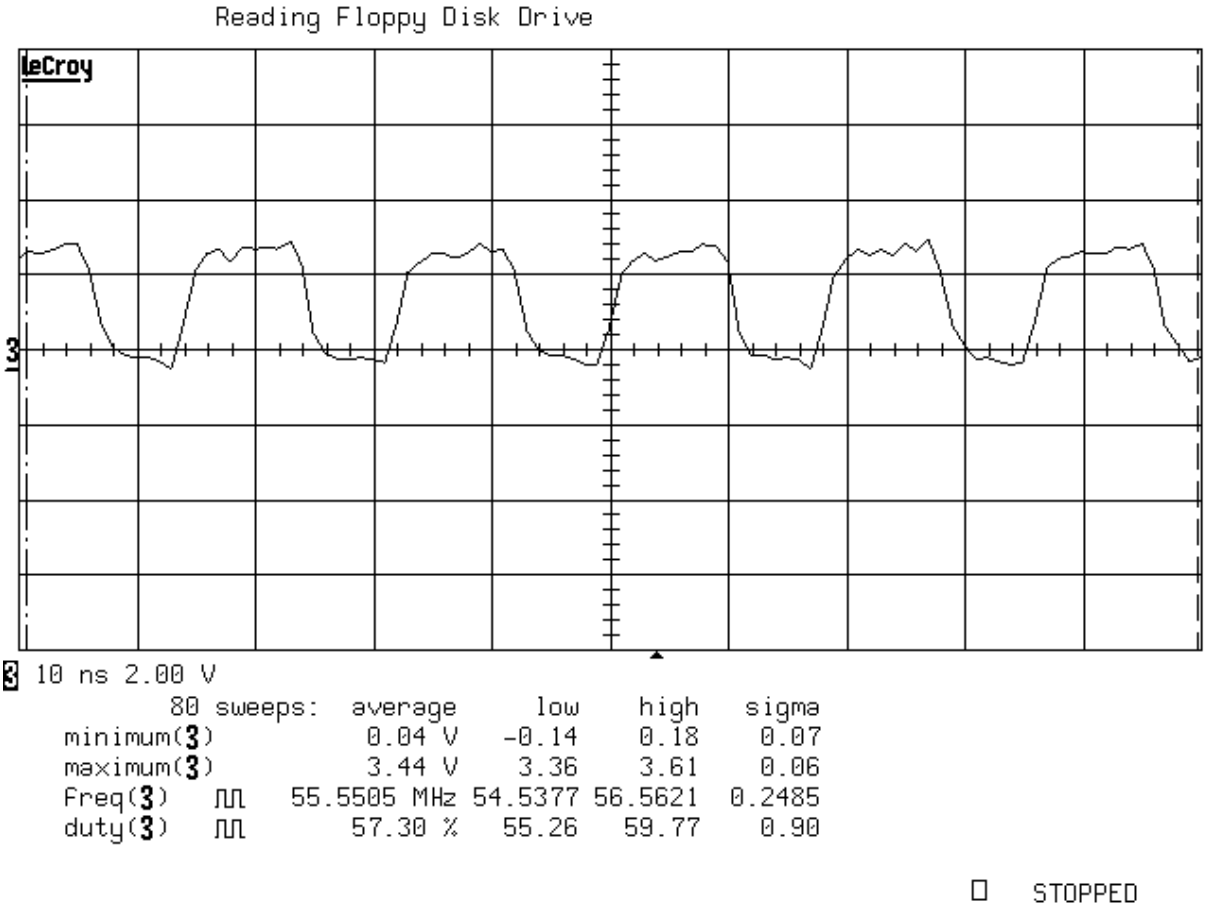
From MCLK

P_DATA 7.5

Process Properties:



Achieved (and measured) Duty Cycle (p_data):



Achieved Clock: 57% --> Must have : 50% - 52%