

## Description of Design:

MCLK --> 55.55MHz (Global Clock)

P\_sel1 --> asynchron external reset

P\_data\_int --> enable signal for p\_data (internal signal)

P\_data --> Output pin

## VHDL-Code:

```
--//////////Start Process p_data//////////
```

```
Out_p_data : Process (MCLK,p_sel1)
```

```
    --Counter Variable
```

```
    type Count is range 0 to 1;
```

```
    variable Count_p_data : Count;
```

```
begin
```

```
if p_sel1 = Low then
```

```
    p_data_int <= Low;
```

```
    Count_p_data := 0;
```

```
elseif MCLK'event then
```

```
    case Count_p_data is
```

```
        when 0 => Count_p_data := 1;
```

```
                p_data_int <= high;
```

```
        when 1 => Count_p_data := 0;
```

```
                p_data_int <= low;
```

```
    end case;
```

```
end if;
```

```
end process Out_p_data;
```

```
--//////////End Process p_data//////////
```

```

--//////Start Process Sync p_data////////////////////////////////////
Sync_p_data : Process (MCLK,p_sel1, p_data_int)

begin

if p_sel1 = Low then

    p_data <= Low;

-elsif MCLK'event then

    if p_data_int = High then

        p_data <= High;

    else

        p_data <= Low;

    end if;

end if;

end process Sync_p_data;

--//////////End Process Sync p_data////////////////////////////////////

```

## Timing Report:

### 1) Timing Constraint Summary:

TS\_MCLK=PERIOD:MCLK:18.000nS:HIGH:9.000nS

Met

### 2) Clock Pad to Output Pad (tCO) (nsec)

From MCLK

P\_DATA        7.5

## Process Properties:

**Process Properties** [X]

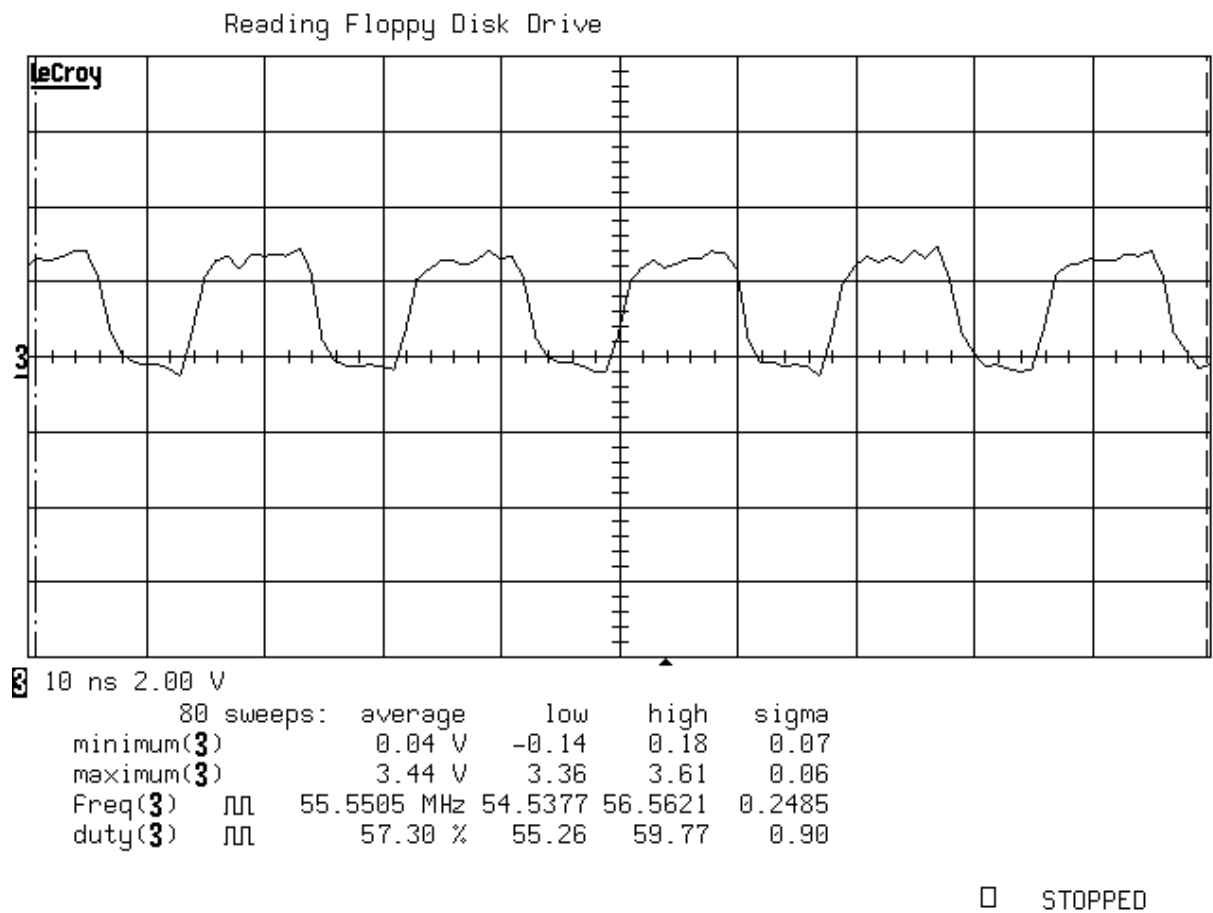
Synthesis Fitting Reports Simulation Model Programming

Property Name	Value
<b>Standard Options</b>	
Allow Unmatched LOC Constraints	<input type="checkbox"/>
Implementation Template	Optimize Speed
Use Location Constraints	Always
Output Slew Rate	Fast
Default Powerup Value of Registers	Low
Use Global Clocks	<input checked="" type="checkbox"/>
Use Global Output Enables	<input checked="" type="checkbox"/>
Use Global Set/Reset	<input checked="" type="checkbox"/>
Unused I/O Pad Termination Mode	Pullup
Input and tristate I/O Termination Mode	Pullup
I/O Voltage Standard	LVC MOS33
<b>Advanced Options</b>	
Macro Search Path	
Use Timing Constraints	<input checked="" type="checkbox"/>
Logic Optimization	Speed
Preserve Unused Inputs	<input type="checkbox"/>
Exhaustive Fit Mode	<input type="checkbox"/>
Use Multi-level Logic Optimization	<input checked="" type="checkbox"/>
Use Data Gate	<input checked="" type="checkbox"/>
Collapsing Input Limit (4-40)	35
Collapsing Pterm Limit (3-56)	36
Use Fast Input for Input Registers	<input type="checkbox"/>
Function Block Input Limit (4-40)	38
Other CPLD Fitter Command Line Options	
Other Ngdbuild Command Line Options	

Property display level: Advanced

OK Cancel Default Help

Achieved (and measured) Duty Cycle (p\_data):



Achieved Clock: 57% --> Must have : 50% - 52%