The MSP430x1xx Basic Clock System

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ABSTRACT

The MSP430 family of microcontrollers offers designers a unique blend of 16-bit processing power, flexible and easy to use peripherals, and ultra low-power consumption. In a typical 3-V application running at 1 MHz, single cycle 16-bit instructions are executed at one million instructions per second, with a current consumption of only 400 μA. True, real-time interrupt handling can now be achieved with the MSP430's rapid wake up from low power mode 3 (only 1.5-μA current consumption) to fully active mode in only 6 μS.

These remarkable capabilities are direct results of two of the MSP430's most interesting design features: the 16-bit RISC-like architecture, and the clock/oscillator subsystem.

The newest member of the MSP430 family, the MSP430x1xx, introduces a new clock system. The basic clock system is simpler than its predecessor, but is more flexible. This document describes the basic clock system in detail.

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1 The Oscillators

The basic oscillator system is composed of up to three oscillators. These three oscillator blocks form the basis of all MSP430x1xx clock systems. The exact configuration is device dependent, however. For example, the MSP430x11x has only two of the three possible blocks – the LF/XT1 and the DCO.

1.1 The LF/XT1 Oscillator

The ultralow-power 32-kHz oscillator has been retained from the MSP430x3xx clock system, but it has been further enhanced by the addition of a software-selectable high-frequency mode. In this high-frequency mode, the oscillator operates with ceramic resonators and quartz crystals in the frequency range 450 kHz to 8 MHz. However, in this high-frequency mode the current consumption of the oscillator is significantly increased when compared to operation at 32 kHz. Figure 1 shows the LF/XT1 oscillator block diagram.

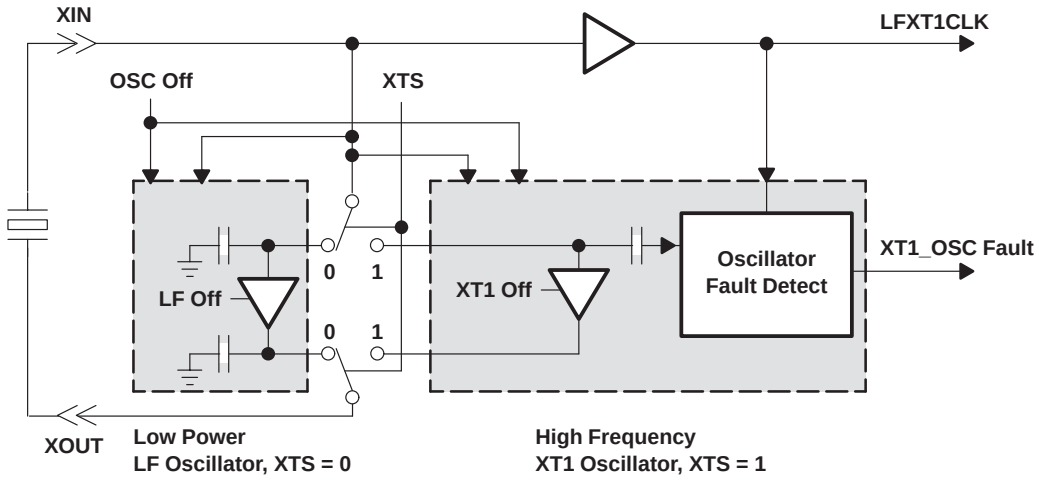


Figure 1. The LF/XT1 Oscillator

The OscOff control bit allows the oscillators to be shut down when not required, to save power. The XTS control bit allows the application software to select either 32-kHz operation (with a 32-kHz quartz crystal) or high-frequency operation (450 kHz to 8 MHz) with a ceramic resonator or quartz crystal.

Additional external capacitors are required on the XIN and XOUT pins when operating this oscillator in high-frequency mode (see characterization information at the end of this document). No additional capacitance is required when used with a 32-kHz crystal, as 12-pF capacitors are integrated onto the device.

1.2 The XT2 Oscillator

The XT2 oscillator is identical to the high-frequency oscillator section of the LF/XT1 oscillator. It does not support the LF (32 kHz) mode of operation. Figure 2 shows the XT2 oscillator block diagram. Additional external capacitors are required on the XT2IN and XT2OUT pins.

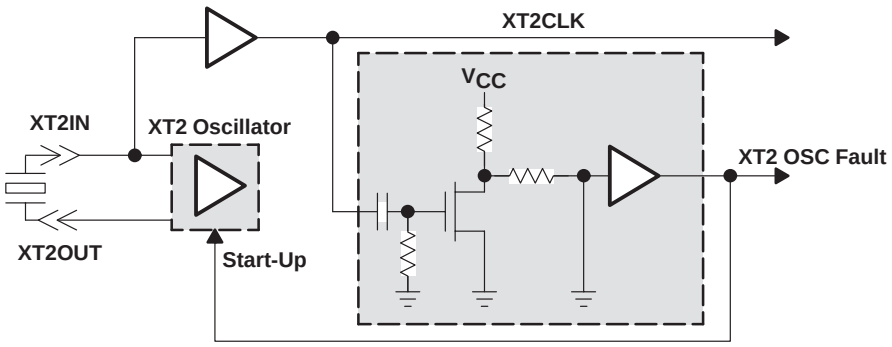


Figure 2. The XT2 Oscillator

1.3 The Digitally Controlled Oscillator (DCO)

The basic clock system DCO is identical to the DCO used in the frequency-locked-loop (FLL) system of the MSP430x3xx family, but it has 8 rather than 32 frequency taps, and it does not have the FLL feedback loop, that is, it is a free running DCO. The modulator is identical to the one in the FLL system. Figure 3 shows the DCO block diagram.

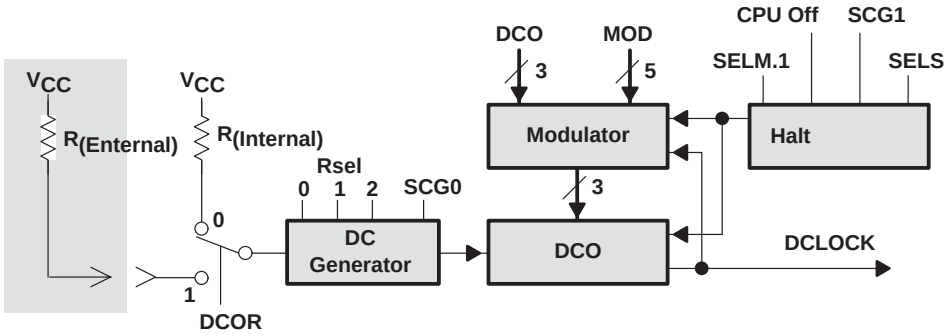


Figure 3. The DCO

The DCO's output frequency, DCOCLK, is dependent upon three factors:

- The current injected into the dc generator dictates the basic frequency range in which the DCO operates. This current is controlled by either an external or an internal resistor. The D_{COR} bit selects the internal or external resistor option. The three control bits $R_{SEL.0}$, $R_{SEL.1}$ and $R_{SEL.2}$ select one of eight DCO ranges by modifying the injected current.
- The three DCO control bits, $D_{CO.2}$ . . . $D_{CO.0}$ modify the frequency around the nominal frequency by selecting one of the eight frequency taps as the output. Each tap has a frequency approximately 10% higher than the previous one.
- The modulator can automatically adjust the frequency tap selected.

Once the DCO range has been set, the DCOCLK output frequency can be fine tuned by software at any time, allowing the application to tailor its operating frequency to suit particular circumstances.

The modulator has the ability to automatically adjust the bit pattern controlling the DCO, effectively causing the DCO to *hop* between two adjacent (f_n and f_{n+1}) frequency taps in one of 32 predefined patterns. This has the effect of making the DCO generate an average output frequency which would correspond to a *fractional tap*. Figure 4 illustrates this *fractional frequency tap* concept.

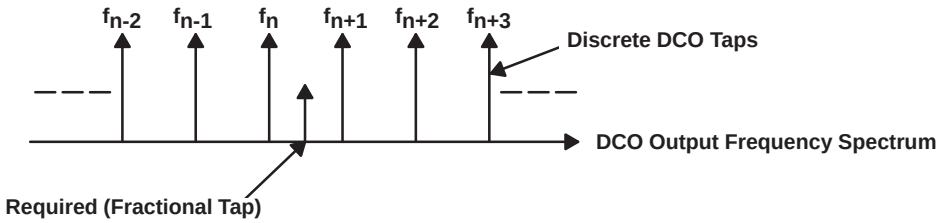


Figure 4. A Fractional DCO Tap Frequency

If an application needs to perform a particularly accurate timing function, it will require a very stable DCOCLK. The modulator's ability to change the DCOCLK frequency automatically could introduce timing errors in such circumstances. The modulator can therefore be disabled by manually selecting hop-pattern 0, that is, writing 0s to the $M_{OD.4}$ . . . $M_{OD.0}$ bits in the DCOCTL register. This leaves the DCO set at the lower of the two adjacent frequency taps. Take care however, to ensure that any particularly sensitive timings are carried out in as short a time as possible to minimize the effects of temperature and supply voltage drifts.

Figure 5 shows some of the 32 modulator hop-patterns available.

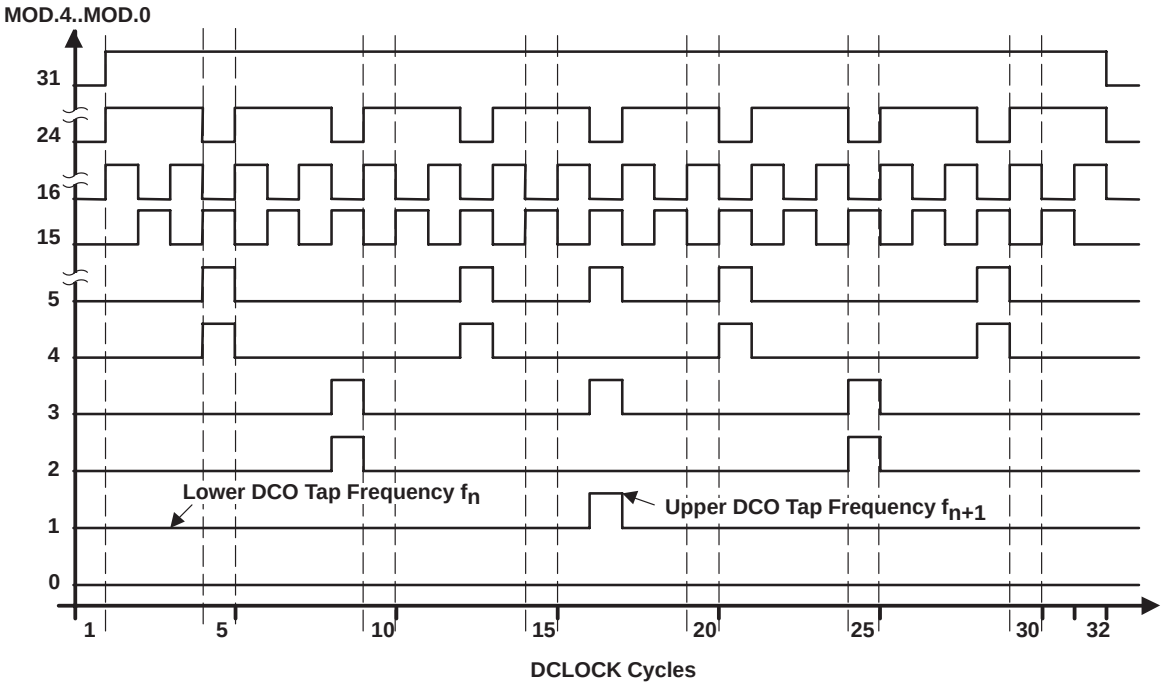


Figure 5. Modulator Hop-Patterns

2 Clock Distribution

The MSP430x3xx clock system provided the CPU and peripherals with a choice of only two internal clock signals, ACLK (32 kHz) driving the peripherals, and MCLK (nominally 500 kHz to 5 MHz) driving the CPU and peripherals. The basic clock system introduces an additional internal clock, SMCLK, specifically for the peripherals.

A new clock distribution block allows the three clock sources (LFXT1, XT2, and DCO) to be connected to the three internal clocks (ACLK, MCLK, and SMCLK) in a wide range of configurations. Additionally, programmable dividers allow the three clock sources to be divided by 1, 2, 4, or 8. Figure 6 shows a block diagram of the oscillators and clock distribution.

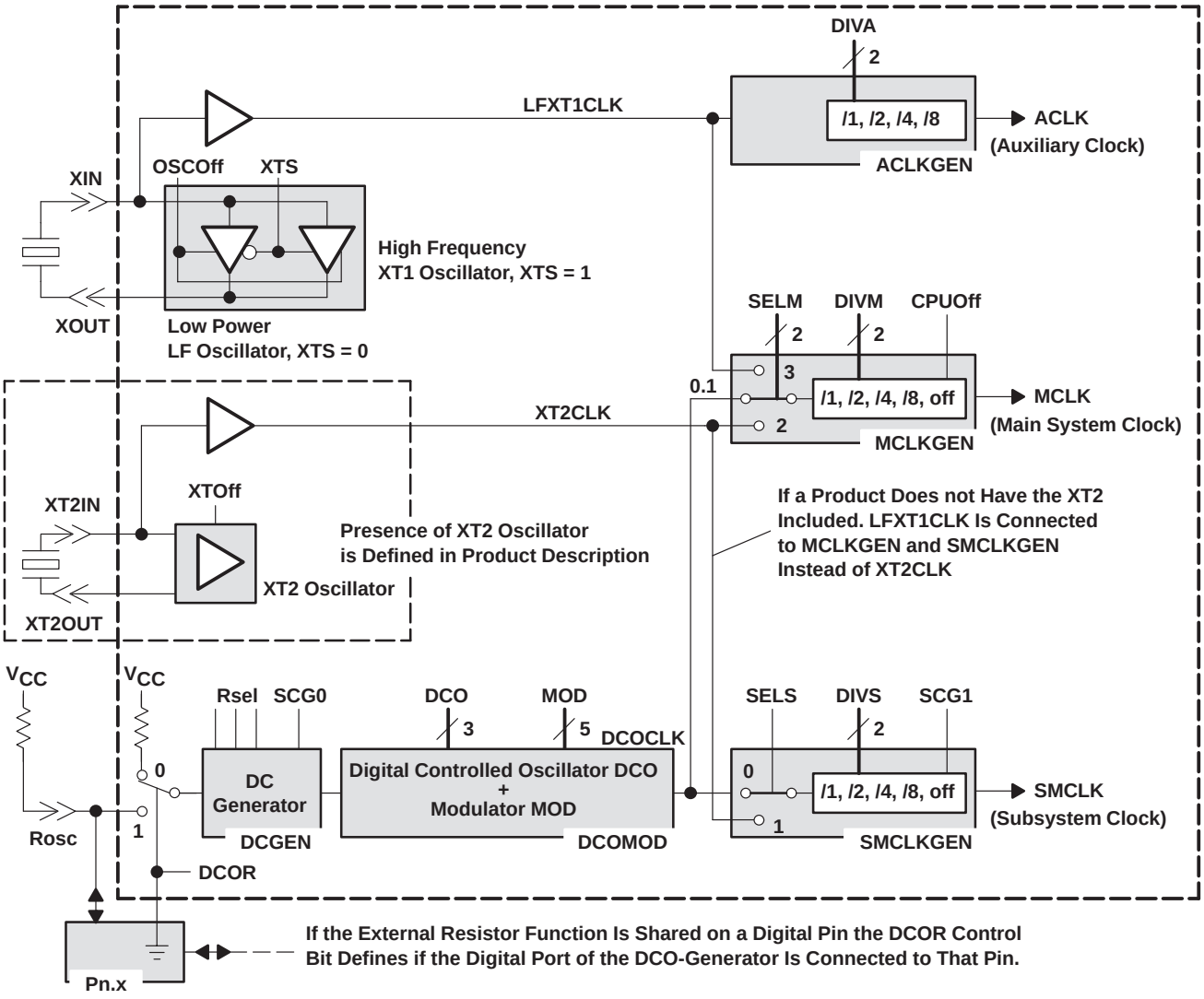


Figure 6. Clock Distribution Block Diagram

The clock distribution system provides a great deal of flexibility as it allows a different clock source to be selected for each of the three internal clock signals ACLK, MCLK, and SMCLK.

2.1 Choice of Oscillator

Use of the DCO has several advantages over crystal- or resonator-based oscillators:

- It is a low-cost solution requiring no external components. If the internal control resistor is unsuitable, an external one may be used instead.
- It starts oscillating immediately, with no start-up delay.

- It has a relatively low operating current.
- Its operating frequency is software selectable.
- Fail-safe operation. Operation reverts back to the internal DCO, with the injected current controlled by the internal resistor, should the external XT1 or XT2 crystal or resonator fail.

It does have some disadvantages, however:

- Its operating current is not as low as the LF (32 kHz) oscillator.
- As with any DCO, its output frequency will drift with supply voltage and temperature.

The temperature and supply voltage drifts occur because the DCO is not part of the frequency-locked-loop arrangement found on the MSP430x3xx family. Also, for any given frequency tap, DCOCLK will vary from device to device. In the simplest of applications this is not a problem, and no further action will be needed.

In applications where a stable DCOCLK frequency is required, a software control loop and a reference frequency/timing may be required. The frequency reference could, for example, be ACLK derived from the LF (32 kHz) oscillator, or it could be derived from the mains supply in mains-powered applications, or it could be derived from a simple external RC circuit. A simple software control loop is implemented, which then adjusts the DCO frequency periodically. Refer to the end of this application report for details of this and other application materials.

Many applications require maximum battery life and/or regular background timer interrupts for a real-time-clock, serial interface, etc. These requirements usually dictate that the LF (32 kHz) oscillator is also used. A 32 kHz ACLK serves a number of functions. It provides a frequency reference for maintaining a stable DCOCLK frequency. When used in conjunction with the MSP430's low-power modes, the operating current is much lower than can be achieved with the DCO. ACLK can be used as the clock source for on-chip timers, which can then generate regular interrupts.

With the new clock distribution system, ACLK can be as low as 4 kHz (32 kHz LFXT1CLK divided by 8), reducing the low power mode operating current even further.

Figure 6 also shows that the CPU clock, MCLK, can now also be derived from LFXT1CLK. The most obvious implication of this is that the CPU can now execute code with an MCLK frequency of only 4 kHz. Although this is not necessary in all applications, it results in a very low and fairly constant average current, which might be advantageous in some cases.

In applications requiring very stable or very precise clock frequencies, the XT1 or XT2 high frequency oscillators can be used.

To achieve optimum performance for a nontrivial application, the clocking system adopted will typically use a combination of DCO and ceramic resonator or quartz crystal. At power-up or reset, MCLK and SMCLK are automatically switched to the DCOCLK source, the internal resistor supplies the necessary current for the DCO's dc-generator, and a central DCO frequency tap is selected. This gives a DCOCLK frequency somewhere in the middle of the available range. Software execution begins immediately, and the application can then configure the clock system as required.

2.2 Basic Clock System Control

Three new control registers have been introduced with the basic clock system. The DCO control register shown in Figure 7, DCOCTL, provides direct access to the DCO and modulator. The basic clock system control registers 1 (Figure 8) and 2 (Figure 9) provide access to all the other control bits. These registers, together with the SCG1, SCG0, OscOff, and CPUOff bits in the status register, provide complete control over the clock system.

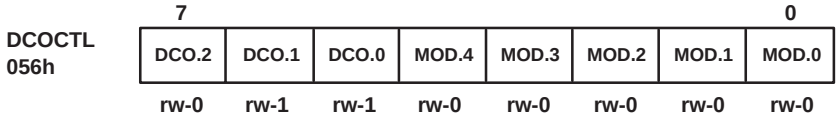


Figure 7. DCO Control Register

$M_{OD.4} \ldots M_{OD.0}$: These bits control the *hop pattern* of the modulator. They define how often the upper frequency tap, f_{n+1} in Figure 4, is used within a period of 32 DCOCLK cycles. For the remaining 32-M_{OD} DCOCLK cycles, the lower frequency tap, $f_{n,}$ is used. When the $D_{CO.2} \ldots D_{CO.0}$ bits are all ones, no modulation is possible, as the highest available frequency tap has then been selected.

$D_{CO.2} \ldots D_{CO.0}$: These bits define which of the eight possible frequency taps is currently selected as the output frequency DCOCLK. The actual output frequency is dependent on the current injected into the dc generator.

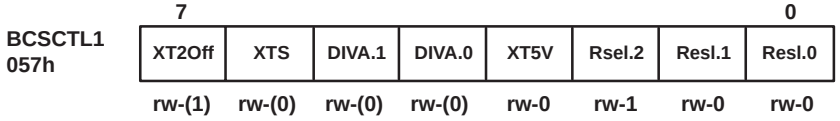


Figure 8. Basic Clock System Control Register 1

$R_{SEL.2} \ldots R_{SEL.0}$: These bits select one of eight possible dc-generator output levels. The output level directly affects the nominal frequency of the DCO. The lowest nominal frequency is selected by setting $R_{SEL.\ 2} \ldots R_{SEL.\ 0}$=0.

XT5V: This bit should always be left as a 0 for best results.

DIVA.1 . . . DIVA.0: The selected clock source for ACLK is divided by:
DIVA.1 . . . DIVA.0 = 00: Divide by 1
DIVA.1 . . . DIVA.0 = 01: Divide by 2
DIVA.1 . . . DIVA.0 = 10: Divide by 4
DIVA.1 . . . DIVA.0 = 11: Divide by 8

XTS: Low/high frequency select for LFXT1 oscillator:
XTS = 0: The low-frequency oscillator is selected.
XTS = 1: The high-frequency oscillator is selected.

The XTS setting must correspond to the type of external crystal connected, because unpredictable results occur if XTS=1 with a 32 kHz crystal attached.

XT2Off: The XT2 oscillator is switched on or off:
XT2Off = 0: The oscillator is on.
XT2Off = 1: The oscillator is turned off, but only if it is not used by MCLK or SMCLK.

The function of XT2Off is only applicable ifXT2 oscillator is implemented.

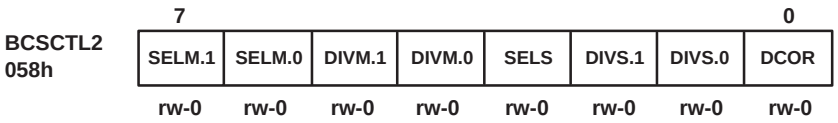


Figure 9. Basic Clock System Control Register 2

DCOR: The DCOR bit selects the internal resistor for injecting current into the dc generator. When activated, the DCO output frequency will depend on this current.
- DCOR = 0: Internal resistor on, the oscillator can operate. The fail safe mode is on.
- DCOR = 1: Internal resistor off, the current must be injected by an external resistor if the DCO output drives any clock using the DCOCLK.

DIVS.1 . . . DIVS.0: The selected clock source for SMCLK is divided by:
- DIVS. 1. . . DIVS. 0 = 00: Divide by 1
- DIVS. 1. . . DIVS. 0 = 01: Divide by 2
- DIVS. 1. . . DIVS. 0 = 10: Divide by 4
- DIVS. 1. . . DIVS. 0 = 11: Divide by 8

SELS: Selects the source for generating SMCLK:
- SELS = 0: Use DCOCLK
- SELS = 1: Use XT2CLK (in a three oscillator system)
  or
  Use LFXT1CLK signal (in a two oscillator system)

DIVM.1 . . . DIVM.0: The selected clock source for MCLK is divided by:
- DIVM.1 . . . DIVM.0 = 00: Divide by 1
- DIVM.1 . . . DIVM.0 = 01: Divide by 2
- DIVM.1 . . . DIVM.0 = 10: Divide by 4
- DIVM.1 . . . DIVM.0 = 11: Divide by 8

SELM.1 . . . SELM.0: Selects the source for generating MCLK:
- SELM.1 . . . SELM.0 = 00: Use DCOCLK
- SELM.1 . . . SELM.0 = 01: Use DCOCLK
- SELM.1 . . . SELM.0 = 10: Use XT2CLK
- SELM.1 . . . SELM.0 = 11: Use LFXT1CLK

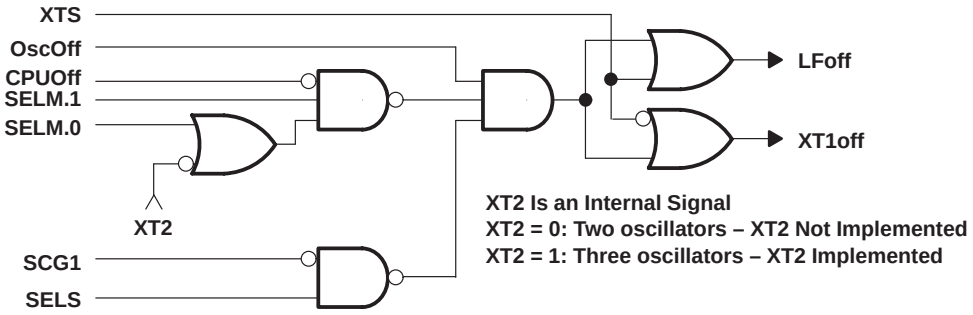
2.3 Oscillator Shutdown, Fail Safe Operation

The extra flexibility of the basic clock system means that the different oscillators cannot simply be shut down at any time. For example, what would happen if an application stopped the DCO when the CPU's MCLK was dependent on DCOCLK?

Thankfully, most of the complexity associated with deciding under what circumstances the oscillators can be stopped is taken care of by internal logic. The following truth tables and logic diagrams show the relationships between the various signals for the different oscillators.

2.3.1 LF/XT1 Oscillator

Figure 10 shows the internal logic which prevents the LF/XT1 oscillator being stopped if either MCLK or SMCLK are dependent upon it.



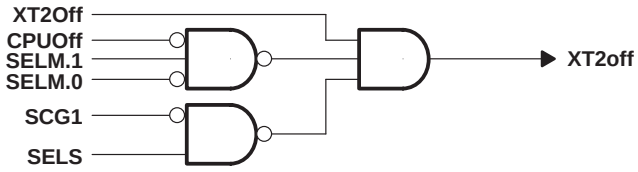
OscOff	CPUOff	SELM.x	SCG1	SELS	LFXT1CLK	Comment
0	x	x	x	x	on	Oscillator Active
1	0	3 or 2+3†	x	x	on‡	Clock sig. Needed for MCLK
1	x	x	0	1	on‡	Clock sig. Needed for SMCLK

† Two oscillators: SELM.x = 3 and 2. Three oscillators: SELM.x = 3.
‡ LFXT1CLK is switched off in all other bit combinations

Figure 10. LF/XT1 Oscillator Shutdown Control Logic

2.3.2 XT2 Oscillator

Figure 11 shows the internal logic which prevents the XT2 oscillator being stopped if either MCLK or SMCLK are dependent upon it.



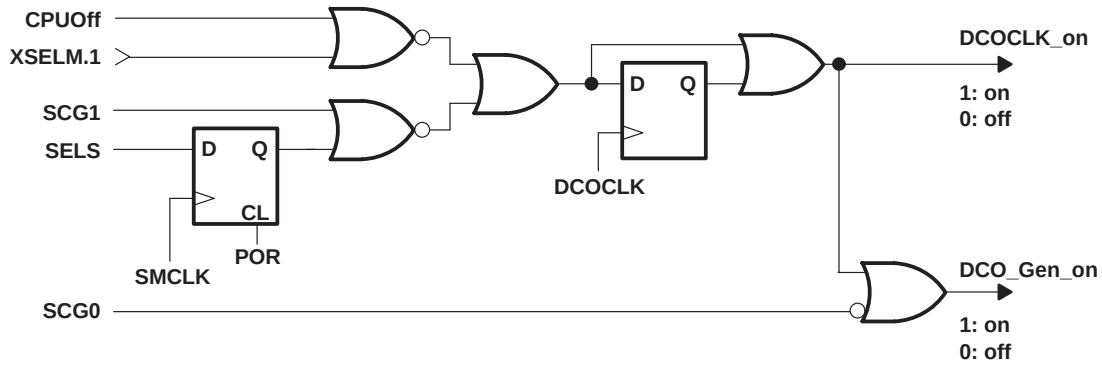
OscOff	CPUOff	SELM.x	SCG1	SELS	LFXT1CLK	Comment
0	x	x	x	x	on	Oscillator Active
1	0	2	x	x	on†	Clock sig. Needed for MCLK
1	x	x	0	1	on†	Clock sig. Needed for SMCLK

† XTCLK is Switched off in all other bit combinations

Figure 11. XT2 Oscillator Shutdown Control Logic

2.3.3 DCO

Figure 12 shows the internal logic which prevents the dc generator or the DCO being switched off if either MCLK or SMCLK are dependent upon them.



SCG0	CPUOff	XSELM.1	SCG1	SELS	DCOCLK	DCOGEN	Comment
x	0	0	x	x	on	on	DCO Clock Needed for MCLK
x	x	x	0	0	on	on	DCO Clock Needed for SMCLK
0	0	1	(see Note A)		off	on	DCO Clock is not Needed
0	1	x			off	on	for MCLK (and SMCLK)
0	(see Note B)		0	1	off	on	DCO Clock is not Needed
0			1	X	off	on	for SMCLK (and MCLK)
1	(see Note C)				off	off	DCO Clock is not Needed: SCG0 Bit Switch off DCOGEN

NOTES: A. SMCLK does not need the DCOCLK signal, if:
SMCLK is switched off (SCG1 = 1) or DCOCLK is not selected for SMCLK (SELS = 0).

B. MCLK does not need the DCOCLK signal, if:
MCLK is switched off (CPUOff = 1) or DCOCLK is not selected for MCLK (SELM.1 = 1).

C. MCLK and SMCLK does not need the DCOCLK signal, if:
The control bit SCG0 in the status register can switch off (SCG0 1) the DCOGEN.

Figure 12. DCO Shutdown Control Logic

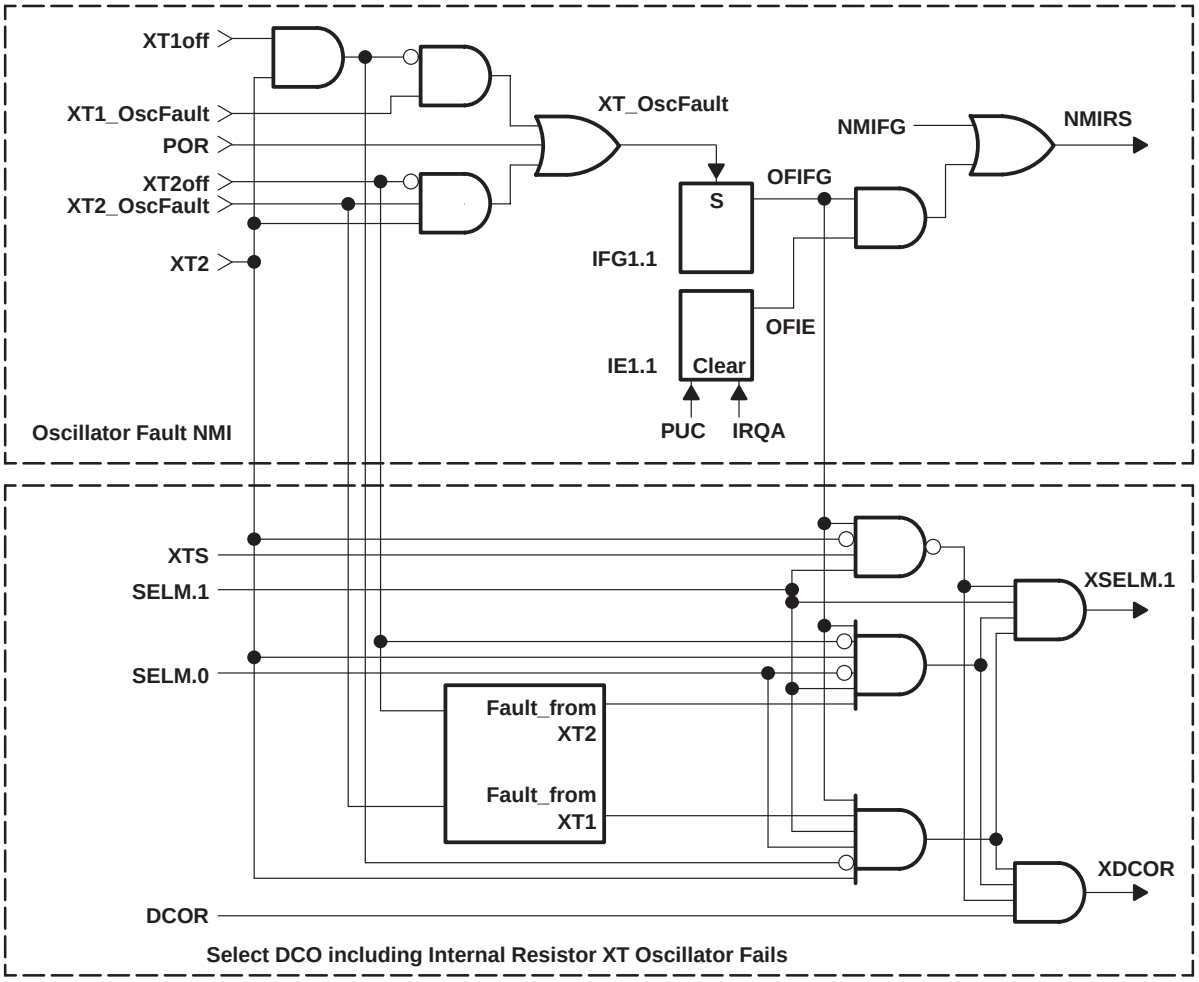
2.4 Oscillator Fault Detection

The XT1 and XT2 oscillators have fault detection circuitry. An oscillator fault condition is flagged when approximately 50 cycles (at 1 MHz) of the oscillator have been missed. When an oscillator fault condition is detected, the oscillator fault interrupt flag, OFIFG in register IFG1 is set. If the oscillator fault interrupt is enabled, i.e., if bit OFIE in register IE1 is set to logic 1, a nonmaskable interrupt is requested.

Note that the XT1 and XT2 oscillators have independent fault detection circuitry, and either can initiate the oscillator fault interrupt. If both of these oscillators are present, then both fault detection circuits must be clear for the interrupt flag to be cleared.

At power up the oscillator fault flag OFIFG is automatically set, but the interrupt is disabled (OFIE is 0). Note that the OFIFG flag is NOT automatically cleared, even after the oscillators have stabilized (after approximately 50 cycles, at 1 MHz). If the application depends on the oscillator fault functionality, then the application must clear the OFIFG flag when appropriate.

Figure 13 shows the internal logic which controls the oscillator fault detection.



XT2 Is an internal signal
XT2 = 0: Two oscillators – XT2 not implemented
XT2 = 1: Three oscillators – XT2 implemented
IRQA: Interrupt request accepted

Figure 13. Oscillator Fault Detection Logic

2.5 Buffered Oscillator Outputs

The majority of MSP430x1xx devices can provide buffered ACLK and/or SMCLK signals on I/O pins. The exact capabilities are device dependent, but the code fragment below shows how to output a buffered ACLK signal on the P2.0 port pin.

```
;
; Code fragment for configuring P2.0 pin as buffered
; ACLK output on MSP430x112.
;
P2DIR .equ 002ah  ; Port2 Direction Register
P2OUT .equ 0029h  ; Port2 Output Register
P2SEL .equ 002eh  ; Port2 Mode Register

mov.b #-1h,&P2DIR ; All Port2 pins outputs
clr.b &P2OUT      ; Clear Port2 output register
bis.b #1,&P2SEL   ; Output ACLK on P2.0
```

3 Other Application Materials

Application Note SLAA074 describes the implementation of a software feedback loop for DCO control.

MSP430 application notes can be found on the Internet at http://www.ti.com/sc/docs/msp/msp430/msp430.htm, and can be ordered from the Texas Instruments European Information Centre (EPIC).

3.1 References to Architecture Guide and Application Report

These references refer to:

AGML - Architecture Guide and Module Library, SLAUE10B, 1996.
AR - Application Report, SLAAE10C, 1998

Reference	Book	Page
Interrupt Processing	AGML	3-8
Interrupt Related Special Function Registers IEx, IFGx	AGML	3-10
Interrupt Vector Addresses	AGML	3-13
Operating Modes	AGML	3-16
Low Power Modes	AGML	3-19
Oscillator and System Clock Generator	AGML	7-1
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Checklist for Problems	AR	7-15

Appendix A Oscillator Characterization Information

The following oscillator characterization information shows representative characteristics under the conditions indicated. It does not necessarily cover all device types and configurations.

During the following oscillator characterization tests, two capacitors of the indicated value are required, one from X_{IN} to V_{SS} and one from X_{OUT} to V_{SS}, as shown in Figure A-1.

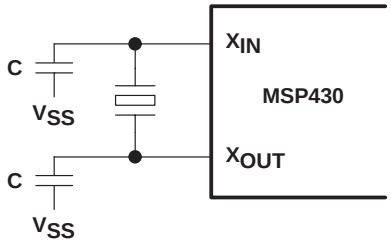

Figure A–1. Oscillator Characterization

A.1 Crystal Data

FREQUENCY (kHz)	TYPE	HOLDER STYLE	C_L (pF)	FREQUENCY TOLERANCE (ppm)	MANUFACTOR OR DISTRIBUTOR	WEB-ADRESS
32.756	Quartz Crystal	TC-26	7.5	±20	Digital Electronic Siegfried Lehrer GmbH	www.digitallehrer.de
455	Ceramic Resonator	SMD	No info.	±5000	Murata	www.murata.com
1000	Quartz Crystal	HC-51/U	32	±30	HY-Q International / CBF-Electronics	www.hy-q.com www.cbf-electronics.de
4000	Quartz Crystal	HC-49/U	30	±30	Digital Electronic Siegfried Lehrer GmbH	www.digitallehrer.de
8000	Quartz Crystal	HC-49/U	20	±30	Digital Electronic Siegfried Lehrer GmbH	www.digitallehrer.de

For a given load capacitance, C_L, a capacitance of 2 x C_L is required on each pin of the crystal/resonator.

e. g. C_L=30 pF therefore $C_{(XIN)} = C_{(XOUT)}$ = 60 pF

Note for 1 MHz: ESR (equivalent serial resistance) should be lower then 500 Ω.

A.2 MSP430P112 Characterization (MSP430C112 follows below)

A.2.1 MSP430P112 Oscillator Start-Up

Table A-1 below shows the oscillator start-up time for a range of frequencies and supply voltages.

NOTES:

1. No additional external capacitance is required when using a 32-kHz crystal.
2. The XT5V bit in register BCSCTL1 must be 0 for best results.
3. Temperature during test was 25°C.
4. All components were soldered, and leads were kept to a minimum length.

Table A–1. XT1/XT2 Oscillator Start-Up Time

OSCILLATOR FREQUENCY	OSCILLATOR TYPE	V_{CC} (V)	START-UP TIME (ms)
32 kHz C = none	Quartz crystal	3	201
		5	96.4
455 kHz C = 82 pF	Ceramic resonator	3	1.77
		5	—
1 MHz C = 47 pF	Quartz crystal	3	5.82
		5	3.81
4 MHz C = 56 pF	Quartz crystal	3	4.54
		5	3.07
8 MHz C = 39 pF	Quartz crystal	3	1.97
		5	1.27

A.2.2 MSP430P112 Temperature Characteristics

Table A-2 shows 32-kHz oscillator characteristics for a range of temperatures and operating voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. No additional external capacitance is required on the X_{IN} and X_{OUT} pins as a 32-kHz crystal is being used.
2. The XT5V bit in register BCSCTL1 must be 0 for best results.
3. All components were soldered, and leads were kept to a minimum length.
4. The 32-kHz crystal was kept at room temperature to remove its temperature characteristics from the measurements. The figures stated below are then representative of the MSP430 internal oscillator.

Table A–2. XT1/XT2 32-kHz Quartz Crystal Oscillator Temperature Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	32770.1	318	1.5	0.9
	3.0	32770.3	420		1.6
	5.0	32770.7	870		6.2
	5.5	32770.8	1005		10.3
25	2.5	32770.2	261	1.5	0.8
	3.0	32770.3	340		1.4
	5.0	32770.5	693		5.0
	5.5	32770.5	797		6.2
85	2.5	32770.2	208	1.6	0.8
	3.0	32770.3	268		1.3
	5.0	32770.4	543		4.6
	5.5	32770.4	624		5.9

A.2.3 MSP430P112 455-kHz Ceramic Resonator Characteristics

Table A-3 shows 455-kHz ceramic resonator characteristics for a range of temperatures and operating voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. The XT5V bit in register BCSCTL1 must be 0 for best results.
2. Two external 82-pF capacitors were connected between X_{IN} and V_{SS}, and X_{OUT} and V_{SS}.
3. All components were soldered, and leads were kept to a minimum length.

Table A–3. XT1/XT2 455-kHz Ceramic Resonator Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	455535	326	1.7	29.5
	3.0	455572	473		48.9
	5.0	455733	1013		202.6
	5.5	455750	1258		389.7
25	2.5	454957	294	1.8	25.2
	3.0	454984	390		39.8
	5.0	455115	865		152.3
	5.5	455101	1027		209.6
85	2.5	454926	257	2.0	33.1
	3.0	454959	339		51.4
	5.0	455096	756		176.0
	5.5	455123	891		227.7

A.2.4 MSP430P112 1-MHz Crystal Oscillator Characteristics

Table A-4 shows 1-MHz crystal oscillator characteristics for a range of temperatures and operating voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. The XT5V bit in register BCSCTL1 must be 0 for best results.
2. Two external 47-pF capacitors were connected between X_{IN} and V_{SS}, and X_{OUT} and V_{SS}.
3. The effective series resistance (ESR) for the 1MHz quartz crystal should be less than 500 Ω.
4. All components were soldered, and leads were kept to a minimum length.

Table A–4. XT1/XT2 1-MHz Crystal Oscillator Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	1000059	384	1.7	29.4
	3.0	1000060	513		46.3
	5.0	1000064	1125		173.4
	5.5	1000065	1312		224.9
25	2.5	1000043	308	1.6	28.3
	3.0	1000044	407		43.3
	5.0	1000047	885		144.9
	5.5	1000048	1031		180.8
85	2.5	1000014	266	2.0	26.7
	3.0	1000015	348		40.4
	5.0	1000018	747		130.3
	5.5	1000018	868		161.6

A.2.5 MSP430P112 4-MHz Crystal Oscillator Characteristics

Table A-5 shows 4-MHz crystal oscillator characteristics for a range of temperatures and operating voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. The XT5V bit in register BCSCTL1 must be 0 for best results.
2. Two external 56-pF capacitors were connected between X_{IN} and V_{SS}, and X_{OUT} and V_{SS}.
3. All components were soldered, and leads were kept to a minimum length.

Table A–5. XT1/XT2 4-kHz Crystal Oscillator Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	3999936	497	2.2	67.3
	3.0	3999936	656		93.9
	5.0	3999939	1400		254.9
	5.5	3999940	1623		312.9
25	2.5	3999992	410	2.1	66.1
	3.0	3999993	539		90.8
	5.0	399996	1148		230.4
	5.5	3999997	1328		274.8
85	2.5	4000002	392	2.3	64.7
	3.0	4000004	510		88.3
	5.0	4000008	1061		216.6
	5.5	4000010	1221		256.6

A.2.6 MSP430P112 8-MHz Crystal Oscillator Characteristics

Table A-6 shows 8-MHz crystal oscillator characteristics for a range of temperatures and supply voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. The XT5V bit in register BCSCTL1 must be 0 for best results.
2. Two external 39-pF capacitors were connected between X_{IN} and V_{SS}, and X_{OUT} and V_{SS}.
3. All components were soldered, and leads were kept to a minimum length.

Table A–6. XT1/XT2 8-kHz Crystal Oscillator Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	—	574	2.7	104.9
	3.0	7999644	839		140.0
	5.0	7999654	1758		331.3
	5.5	7999656	2027		394.2
25	2.5	—	461	2.9	104.6
	3.0	7999793	682		139.3
	5.0	7999804	1446		316.7
	5.5	7999807	1666		370.6
85	2.5	—	385	3.3	104.3
	3.0	—	592		138.7
	5.0	7999922	1442		308.6
	5.5	7999928	1651		358.7

A.3 MSP430C112 Characterization (MSP430P112 above)

A.3.1 MSP430C112 Oscillator Start-Up Time

Table A–7 shows the oscillator start-up time for a range of frequencies and supply voltages.

NOTES:

1. No additional external capacitance is required when using a 32 kHz crystal.
2. The XT5V bit in register BCSCTL1 must be 0 for best results.
3. Temperature during test was 25°C.
4. All components were soldered, and leads were kept to a minimum length.

Table A–7. XT1/XT2 Oscillator Start-Up Time

OSCILLATOR FREQUENCY	OSCILLATOR TYPE	V_{CC} (V)	START-UP TIME (ms)
32 kHz C = none	Quartz crystal	3	281
		5	130.0
455 kHz C = 82 pF	Ceramic resonator	3	1.57
		5	1.12
1 MHz C = 47 pF	Quartz crystal	3	40.0
		5	19.8
4 MHz C = 56 pF	Quartz crystal	3	59.4
		5	26.8
8 MHz C = 39 pF	Quartz crystal	3	32.9
		5	12.88

A.3.2 MSP430C112 32-kHz Temperature Characteristics

Table A-8 shows 32-kHz oscillator characteristics for a range of temperatures and operating voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. No additional external capacitance is required on the X_{IN} and X_{OUT} pins as a 32-kHz crystal is being used.
2. The XT5V bit in register BCSCTL1 must be 0 for best results.
3. All components were soldered, and leads were kept to a minimum length.
4. The 32-kHz crystal was kept at room temperature to remove its temperature characteristics from the measurements. The figures stated below are then representative of the MSP430 internal oscillator.

Table A–8. XT1/XT2 32-kHz Temperature Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	32769.4	301	1.5	0.9
	3.0	32769.4	403		1.6
	5.0	32769.7	750		5.9
	5.5	32769.8	824		7.5
25	2.5	32769.4	212	1.7	0.8
	3.0	32769.4	276		1.4
	5.0	32769.6	535		4.9
	5.5	32769.7	606		6.2
85	2.5	32769.4	178	1.7	0.7
	3.0	32769.4	229		1.3
	5.0	32769.5	440		4.6
	5.5	32769.6	497		

A.3.3 MSP430C112 455-kHz Ceramic Resonator Characteristics

Table A-9 shows 455-kHz ceramic resonator characteristics for a range of temperatures and operating voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. The XT5V bit in register BCSCTL1 must be 0 for best results.
2. Two external 82-pF capacitors were connected between X_{IN} and V_{SS}, and X_{OUT} and V_{SS}.
3. All components were soldered, and leads were kept to a minimum length.

Table A–9. XT1/XT2 455-kHz Ceramic Resonator Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	455025	298	1.7	23.4
	3.0	455079	401		40.3
	5.0	455276	865		187.8
	5.5	455331	1016		219.3
25	2.5	454954	246	1.8	24.2
	3.0	454982	325		38.2
	5.0	455147	694		143.3
	5.5	455173	812		183.8
85	2.5	454928	216	2.0	31.1
	3.0	454960	284		48.4
	5.0	455091	609		162.3
	5.5	455122	710		206.4

A.3.4 MSP430C112 1-MHz Crystal Oscillator Characteristics

Table A-10 shows 1-MHz crystal oscillator characteristics for a range of temperatures and supply voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. The XT5V bit in register BCSCTL1 must be 0 for best results.
2. Two external 47-pF capacitors were connected between X_{IN} and V_{SS}, and X_{OUT} and V_{SS}.
3. All components were soldered, and leads were kept to a minimum length.

Table A–10. XT1/XT2 1-MHz Crystal Oscillator Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	1000060	332	1.7	28.9
	3.0	1000061	443		45.2
	5.0	1000066	924		162.4
	5.5	1000067	1101		242.5
25	2.5	1000044	261	1.8	27.1
	3.0	1000045	344		41.3
	5.0	1000050	718		136.7
	5.5	1000051	826		169.8
85	2.5	1000016	232	2.0	25.8
	3.0	1000016	302		38.8
	5.0	1000019	618		122.3
	5.5	1000020	710		150.8

A.3.5 MSP430C112 4-MHz Crystal Oscillator Characteristics

Table A-11 shows 4-MHz crystal oscillator characteristics for a range of temperatures and operating voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. The XT5V bit in register BCSCTL1 must be 0 for best results.
2. Two external 56-pF capacitors were connected between X_{IN} and V_{SS}, and X_{OUT} and V_{SS}.
3. All components were soldered, and leads were kept to a minimum length.

Table A–11. XT1/XT2 4-MHz Crystal Oscillator Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	3999951	427	2.2	64.1
	3.0	3999952	563		90.8
	5.0	3999954	11.49		247.9
	5.5	3999955	1317		292.6
25	2.5	3999997	356	2.2	63.2
	3.0	3999999	456		86.7
	5.0	4000003	952		217.8
	5.5	4000004	1092		259.3
85	2.5	4000002	345	2.1	61.2
	3.0	4000004	445		83.4
	5.0	4000009	892		203.1
	5.5	4000010	1021		240.3

A.3.6 MSP430C112 8-MHz Crystal Oscillator Characteristics

Table A-12 shows 8-MHz crystal oscillator characteristics for a range of temperatures and supply voltages. f_{ACLK} is the actual A_{CLK} frequency seen. I_{CC} is the current consumption in active mode, with an MCLK of 1 MHz. $V_{CC(ACLK)low}$ is derived by reducing V_{CC} until the oscillator stops, and then raising V_{CC} again until the oscillator restarts. $V_{CC(ACLK)low}$ is the point at which correct oscillation starts again. I_{OSC} is the current consumption of only the oscillator.

NOTES:

1. The XT5V bit in register BCSCTL1 must be 0 for best results.
2. Two external 39-pF capacitors were connected between X_{IN} and V_{SS}, and X_{OUT} and V_{SS}.
3. All components were soldered, and leads were kept to a minimum length.

Table A–12. XT1/XT2 8-MHz Crystal Oscillator Characteristics

TEMPERATURE (°C)	V_{CC} (V)	f_{ACLK} (Hz)	I_{CC} (μA)	$V_{CC(ACLK)low}$ (V)	I_{OSC} (μA)
-40	2.5	7999692	564	2.5	100.6
	3.0	7999698	741		134.3
	5.0	7999707	1483		313.5
	5.5	79997.9	1690		377.1
25	2.5	7999812	458	2.5	99.9
	3.0	7999817	605		133.0
	5.0	7999833	1222		300.8
	5.5	7999835	1398		351.3
85	2.5	—	390	2.6	98.9
	3.0	7999914	613		131.9
	5.0	7999932	1252		291.4
	5.5	7999936	1424		339.0

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