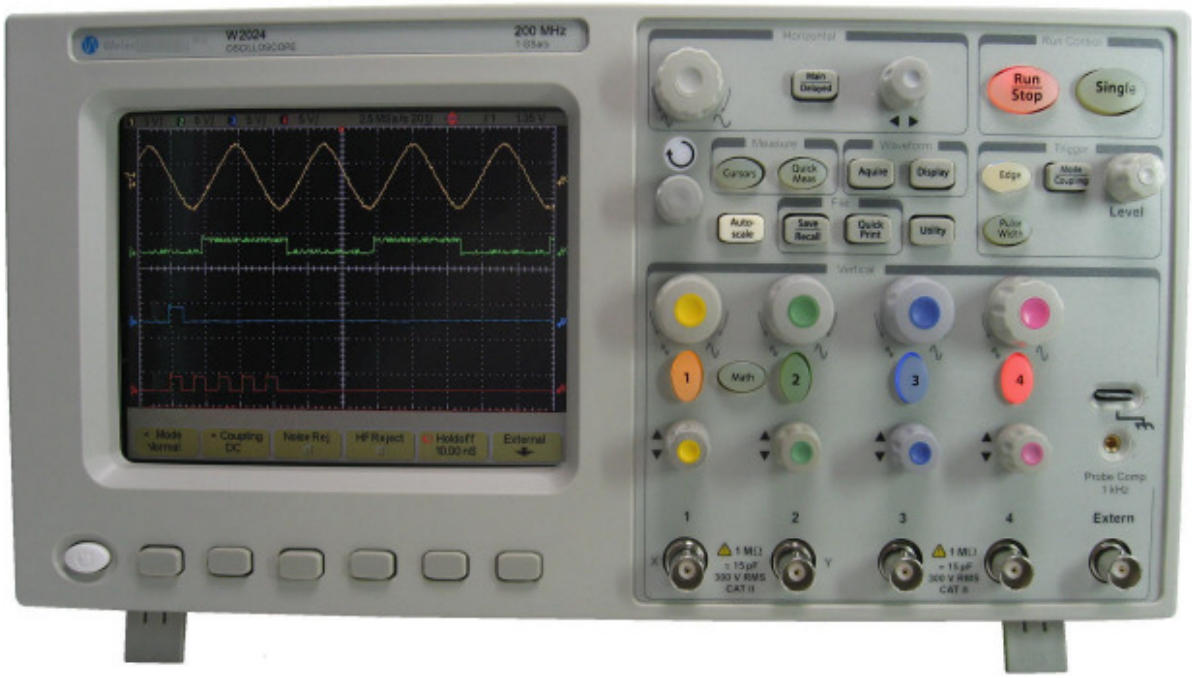
W2000A Low Budget Mod



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Preface

The W200A Series mainly suffers from two problems:

- Strong noise, especially in the 1 and 2 per div. voltage ranges
- Strongly non linear amplitude response. From 50MHz to 200MHz amplitude readings are way too high, causing distorted signal display.

The strong noise is mainly caused by a poor amplification of the input signal, so less than the 256 levels of the 8bit ADC can be used. As a result, the signal has to be scaled up to be displayed. The unavoidable noise of the ADCs and input circuit becomes more significant. Or in technical terms: The Signal to Noise Ratio (SNR) is very poor for these resolutions.

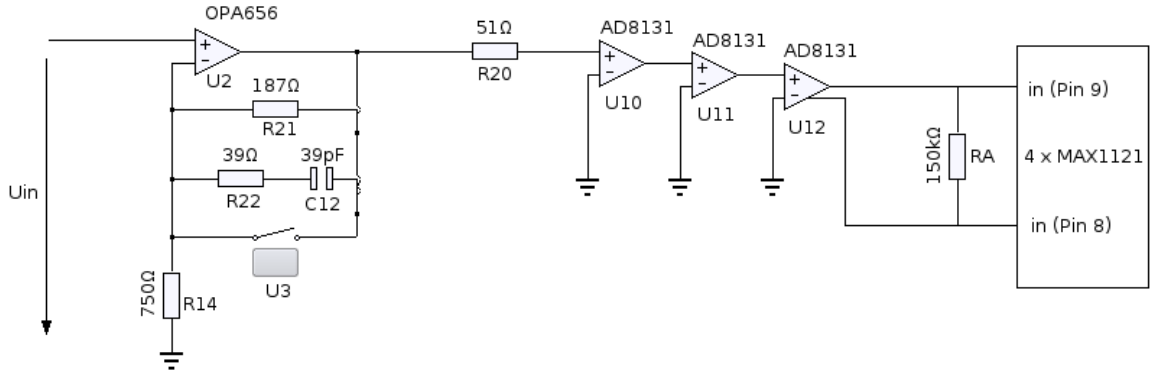

Fig 1: Analog input stage in original condition

Fig 1 shows a simplified schematic of the analog input stage. Basically consisting of an OPA656 and three AD8131 op-amps in series. The Part numbers refer to the circuit diagram Analog-Input-Part_assignment_V3_4.pdf. The file is located in the W2000A Wiki on SFN:

http://sourceforge.net/apps/trac/welecw2000a/wiki/WikiStart

follow the link „Hardware overview“.

The OPA656 just acts as an impedance converter, the gain is hardly higher than 1. The feedback circuit of R_{21} and R_{14} results in a gain of approx. 1.25. For frequencies above 5 to 7MHz, the parallel high pass filter consisting R_{22} and C_{12} reduces the gain down to 1. The result is an additional non-linearity in the range of 5 to 15 MHz.

It is unclear what WELEC tried to achieve with this design. We will come back to that later, because we can make use of it.

There is an additional switch (U3) that is permanently set to 1 by the original WELEC firmware in some voltage ranges. In the open source firmware the switch is always open to get as much gain as possible.

The three AD8131 work as:
a) voltage dividers for the individual voltage ranges by switching the amplification between 1 and 2

b) differential drivers for the ADC input

The distorted frequency response of the DSO is caused by the characteristic curve of the OPA656, the first stage of the input amplifier.

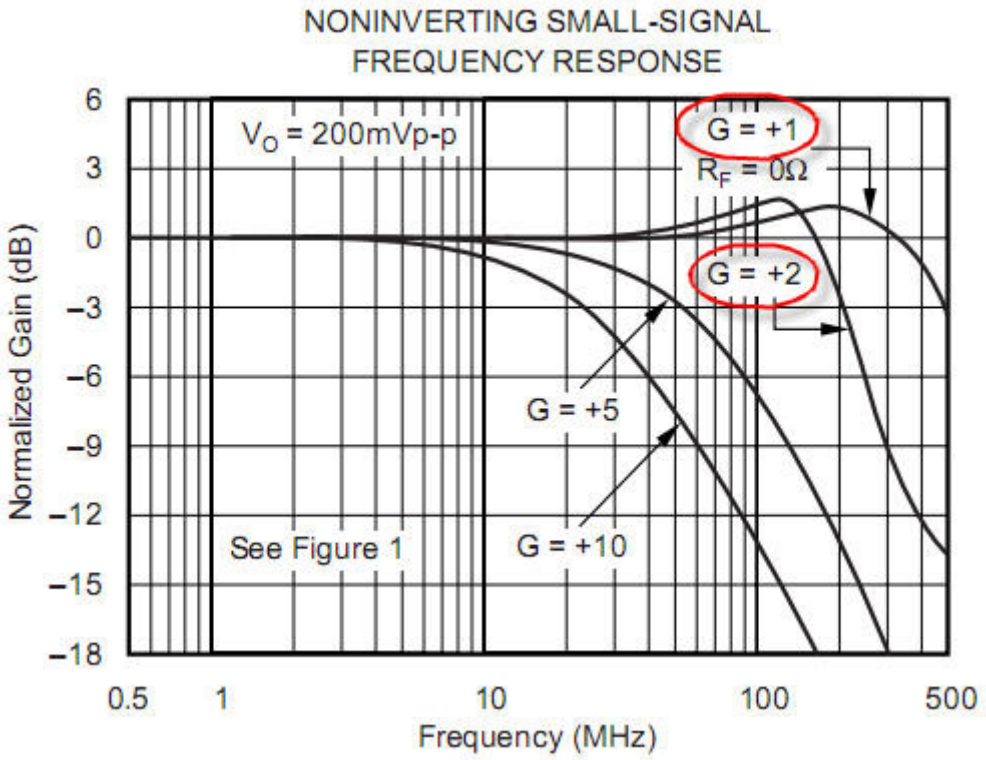

Fig 2: Frequency response OPA656

The response curve of the gain range between 1 and 2 quite exactly represents the amplitude response of our W2000A. One clearly can see the amplitude rising towards 2dB between 100MHz and 200MHz. This is a factor of approx. 1.25 or a deviation of 25%.

The AD8131 on the other hand, have a very linear response up to 200MHz, falling to -3dB at about 400MHz (Fig 3). Our operating levels are lower than 2Vpp, but other than circuit used for measuring here, the WELEC doesn't use a 200 ohms load resistor. The resulting load resistance is about 1.1kOhms, which leads to the same result.

The distorted frequency response of the OPA656 is thus passed on to the ADC.

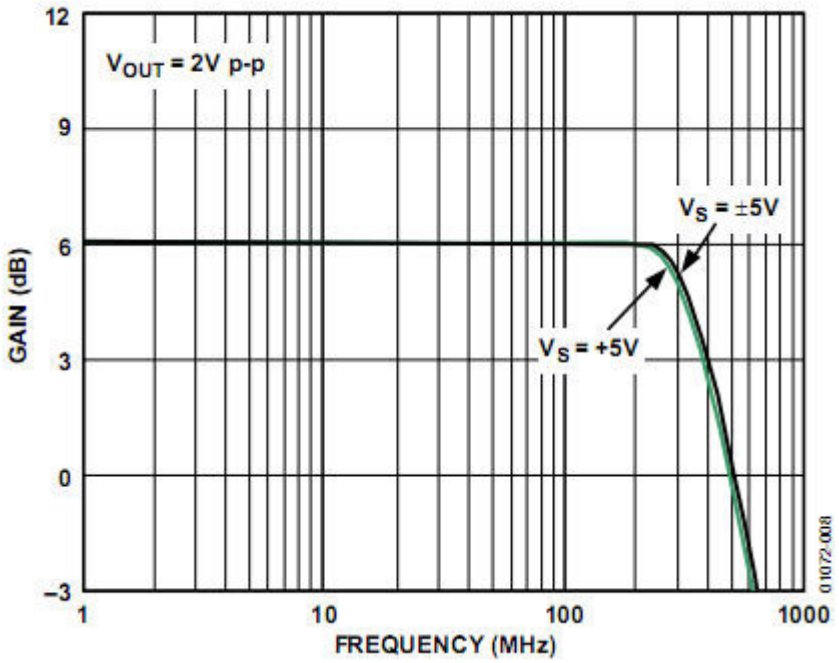

Fig 3: Frequency response AD8131 with load > 200Ω

There were some attempts to rectify the distorted frequency response. One attempt is to use a different terminating resistor (174Ohm) at the output of the last AD8131. More than that, 24.9 Ohms series resistors have been used to replace the 0Ohm Resistors. The goal was to reach a resulting resistance of 200 Ohms, as used in the test circuits of the manufacturer's data sheet. The serial resistors are recommended by the manufacturers for capacitive loads to reduce the tendency of the AD8131 to oscillate. The 4 ADCs cause a combined capacitive load of about. 15pF, which makes it plausible to use series resistors.

A 200Ohms termination causes a reduction of the AD8131s response exactly in the range where the response of the OPA656 rises. (Fig 4) We correct the distorted frequency response by also bending the otherwise linear frequency response of the AD8131 - the result is less that ideal.

These measures come with some more disadvantages: The two 24.9 Ohms resistors and the 174Ohms (180 Ohms) resistor in parallel with the ADC inputs form a 1:3 voltage divider. In other words: less of the ADC's resolution can be used, the signal has to be scaled up and the SNR becomes worse, which results in a noisy Figure on the screen.

Then, causing a higher load on the AD8131's output in the upper operating range, the 200 Ohms termination causes a non-linearity, so this range is not fully usable. This is essential to our next considerations about raising the signal levels, because that is exactly the range we will want to use.

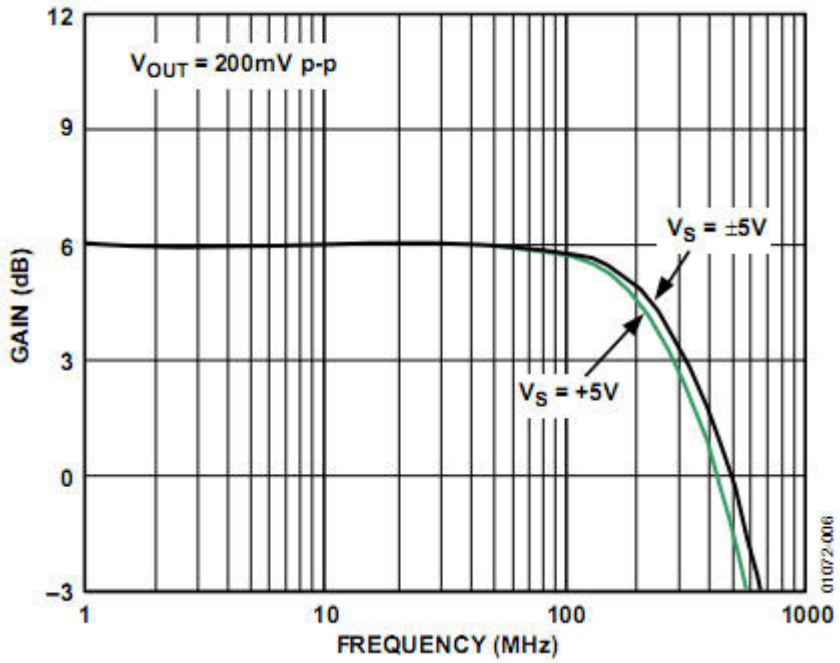

Fig 4: Frequency response AD8131 with 200Ω load

The Idea

To get a usable representation of the signal on the screen, we have to do two things:

1. Increase the gain to better use the ADC's resolution in order to get a better SNR. The components should be chosen for low noise.
2. The frequency response has to be adjusted so it remains as linear as possible from 1MHz - 150MHz to get a valid display of the signal and it’s amplitude.

That should be achieved with a few, easy to accomplish modifications.

To increase the gain, there are several options. As a first step, we could change the terminating voltage divider to get a higher signal voltage at the ADC's input. Tests have shown that values of 300 Ohms by 2x24.9Ohms are suitable. Both series resistors dampen the op-amp’s tendency to oscillate.

The four ADC inputs (4.4kOhm each) are in parallel with the 330Ohms which amounts to about 250Ohms. With the series resistors, this adds up to 300Ohms as the AD8131's load. The voltage is divided 1:5, i.e. with 1V at the op-amp’s output, we have 0.166V drop at the series resistors and 0.833V at the ADC input. That is a significantly better ratio than with the 200Ohms terminator. In addition to that, the usable dynamic range of the AD8131 is wide enough to supply the e1.25V p-p FS of the ADC inputs without too much distortion.

An other option to increase the gain are the three AD8131. Their internal feedback fixes their gain to 2. Changing the gain with external components is quite complex, because these op-amps are also used to switch voltage ranges. So there would be unwanted side effects. So the AD8131 are not suitable for a simple modification.

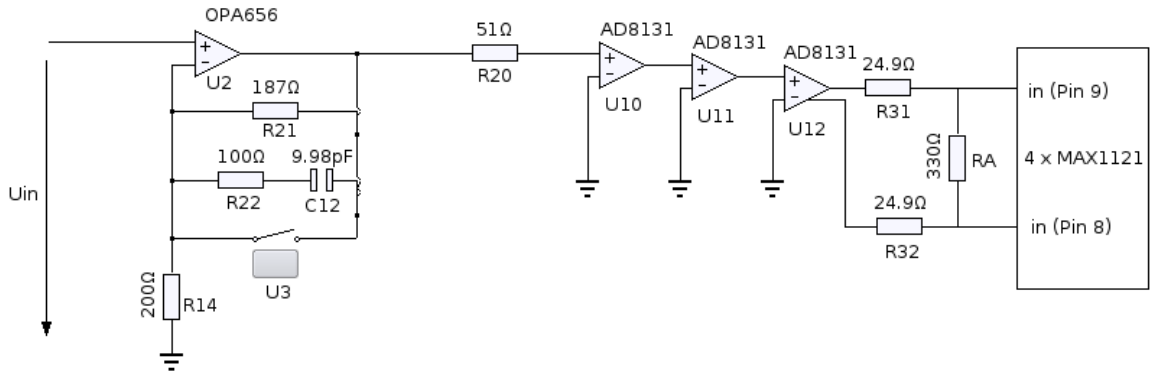

Fig 5: Newly designed input stage

This leaves the first input stage, the OPA656. Our usable gain is between 1 and 2. To use the ADC's full range, an amplification of 1.9 should be achieved. Higher values would not fit the height of the screen, lower values would not yield the best possible SNR.

To increase the gain, the voltage divider consisting of the feedback resistor R_{21} and R_{14} have to be recalculated. The gain is:

$V = 1 + (R_{21} / R_{14})$

One option is to increase R_{21} to about. 680Ohms. This reduces the current passing the voltage divider, but is not ideal for the noise level. The manufacturer recommends a parallel resistance of $R_{21} \| R_{14}$ to be less than 200 Ohms. So I left R_{21} unchanged and changed R_{14} to 200Ohms. The resulting gain is 1.915 with low input noise ($R_{21} \| R_{14} < 100$Ohms).

Having the gain set properly, the other issue is to rectify the frequency response. To achieve this, we can use the nonsensical high pass filter of the feedback circuit.

The goal is to reduce the amplifier gain at the point when the amplitude response rises and to reduce the gain exactly that far, that the resulting response is linear. Simply put: R_{22} influences how much the gain is reduced, C_{12} influences when the bandwidth limit cuts in. Of course the reactance of the capacitor also plays a role, but this simplified view is a good start.

As the amplitude is, as stated in the preface, by 25% too high, the gain has to be reduced by about 25% at 150MHz.

At a start value of 1.9 for the gain, a reduction by 25% results in a remaining gain of 1.4.

This is calculated from:

$V = 1 + (R_{21} || Z_F) / R_{14}$

$R_{21} || Z_F = (R_{21} * |Z_F|) / (R_{21} + |Z_F|)$ with $|Z_F| = \sqrt{(X^2_{C12} + R^2_{22})}$

and $X_{C12} = 1 / (2 * \pi * f * C_{12})$ at f = 150MHz

Inserting various combinations of R and C in the formula finally resulted in C_{12} = 10pF and R_{22} = 100Ohms.

This makes sure that the high pass filter kicks in slowly from approx. 25MHz and reduces the gain noticeably from 50MHz up.

At this point some fine tuning with other resistors or capacity values is possible. A slightly different value of C_{12} might reduce the small dent between 20MHz and 80MHz. I do not have suitably spaces component values, so I left it at 10pF. The result is quite appealing to me.

Implementation

Main PCB removal

First the main PCB has to be removed. To achieve this, the knobs of the front panel have to be removed. Otherwise we won't get to the BNC mounts. The knobs sit very tightly, but can be pried off with a small screwdriver. Set the screwdriver against the rim where the flattened part of the shaft begins.

Remove the back cover (three bolts). The power supply is on one side, the main board on the other. First we have to remove the power supply (4 bolts). Pull the board carefully off the headers. Then remove the two little plugs connecting the PSU to the display.
Next, remove the display connector and the bolts holding the main PCB. Now, remove the complete metal frame from the plastic front panel and remove the screws of the BNCs. The main PCB can now carefully be pried free. This works best at the place were the little screw was. The PCB then pops off the connector below (Fig 6 - Connector 1) and can easily be removed.

For the following steps it is good to have the PCB lying flat and stable. I have cut two support blocks from packaging foam with a carpet knife.

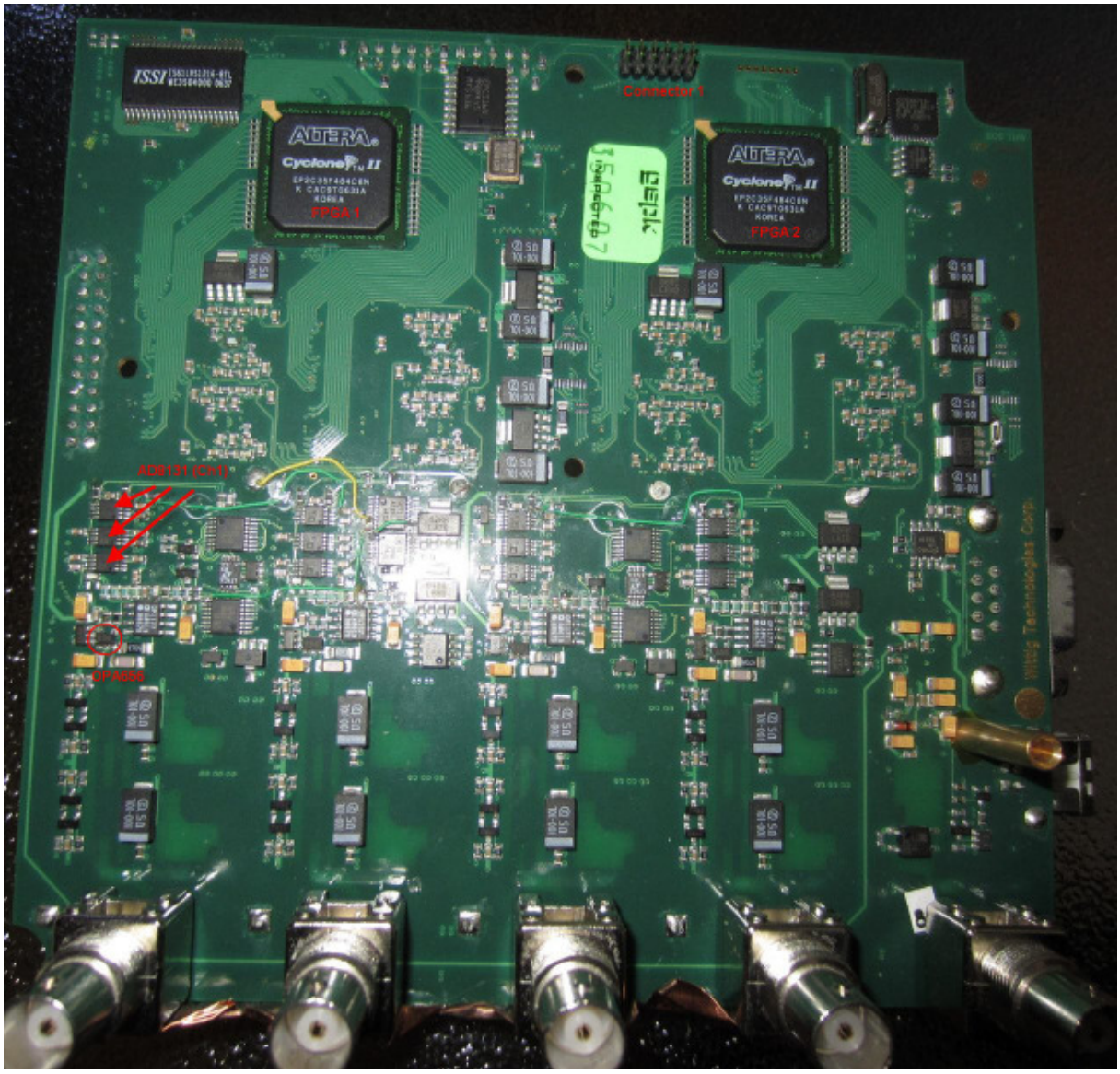

Fig 6: Main PCB

Remove Shieldings

Next you need the soldering iron. The tin shields over the input stages have to be removed. Each shield is soldered diagonally to the PCB at two points. In addition to that, there is a little wire to ground the BNCs (Fig 7). This can be done with a somewhat bigger soldering iron. At one solder joint some extra care is needed because an insulated wire runs through the hole.

Among other things, the OPA656's feedback circuit is under the shield. That is what we want to modify.

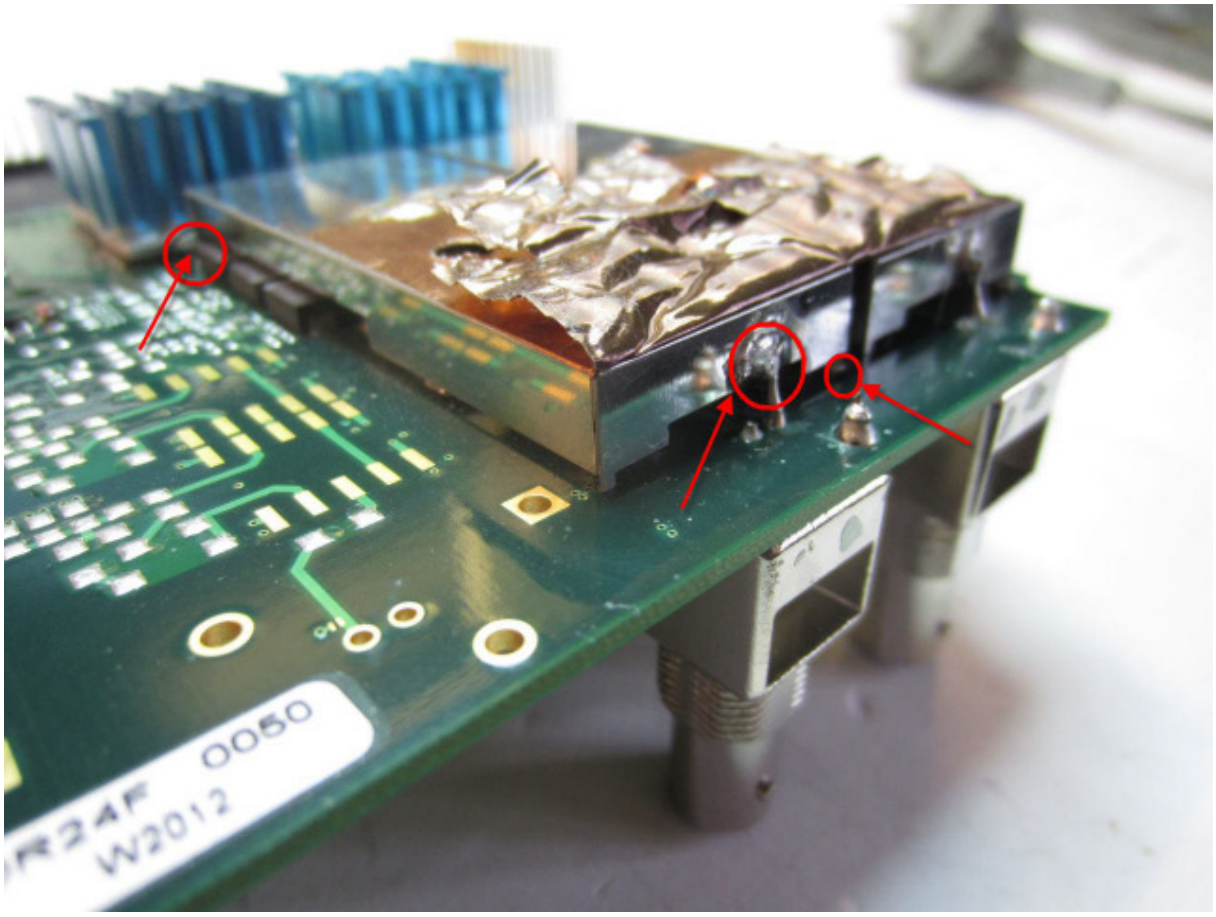

Fig 7 Shielding

Assembly of the feedback circuit

Remove resistor R_{22} (labelled 390) and the C_{12} capacitor (Fig 8 shows original components) and replace with the new values of R_{22} = 100 Ohms (labelled 101 or 01A) and C_{12} = 10pF. R_{21} remains unchanged.

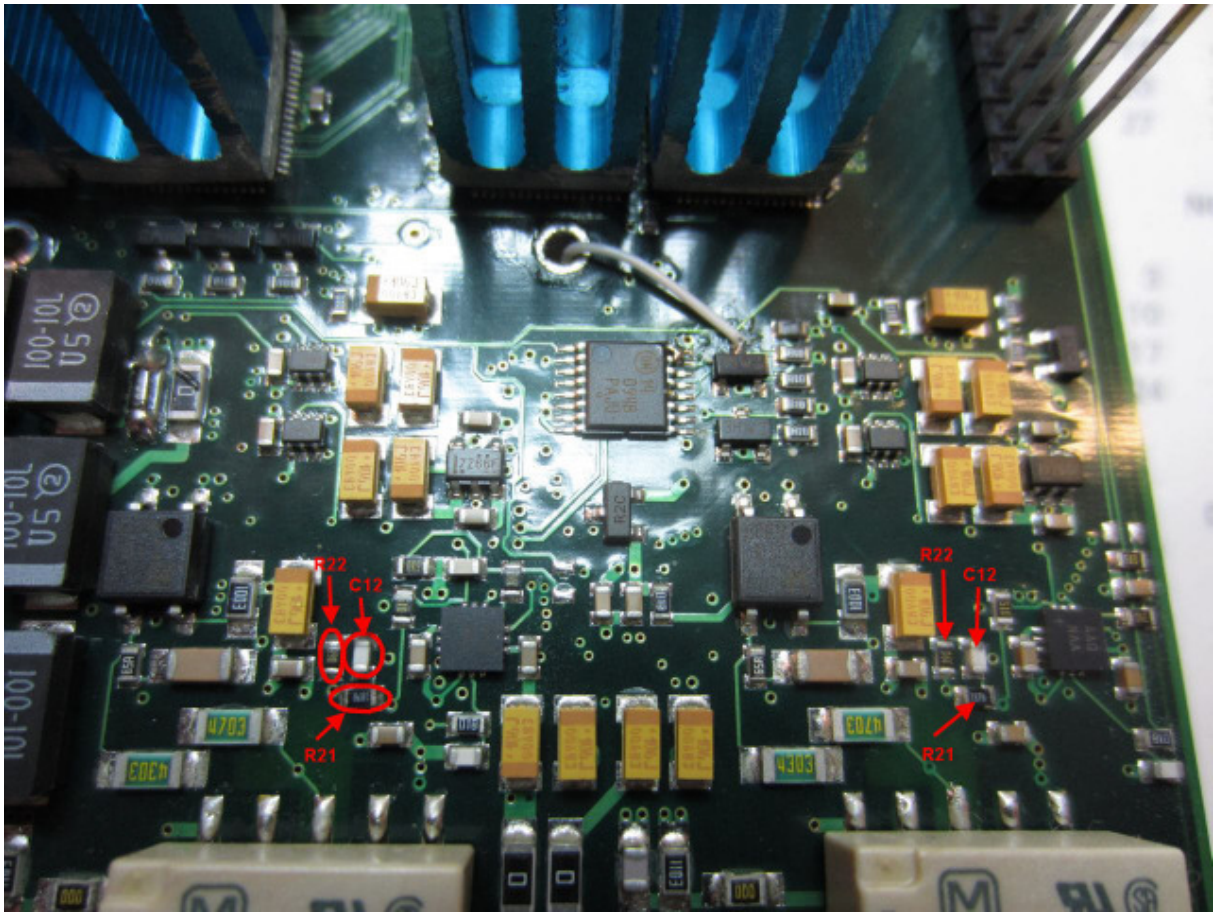

Fig 8: Feedback circuit R_{21} / R_{22} / C_{12}

When working on that side of the PCB, please check the soldering of the variable capacitors. In my scope, all of them weren't soldered properly on one side.

That is it for that side of the board. We'll continue on the other side.

R14 and the series resistors

On the other side of the board, first locate the OPA656. Our R14 is located between the OPA656 and the first AD8131 (Fig 9). Shown here with a 270Ohms resistor for testing. The original value is R14 = 750Ohms (marked: 751). Remove R15 and replace with 200Ohms (Marked 201 or 30A).

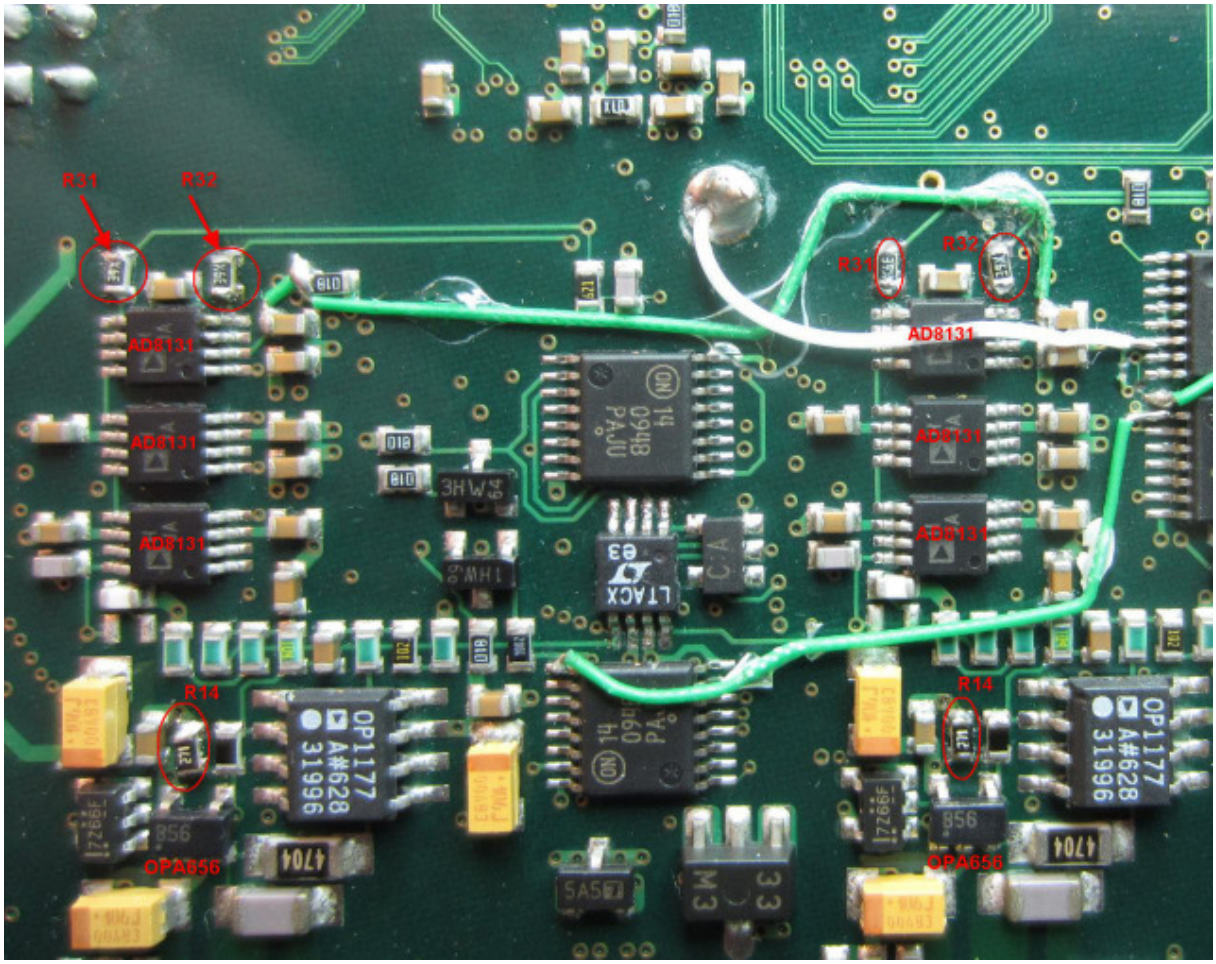

Fig 9: R14 and the series resistors

The next step is to replace the series resistors R31 and R32. We'll find them near the last AD8131. Originally 0Ohms have been used. We'll replace them with 24.9Ohms (Marked: 39X) as seen in Fig 9.

The terminating resistor

Now only the terminating resistor is missing from the ADC input. We find it somewhat above the series resistors towards the FPGA. The original value is 150KOhms (marked 154). In the meantime some have replaced them with 150Ohms, 174 Ohms or 180 Ohms.

In Fig 10, it is the bright blue resistors without markings. This is from a test with 180 Ohms.

We remove the old resistor and replace it with 330Ohms (marked: 331 or 51A).

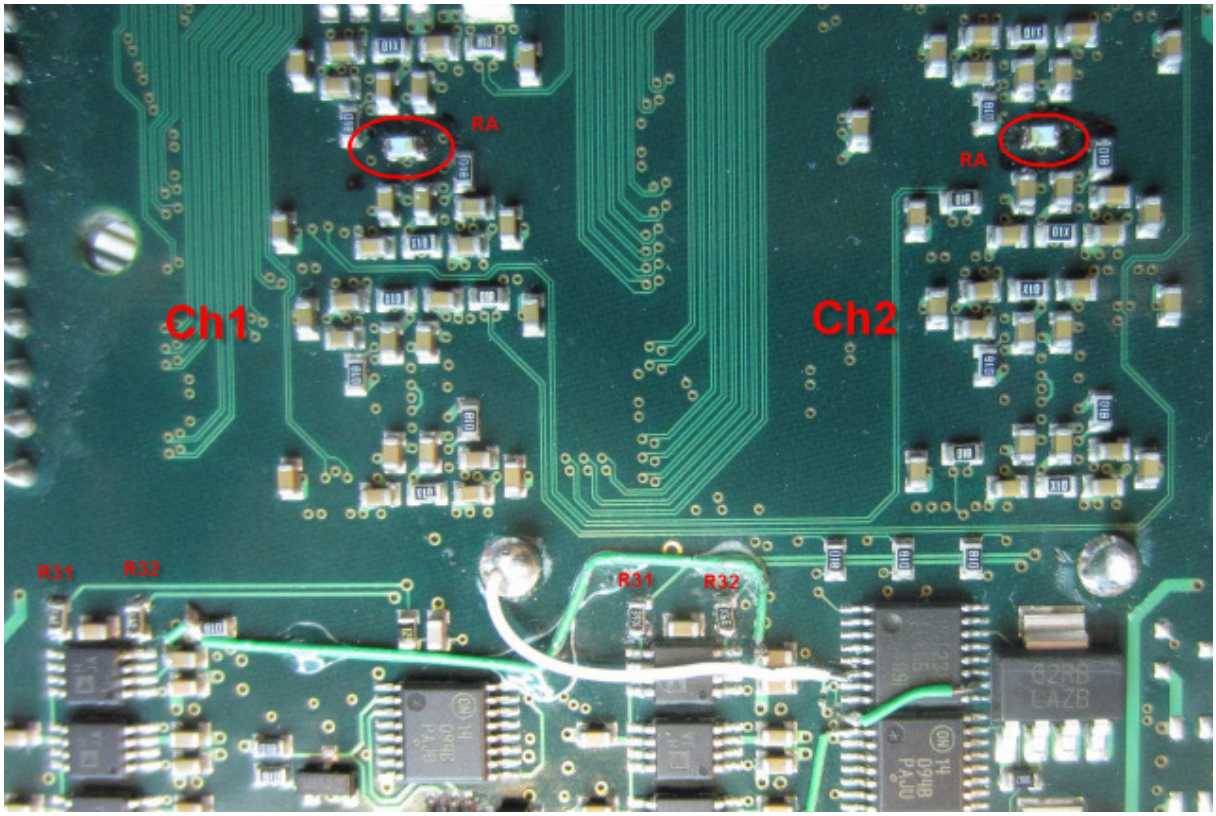

Fig 10: Terminator

Final steps

After reassembly it is advisable to check the signal display. The whole effort to improve the signal representation is futile if the first amplifier stage causes distortions. To do this we need a square wave signal between 1kHz and 1MHz. The edges should have a rise time of less than 40 ns. The signal source must be connected through a link terminated at 50Ω. The probes are unsuitable because they influence the signal.

Adjust the pre-trigger to the left for the second grid division, so you can see the edge and enough of the positive part of the signal.

If you switch through the time bases, you can see the upper corner of the rising edge forming. It should neither be rounded, nor have too much of an overshooting spike. Ideally this should be a perfect angle. In reality, there will always be some overshoot (see Fig. 13-15).

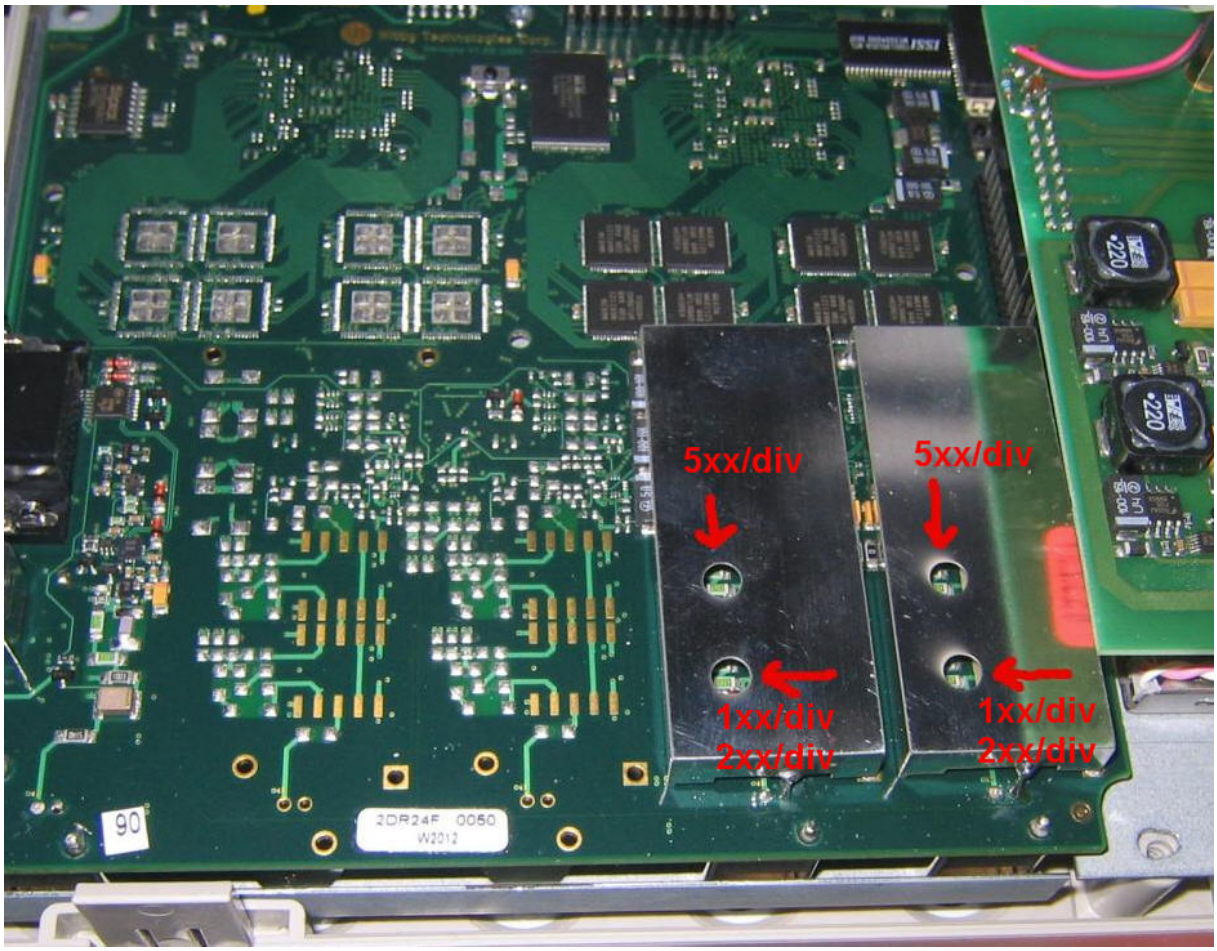

Fig 11: Input adjustment

The Result

Measuring proves the modification's effects. The frequency response of the modified W2022A is almost a bit better than that of the current Owon SDS8102 I used for comparison. While the W200A is rated 200MHz, the SDS8102 is officially sold as a 100MHz instrument. I find this more realistic.

The characteristic curve can be shifted up and down around the zero line with the gain adjustment found in the hardware menu. Depending if you prefer to have less deviation at low frequencies, or a lower average overall deviation over the whole range.

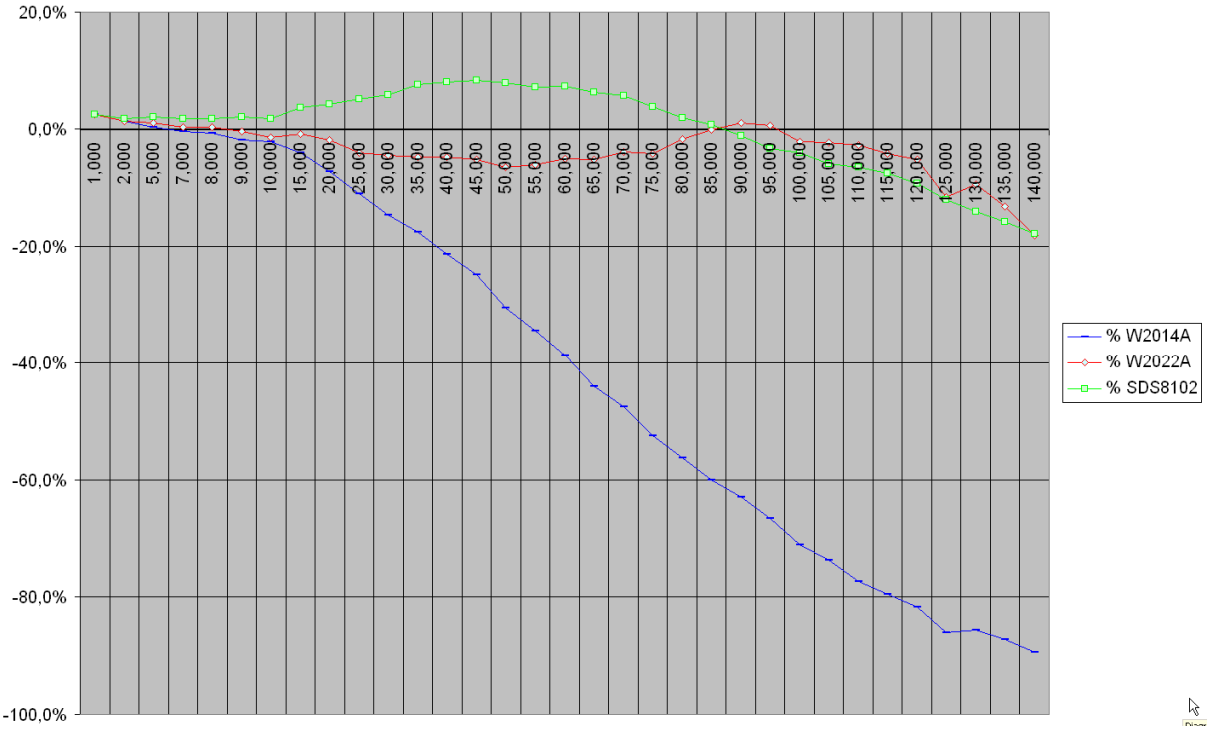

Fig. 12: Frequency response

I took the measurements with a Leader 3216 sine wave generator. It's operational range of 1MHz to 140MHz covers the most relevant frequency range. As a reference I sampled all signal levels with a Tektronix 2465A.

It is apparent that the W2014A's bandwidth is significantly lower than the W2022A's. Welec has built in some sort of brake that still has to be found. That is still work in progress and the conversion from 100MHz to 200MHz will be the topic of another modification.

Noise has gone down considerably and is up to par with the current devices of the same price range. For comparison, here is an identical signal on a W2014A (with the standard modification 2x24.9Ω / 180Ω) in Fig. 13. Then on a W2022A with our low budget mod (Fig. 14) and on a Chinese SDS8102 (Fig. 15).

Noise is still higher in the 1- and 2- ranges, that in the 5-range because the steps chosen by Welec doesn't allow as good scaling as in the 5-range. Compared to the original components the overall picture has improved a lot.

This LB-mod is supported from Firmware BF.6.6.

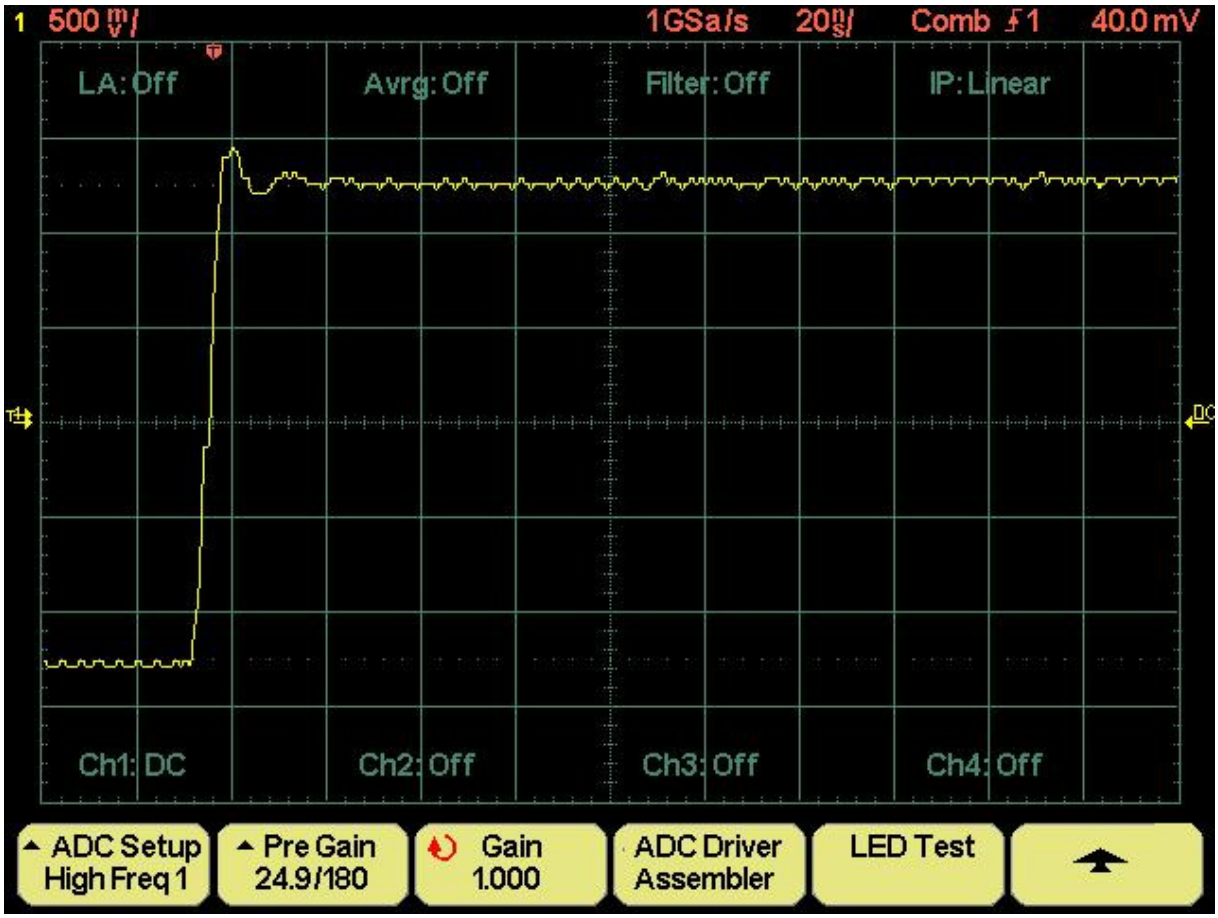

Fig. 13: Noise with the standard mod

Scaling has improved for the 5-Voltage ranges from 2.75 to 1.6 and from 3.45 to 1.975 for the 1- and 2-ranges. From the screen's resolution we can calculate the use of the ADC's resolution. At a grid height of 400 pixels the resolution is 400 / Scaling. For the individual voltage ranges this is:

5-ranges	before 145	after 250
2-ranges	before 115	after 202
1-ranges	before 115	after 202

In the 5-voltage ranges, the resolution is almost fully used. If you want to leave some spare, you can reduce the gain a bit. To do this you can choose a higher terminating resistor (300Ω or 270Ω) or a somewhat higher R_{14} at OPA656 (205 Ω or 210 Ω).
Essentially changes to R_{14} have a stronger effect on the gain than changes to the terminator. The necessary adjustments of the scaling can be done with the gain in the hardware menu.

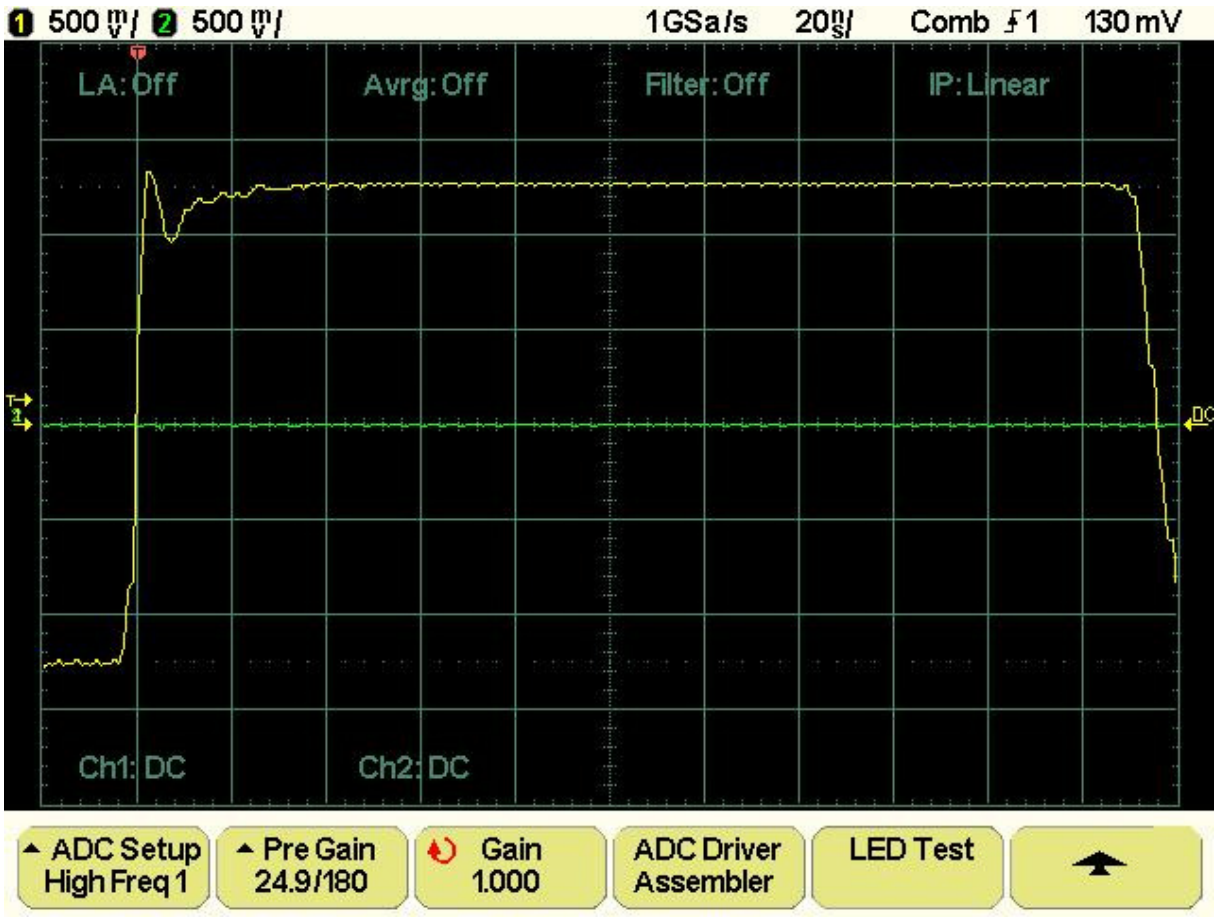

Fig 14: Noise with LB-mod

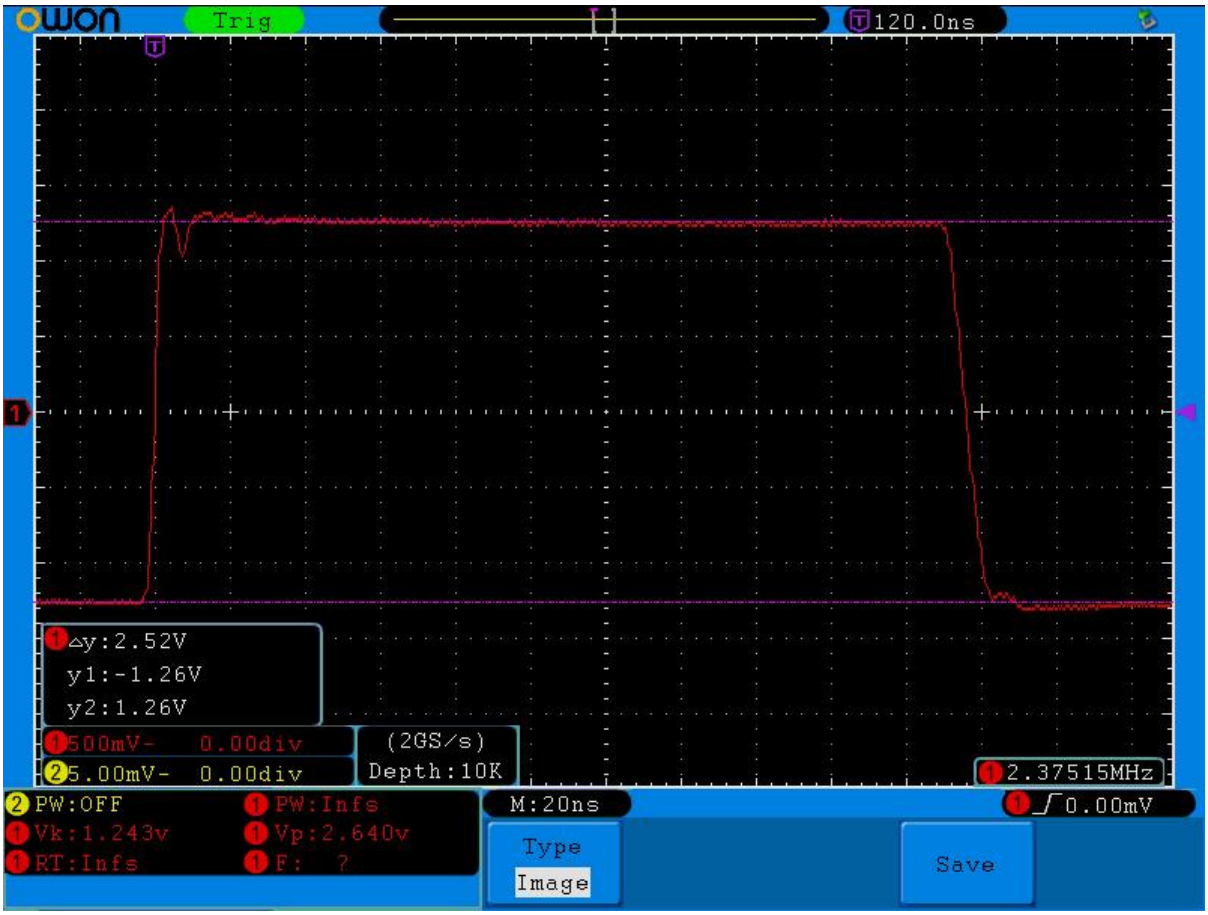

Fig 15: SDS8102

Bill of Material

Part Number	Value	Form factor	Number per channel
R_{14}	200Ω (1%)	SMD 0603	1
R_{22}	100Ω (1%)	SMD 0603	1
R_{31}/R_{32}	24.9Ω (1%)	SMD 0603	2
R_A	330Ω (1%)	SMD 0603	1
C_{12}	10pF (10%)	SMD 0603	1