Libraries Guide

ISE 8.1i

XILINX®

About This Guide

The Libraries Guide is part of the ISE documentation collection.

Guide Contents

This guide contains the following:

- Discussion of the Xilinx Unified Libraries
- Slice Count information for FPGAs
- Design elements associated with the following architectures are described in this guide.
  - Spartan™-II
  - Spartan™-IIE
  - Spartan™-3
  - Virtex™
  - Virtex™-E
  - Virtex™-II
  - Virtex™-II Pro
  - Virtex™-II Pro X
  - XC9500™
  - XC9500XV™
  - XC9500XL™
  - CoolRunner™ XPLA3
  - CoolRunner™-II
- A listing of the various Functional Categories of design elements
- Individual sections for each of the Design Elements.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File →Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*`option_name`*] *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr =`**{**`on`**|**`off`**}
Vertical bar |	Separates items in a list of choices	**`lowpwr =`**{**`on`**|**`off`**}

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Functional Categories

The functional categories list the available design elements in each category along with a brief description of each element that is supported under each Xilinx architecture.

Design Elements

Design elements are organized in alphanumeric order, with all numeric suffixes in ascending order. For example, FDR precedes FDRS, and ADD4 precedes ADD8, which precedes ADD16.

The following information is provided for each library element, where applicable:

- Name of the element
- Graphic symbol (only in the schematic version of the guide)
- Applicability table (with primitive versus macro identification)
- Functional description
- Truth table
- VHDL and Verilog instantiation and inference code (only in the HDL version of the guide)

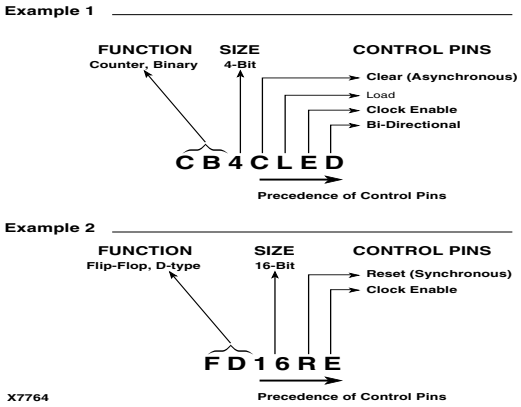
Schematic Examples

Schematics are included for each device library, if the implementation differs. These schematics are illustrated only in the schematic user version of the libraries guide for each Xilinx architecture.

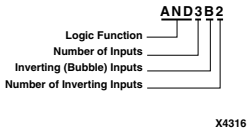
Design elements with bussed or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic -- generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

Naming Conventions

Examples of the general naming conventions for the unified library elements are shown in the following figures.



Naming Conventions



Combinatorial Naming Conventions

Attributes and Constraints

The terms attribute and constraint have been used interchangeably by some in the engineering community, while others ascribe different meanings to these terms. In addition, language constructs use the terms attribute and directive in similar yet different senses. For the purpose of clarification, the Xilinx documentation refers to the terms attributes and constraints as defined below.

Table of Contents

Design Elements

Xilinx Unified Libraries

This chapter describes the Unified Libraries and the applicable device architectures for each library. It also briefly discusses the contents of the other chapters, the general naming conventions, and performance issues.

This chapter consists of the following major sections.

Overview

Xilinx maintains software libraries with thousands of functional design elements (primitives and macros) for different device architectures. New functional elements are assembled with each release of development system software. The catalog of design elements is known as the Unified Libraries. Many of the elements in these libraries can be used in multiple Xilinx device architectures. This "unified" approach means that you can use your circuit design created with "unified" library elements across all current Xilinx device architectures that recognize the element you are using.

Elements that exist in multiple architectures look and function the same, but their implementations might differ to make them more efficient for a particular architecture. A separate library still exists for each architecture (or architectural group) and common symbols are duplicated in each one, which is necessary for simulation (especially board level) where timing depends on a particular architecture.

If you have active designs that were created with former Xilinx library primitives or macros, you may need to change references to the design elements that you were using to reflect the Unified Libraries elements.

The *Libraries Guide* describes the primitive and macro logic elements available in the Unified Libraries for the Xilinx FPGA and CPLD devices. Common logic functions can be implemented with these elements and more complex functions can be built by

combining macros and primitives. Several hundred design elements (primitives and macros) are available across multiple device architectures, providing a common base for programmable logic designs.

This libraries guide provides a functional selection guide and describes the design elements.

Applicable Architectures

Design elements for the Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex -II, Virtex-II Pro, Virtex-II Pro X, XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II libraries are included in the Xilinx Unified Libraries. Each library supports specific device architectures. For detailed information on the architectural families referenced below and the devices in each, see the current version of *The Programmable Logic Data Sheets*(an online version is available from the Xilinx web site, http://support.xilinx.com).

Functional Categories

The functional categories list the available elements in each category along with a brief description of each element and an applicability table identifying which libraries (Spartan-II, Spartan-IIE, Virtex, Virtex-E, Virtex -II, Virtex-II Pro, Virtex-II Pro X, XC9500/XV/XL, CoolRunner XPLA3, and CoolRunner-II) contain the element.

Design Elements

Design elements are organized in alphanumeric order, with all numeric suffixes in ascending order. For example, FDR precedes FDRS, and ADD4 precedes ADD8, which precedes ADD16.

The following information is provided for each library element, where applicable:

- Graphic symbol
- Applicability table (with primitive versus macro identification)
- Functional description
- Truth table
- Schematic for macros
- VHDL and Verilog instantiation and inference code
- Commonly used constraints

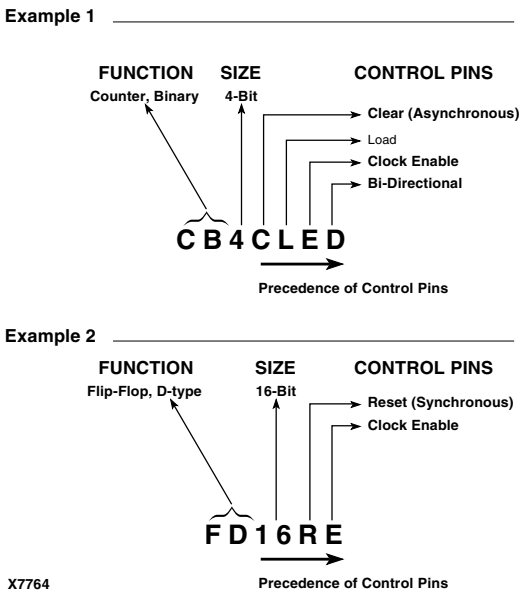
Schematic Examples

Schematics are included for each library if the implementation differs.

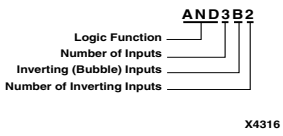
Design elements with bussed or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic -- generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

Naming Conventions

Examples of the general naming conventions for the unified library elements are shown in the following figures.



Naming Conventions



Combinatorial Naming Conventions

Attributes and Constraints

Attributes and constraints are instructions placed on components or nets to indicate their placement, implementation, naming, directionality, etc.. The *Constraints Guide* provides information on all attributes and constraints.

Carry Logic

The Spartan-II, Spartan-IIE, Virtex, and Virtex-II architectures include dedicated carry logic components.

Spartan-II, Spartan-IIE, Virtex, and Virtex-E

Carry Logic for Spartan-II, Spartan-IIE, Virtex, and Virtex-E is a simple structure associated with each look-up table. The design entry library contains the following dedicated carry logic primitives: MULT_AND, MUXCY, MUXCY_D, MUXCY_L, XORCY, XORCY_D, and XORCY_L. The function performed is determined by their

connectivity and the contents of the look-up table. For an example of how to use carry logic, see "CC8CE, CC16CE".

For detailed information on Carry Logic in Virtex and Spartan-II, see *The Programmable Logic Data Sheets* available on the Xilinx web site, http://support.xilinx.com.

Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Spartan-3

The dedicated carry logic primitives for Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Spartan-3 are MULT_AND, MUXCY, MUXCY_D, MUXCY_L, XORCY, XORCY_D, and XORCY_L.

ORCY can only be used exclusively with Virtex-II, Virtex-II Pro, and Virtex-II Pro X.

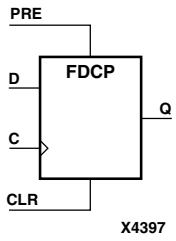
For detailed information on Carry Logic in Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Spartan-3, see *The Programmable Logic Data Sheets* available on the Xilinx web site, http://support.xilinx.com.

Flip-Flop, Counter, and Register Performance

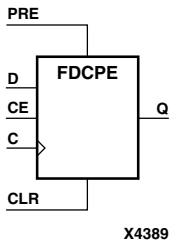
All counter, register, and storage functions derived from the flip-flops are available in the Configurable Logic Blocks (CLBs).

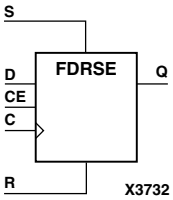
The D flip-flop is the basic building block for all architectures. Differences occur from the availability of asynchronous Clear (CLR) and Preset (PRE) inputs, and the source of the synchronous control signals, such as Clock Enable (CE), Clock (C), Load enable (L), synchronous Reset (R), and synchronous Set (S). The basic flip-flop configuration for each architecture follows.

The basic XC9000 flip-flops have both Clear and Preset inputs.



Virtex and Spartan-II have two basic flip-flop types. One has both Clear and Preset inputs and one has both asynchronous and synchronous control functions.





The asynchronous and synchronous control functions, when used, have a priority that is consistent across all devices and architectures. These inputs can be either active-High or active-Low as defined by the macro. The priority, from highest to lowest, is as follows.

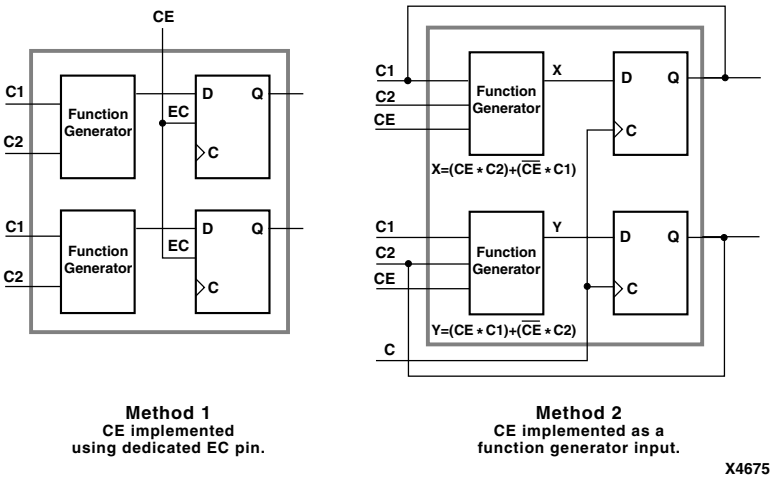
- Asynchronous Clear (CLR)
- Asynchronous Preset (PRE)
- Synchronous Set (S)
- Synchronous Reset (R)
- Clock Enable (CE)

Note: The asynchronous CLR and PRE inputs, by definition, have priority over all the synchronous control and clock inputs.

For FPGA families, the Clock Enable (CE) function is implemented using two different methods in the Xilinx Unified Libraries; both are shown in the following figure.

- In method 1, CE is implemented by connecting the CE pin of the macro directly to the dedicated Enable Clock (EC) pin of the internal Configurable Logic Block (CLB) flip-flop. This allows one CE per CLB. CE takes precedence over the L, S, and R inputs. All flip-flops with asynchronous clear or preset use this method.
- In method 2, CE is implemented using function generator logic. This allows two CEs per CLB. CE has the same priority as the L, S, and R inputs. All flip-flops with synchronous set or reset use this method.

The method used in a particular macro is indicated by the inclusion of asynchronous clear, asynchronous preset, synchronous set, or synchronous reset in the macro ' s description.



Clock Enable Implementation Methods

Unconnected Pins

Xilinx recommends that you *always* connect input pins in your designs. This ensures that front end simulation functionally matches back end timing simulation. If an input pin is left unconnected, mapper errors may result.

If an output pin is left unconnected in your design, the corresponding function is trimmed. If the component has only one output, the entire component is trimmed. If the component has multiple outputs, the portion that drives the output is trimmed. As an example of the latter case, if the overflow pin (OFL) in an adder macro is unconnected, the logic that generates that term is trimmed, but the rest of the adder is retained (assuming all of the sum outputs are connected).

Slice Count

This chapter contains the following sections.

About Configurable Logic Blocks (CLBs)

Configurable Logic Blocks (CLBs) implement most of the logic in an FPGA.

Each Virtex, Virtex-E and Spartan-II, Spartan-IIE CLB contains two slices. Each Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X CLB contains four slices. In the following table, the numbers for Spartan-II, Spartan-IIE, Virtex, Virtex-E, Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X are the number of slices required to implement the component.

The Slice Count table lists FPGA design elements in alphanumeric order with the number of CLBs or slices needed for their implementation in each applicable library.

Note: This information is for reference only. The actual count could vary, depending upon the switch settings of the implementation tools; for example, the effort level in PAR (Place and Route) or usage of the components with other components.

The asterisk for the RAM16X1D and RAM16X1D_1 in the Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X columns indicates that these design elements consume 1/2 of two slices.

The double asterisks for design elements indicate that these primitives cannot be used by themselves. However, there is only one available per slice.

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	**Number of Slices to Implement**			
ACC4	5	6	5	6
ACC8	9	10	9	10
ACC16	17	18	17	18
ADD4	3	3	3	3
ADD8	5	5	5	5
ADD16	9	9	9	9
ADSU4	3	3	3	3
ADSU8	5	5	5	5

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	**Number of Slices to Implement**			
ADSU16	9	9	9	9
AND2	1	1	1	1
AND3	1	1	1	1
AND4	1	1	1	1
AND5	1	1	1	1
AND6	1	1	1	1
AND7	1	1	1	1
AND8	2	2	2	2
AND9	2	2	2	2
AND12	2	2	2	2
AND16	2	2	2	2
BRLSHFT4	8	4	8	4
BRLSHFT8	12	12	12	12
BSCAN_SPARTAN2	-	-	-	-
BSCAN_VIRTEX	-	-	-	-
BSCAN_VIRTEX2	-	-	-	-
BUF	-	-	-	-
BUF4	-	-	-	-
BUF8	-	-	-	-
BUF16	-	-	-	-
BUFCF	-	-	-	-
BUFE	-	-	-	-
BUFE4	-	-	-	-
BUFE8	-	-	-	-
BUFE16	-	-	-	-
BUFG	-	-	-	-
BUFGCE	-	-	-	-
BUFGCE_1	-	-	-	-
BUFGDLL	-	-	-	-
BUFGMUX	-	-	-	-
BUFGMUX_1	-	-	-	-
BUFGP	-	-	-	-
BUFT	-	-	-	-
BUFT4	-	-	-	-
BUFT8	-	-	-	-
BUFT16	-	-	-	-
CAPTURE_SPARTAN2	-	-	-	-

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	**Number of Slices to Implement**			
CAPTURE_VIRTEX	-	-	-	-
CAPTURE_VIRTEX2	-	-	-	-
CB2CE	2	3	2	3
CB2CLE	3	3	3	3
CB2CLED	3	3	3	3
CB2RE	2	3	2	3
CB4CE	3	4	3	4
CB4CLE	5	5	5	5
CB4CLED	6	7	6	7
CB4RE	3	4	3	4
CB8CE	6	7	6	7
CB8CLE	9	10	9	10
CB8CLED	12	12	12	12
CB8RE	6	7	6	7
CB16CE	13	14	13	14
CB16CLE	18	19	18	19
CB16CLED	24	25	24	25
CB16RE	13	14	13	14
CC8CE	8	5	8	5
CC8CLE	9	9	9	9
CC8CLED	9	17	9	17
CC8RE	9	9	9	9
CC16CE	16	9	16	9
CC16CLE	17	17	17	17
CC16CLED	17	33	17	33
CC16RE	17	17	17	17
CD4CE	3	4	3	4
CD4CLE	5	5	5	5
CD4RE	3	4	3	4
CD4RLE	7	7	7	7
CJ4CE	2	4	2	4
CJ4RE	2	4	2	4
CJ5CE	3	5	3	5
CJ5RE	3	5	3	5
CJ8CE	4	4	4	4
CJ8RE	4	4	4	4
CLKDLL	-	-	-	-

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	Number of Slices to Implement			
CLKDLLE	-	-	-	-
CLKDLLHF	-	-	-	-
COMP2	1	1	1	1
COMP4	2	2	2	2
COMP8	3	4	3	4
COMP16	6	9	6	9
COMPM2	1	2	1	2
COMPM4	5	5	5	5
COMPM8	11	13	11	13
COMPM16	24	32	24	32
COMPMC8	8	8	8	8
COMPMC16	16	16	16	16
CR8CE	8	8	8	8
CR16CE	16	16	16	16
D2_4E	2	2	2	2
D3_8E	4	4	4	4
D4_16E	16	16	16	16
DCM	-	-	-	-
DEC_CC4	1	1	1	1
DEC_CC8	1	1	1	1
DEC_CC16	2	2	2	2
DECODE4	1	1	1	1
DECODE8	2	2	2	2
DECODE16	2	2	2	2
DECODE32	4	4	4	4
DECODE64	8	8	8	8
FD	1	1	1	1
FD_1	1	1	1	1
FD4CE	2	4	2	4
FD4RE	2	4	2	4
FD8CE	4	4	4	4
FD8RE	4	4	4	4
FD16CE	8	8	8	8
FD16RE	8	8	8	8
FDC	1	1	1	1
FDC_1	1	1	1	1
FDCE	1	1	1	1

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	Number of Slices to Implement			
FDCE_1	1	1	1	1
FDCP	1	1	1	1
FDCP_1	1	1	1	1
FDCPE	1	1	1	1
FDCPE_1	1	1	1	1
FDDRCPE	-	-	-	-
FDDRRSE	-	-	-	-
FDE	1	1	1	1
FDE_1	1	1	1	1
FDP	1	1	1	1
FDP_1	1	1	1	1
FDPE	1	1	1	1
FDPE_1	1	1	1	1
FDR	1	1	1	1
FDR_1	1	1	1	1
FDRE	1	1	1	1
FDRE_1	1	1	1	1
FDRS	1	1	1	1
FDRS_1	1	1	1	1
FDRSE	1	1	1	1
FDRSE_1	1	1	1	1
FDS	1	1	1	1
FDS_1	1	1	1	1
FDSE	1	1	1	1
FDSE_1	1	1	1	1
FJKC	1	1	1	1
FJKCE	1	1	1	1
FJKP	1	1	1	1
FJKPE	1	1	1	1
FJKRSE	1	1	1	1
FJKSRE	1	1	1	1
FMAP	-	-	-	-
FTC	1	1	1	1
FTCE	1	1	1	1
FTCLE	1	1	1	1
FTCLEX	1	1	1	1
FTP	1	1	1	1

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	**Number of Slices to Implement**			
FTPE	1	1	1	1
FTPLE	1	1	1	1
FTRSE	1	1	1	1
FTRSLE	2	1	2	1
FTSRE	1	1	1	1
FTSRLE	2	2	2	2
GND	-	-	-	-
GT_AURORA_*n*	-	-	-	-
GT_CUSTOM_*n*	-	-	-	-
GT_ETHERNET_*n*	-	-	-	-
GT_FIBRE_CHAN_*n*	-	-	-	-
GT_INFINIBAND_*n*	-	-	-	-
GT_XAUI_*n*	-	-	-	-
GT10_AURORA_*n*	-	-	-	-
GT10_AURORAX_*n*	-	-	-	-
GT10_CUSTOM_*n*	-	-	-	-
GT10_INFINIBAND_*n*	-	-	-	-
GT10_XAUI_*n*	-	-	-	-
GT10_10GE_*n*	-	-	-	-
GT10_10GFC_*n*	-	-	-	-
GT10_OC48_*n*	-	-	-	-
GT10_OC192_*n*	-	-	-	-
IBUF	-	-	-	-
IBUF4	-	-	-	-
IBUF8	-	-	-	-
IBUF16	-	-	-	-
IBUFDS	-	-	-	-
IBUFG	-	-	-	-
IBUFGDS	-	-	-	-
ICAP_VIRTEX2	-	-	-	-
IFD	-	-	-	-
IFD_1	-	-	-	-
IFD4	-	-	-	-
IFD8	-	-	-	-
IFD16	-	-	-	-
IFDDRCPE	-	-	-	-
IFDDRRSE	-	-	-	-

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	Number of Slices to Implement			
IFDI	-	-	-	-
IFDI_1	-	-	-	-
IFDX	-	-	-	-
IFDX4	-	-	-	-
IFDX8	-	-	-	-
IFDX16	-	-	-	-
IFDX_1	-	-	-	-
IFDXI	-	-	-	-
IFDXI_1	-	-	-	-
ILD	1	1	1	1
ILD_1	1	1	1	1
ILD4	2	2	2	2
ILD8	4	4	4	4
ILD16	8	8	8	8
ILDI	-	-	-	-
ILDI_1	-	-	-	-
ILDX	-	-	-	-
ILDX4	-	-	-	-
ILDX8	-	-	-	-
ILDX16	-	-	-	-
ILDX_1	-	-	-	-
ILDXI	-	-	-	-
ILDXI_1	-	-	-	-
INV	1	1	1	1
INV4	1	1	1	1
INV8	1	1	1	1
INV16	1	1	1	1
IOBUF	-	-	-	-
IOPAD	-	-	-	-
IOPAD4	-	-	-	-
IOPAD8	-	-	-	-
IOPAD16	-	-	-	-
IPAD	-	-	-	-
IPAD4	-	-	-	-
IPAD8	-	-	-	-
IPAD16	-	-	-	-
JTAGPPC	-	-	-	-

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	Number of Slices to Implement			
KEEPER	-	-	-	-
LD	1	1	1	1
LD_1	1	1	1	1
LD4	2	4	2	4
LD8	4	4	4	4
LD16	8	8	8	8
LD4CE	2	4	2	4
LD8CE	4	4	4	4
LD16CE	8	8	8	8
LDC	1	1	1	1
LDC_1	1	1	1	1
LDCE	1	1	1	1
LDCE_1	1	1	1	1
LDCP	1	1	1	1
LDCP_1	1	1	1	1
LDCPE	1	1	1	1
LDCPE_1	1	1	1	1
LDE	1	1	1	1
LDE_1	1	1	1	1
LDP	1	1	1	1
LDP_1	1	1	1	1
LDPE	1	1	1	1
LDPE_1	1	1	1	1
LUT1	1	1	1	1
LUT2	1	1	1	1
LUT3	1	1	1	1
LUT4	1	1	1	1
LUT1_D	1	1	1	1
LUT2_D	1	1	1	1
LUT3_D	1	1	1	1
LUT4_D	1	1	1	1
LUT1_L	1	1	1	1
LUT2_L	1	1	1	1
LUT3_L	1	1	1	1
LUT4_L	1	1	1	1
M2_1	1	1	1	1
M2_1B1	1	1	1	1

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	Number of Slices to Implement			
M2_1B2	1	1	1	1
M2_1E	1	1	1	1
M4_1E	1	1	1	1
M8_1E	2	2	2	2
M16_1E	5	5	5	5
MULT_AND **	-	-	-	-
MULT18X18	-	-	-	-
MULT18X18S	-	-	-	-
MUXCY **	-	-	-	-
MUXCY_D **	-	-	-	-
MUXCY_L **	-	-	-	-
MUXF5 **	-	-	-	-
MUXF5_D **	-	-	-	-
MUXF5_L **	-	-	-	-
MUXF6 **	-	-	-	-
MUXF6_D **	-	-	-	-
MUXF6_L **	-	-	-	-
MUXF7 **	-	-	-	-
MUXF7_D **	-	-	-	-
MUXF7_L **	-	-	-	-
MUXF8 **	-	-	-	-
MUXF8_D **	-	-	-	-
MUXF8_L **	-	-	-	-
NAND2	1	1	1	1
NAND3	1	1	1	1
NAND4	1	1	1	1
NAND5	1	1	1	1
NAND6	1	1	1	1
NAND7	1	1	1	1
NAND8	2	2	2	2
NAND9	2	2	2	2
NAND12	2	2	2	2
NAND16	2	2	2	2
NOR2	1	1	1	1
NOR3	1	1	1	1
NOR4	1	1	1	1
NOR5	1	1	1	1

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	**Number of Slices to Implement**			
NOR6	1	1	1	1
NOR7	1	1	1	1
NOR8	2	2	2	2
NOR9	2	2	2	2
NOR12	2	2	2	2
NOR16	2	2	2	2
OBUF	-	-	-	-
OBUF4	-	-	-	-
OBUF8	-	-	-	-
OBUF16	-	-	-	-
OBUFDS	-	-	-	-
OBUFE	-	-	-	-
OBUFE4	-	-	-	-
OBUFE8	-	-	-	-
OBUFE16	-	-	-	-
OBUFT	-	-	-	-
OBUFT4	-	-	-	-
OBUFT8	-	-	-	-
OBUFT16	-	-	-	-
OBUFTDS	-	-	-	-
OFD	-	-	-	-
OFD_1	-	-	-	-
OFD4	-	-	-	-
OFD8	-	-	-	-
OFD16	-	-	-	-
OFDDRCPE	-	-	-	-
OFDDRRSE	-	-	-	-
OFDDRTCPE	-	-	-	-
OFDDRTRSE	-	-	-	-
OFDE	-	-	-	-
OFDE_1	-	-	-	-
OFDE4	-	-	-	-
OFDE8	-	-	-	-
OFDE16	-	-	-	-
OFDI	-	-	-	-
OFDI_I	-	-	-	-
OFDT	-	-	-	-

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	**Number of Slices to Implement**			
OFDT_1	-	-	-	-
OFDT4	-	-	-	-
OFDT8	-	-	-	-
OFDT16	-	-	-	-
OFDX	-	-	-	-
OFDX4	-	-	-	-
OFDX8	-	-	-	-
OFDX16	-	-	-	-
OFDX_1	-	-	-	-
OFDXI	-	-	-	-
OFDXI_I	-	-	-	-
OPAD	-	-	-	-
OPAD4	-	-	-	-
OPAD8	-	-	-	-
OPAD16	-	-	-	-
OR2	1	1	1	1
OR3	1	1	1	1
OR4	1	1	1	1
OR5	1	1	1	1
OR6	1	1	1	1
OR7	1	1	1	1
OR8	2	2	2	2
OR9	2	2	2	2
OR12	2	2	2	2
OR16	2	2	2	2
ORCY **	-	-	-	-
PPC405	-	-	-	-
PULLDOWN	-	-	-	-
PULLUP	-	-	-	-
RAM16X1D	1	2*	1	2*
RAM16X1D_1	1	2*	1	2*
RAM16X1S	1	1	1	1
RAM16X1S_1	1	1	1	1
RAM16X2D	2	4	2	4
RAM16X2S	2	2	2	2
RAM16X4D	4	8	4	8
RAM16X4S	4	3	4	3

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	Number of Slices to Implement			
RAM16X8D	8	16	8	16
RAM16X8S	8	5	8	5
RAM32X1D	-	2	-	2
RAM32X1D_1	-	2	-	2
RAM32X1S	1	1	1	1
RAM32X1S_1	1	1	1	1
RAM32X2S	2	2	2	2
RAM32X4S	8	3	8	3
RAM32X8S	-	6	-	6
RAM64X1D	-	-	-	4
RAM64X1D_1	-	4	-	4
RAM64X1S	-	2	-	2
RAM64X1S_1	-	2	-	2
RAM64X2S	-	4	-	4
RAM128X1S	-	4	-	4
RAM128X1S_1	-	4	-	4
RAMB4_Sn	-	-	-	-
RAMB4_Sm_Sn	-	-	-	-
RAMB16_Sn	-	-	-	-
RAMB16_Sm_Sn	-	-	-	-
ROM16X1	1	1	1	1
ROM32X1	1	1	1	1
ROM64X1	2	2	2	2
ROM128X1	-	4	-	4
ROM256X1	-	8	-	8
SOP3	1	1	1	1
SOP4	1	1	1	1
SR4CE	2	4	2	4
SR4CLE	3	3	3	3
SR4CLED	5	5	5	5
SR4RE	2	4	2	4
SR4RLE	3	3	3	3
SR4RLED	5	5	5	5
SR8CE	4	4	4	4
SR8CLE	5	5	5	5
SR8CLED	9	9	9	9
SR8RE	4	4	4	4

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	Number of Slices to Implement			
SR8RLE	5	5	5	5
SR8RLED	9	9	9	9
SR16CE	8	8	8	8
SR16CLE	9	9	9	9
SR16CLED	17	17	17	17
SR16RE	8	8	8	8
SR16RLE	9	9	9	9
SR16RLED	17	17	17	17
SRL16	1	1	1	1
SRL16_1	1	1	1	1
SRL16E	1	1	1	1
SRL16E_1	1	1	1	1
SRLC16	-	1	-	1
SRLC16_1	-	1	-	1
SRLC16E	-	1	-	1
SRLC16E_1	-	1	-	1
STARTUP_SPARTAN2	-	-	-	-
STARTUP_VIRTEX	-	-	-	-
STARTUP_VIRTEX2	-	-	-	-
UPAD	-	-	-	-
VCC	-	-	-	-
XNOR2	1	1	1	1
XNOR3	1	1	1	1
XNOR4	1	1	1	1
XNOR5	1	1	1	1
XNOR6	1	1	1	1
XNOR7	1	1	1	1
XNOR8	2	2	2	2
XNOR9	2	2	2	2
XOR2	1	1	1	1
XOR3	1	1	1	1
XOR4	1	1	1	1
XOR5	1	1	1	1
XOR6	1	1	1	1
XOR7	1	1	1	1
XOR8	2	2	2	2
XOR9	2	2	2	2

Slice Count for FPGA Components

Design Element	Spartan-II, Spartan-IIE	Spartan-3	Virtex, Virtex-E	Virtex-II, Virtex-II Pro, Virtex-II Pro X
Name	**Number of Slices to Implement**			
XORCY **	-	-	-	-
XORCY_D **	-	-	-	-
XORCY_L **	-	-	-	-

* The RAM16X1D and RAM16X1D_1 consume 1/2 of two slices.

** These primitives cannot be used by themselves. However, there is only one available per slice.

Functional Categories

This section categories, by function, the logic elements that are described in detail in the "Design Elements" sections. Each category is briefly described. Tables under each category identify all the available elements for the function and indicate which architectures are supported by each.

Elements are listed in alphanumeric order under each category.

The Xilinx libraries contain three types of elements.

- Primitives are basic logical elements such as AND2 and OR2 gates.
- Soft macros are schematics made by combining primitives and sometimes other soft macros.
- Relationally placed macros (RPMs) are soft macros that contain relative location constraint (RLOC) information, carry logic symbols, and FMAP symbols, where appropriate.

The last item mentioned above, RPMs, applies only to FPGA families.

The relationally placed macro (RPM) library uses RLOC constraints to define the order and structure of the underlying design primitives. Because these macros are built upon standard schematic parts, they do not have to be translated before simulation. The components that are implemented as RPMs are listed in the "Slice Count" section.

Designs created with RPMs can be functionally simulated. RPMs can, but need not, include all the following elements.

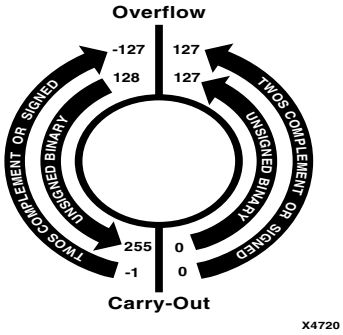
- Relative location (RLOC) constraints to provide placement structure. They allow positioning of elements relative to each other.
- Carry logic primitive symbols.

The RPM library offers the functionality and precision of the hard macro library with added flexibility. You can optimize RPMs and merge other logic within them. The elements in the RPM library allow you to access carry logic easily and to control mapping and block placement. Because RPMs are a superset of ordinary macros, you can design them in the normal design entry environment. They can include any

primitive logic. The macro logic is fully visible to you and can be easily back-annotated with timing information.

Arithmetic Functions

There are three types of arithmetic functions: accumulators (ACC), adders (ADD), and adder/subtracters (ADSU). With an ADSU, either unsigned binary or twos-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated. The following figure shows the ADSU carry-out and overflow boundaries.



ADSU Carry-Out and Overflow Boundaries

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
ACC1	1-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset	No	No	No	No	Primitive	Primitive	Primitive
ACC4	4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
ACC8	8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
ACC16	16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
ADD1	1-Bit Full Adder with Carry-In and Carry-Out	No	No	No	No	Primitive	Primitive	Primitive
ADD4	4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
ADD8	8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
ADD16	16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
ADSU1	1-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out	No	No	No	No	Primitive	Primitive	Primitive
ADSU4	4-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
ADSU8	8-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
ADSU16	16-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow	Macro	Macro	Macro	Macro	Macro	Macro	Macro
MULT18X18	18 x 18 Signed Multiplier	No	Primitive	No	Primitive	No	No	No
MULT18X18S	18 x 18 Signed Multiplier -- Registered Version	No	Primitive	No	Primitive	No	No	No

Buffers

The buffers in this section route high fanout signals, 3-state signals, and clocks inside a PLD device. The "Input/Output Functions" section covers off-chip interfaces.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500 /XV/XL	CR XPLA3	CR-II
BUF	General Purpose Buffer	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
BUF4	4-Bit General Purpose Buffer	Macro	No	No	No	Primitive	Primitive	Primitive
BUF8	8-Bit General Purpose Buffer	Macro	No	No	No	Primitive	Primitive	Primitive
BUF16	16-Bit General Purpose Buffer	Macro	No	No	No	Primitive	Primitive	Primitive
BUFCF	Fast Connect Buffer	Primitive	Primitive	Primitive	Primitive	No	No	No
BUFE	Internal 3-State Buffer with Active High Enable	Primitive	No	Primitive	Primitive	Primitive[a]	No	No
BUFE4	Internal 3-State Buffer with Active High Enable	Primitive	No	Macro	Macro	Primitive	No	No
BUFE8	Internal 3-State Buffer with Active High Enable	Primitive	No	Macro	Macro	Primitive	No	No
BUFE16	Internal 3-State Buffer with Active High Enable	Primitive	No	Macro	Macro	Primitive	No	No
BUFG	Global Clock Buffer	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
BUFGCE	Global Clock MUX with Clock Enable and Output State 0	No	Primitive	No	Primitive	No	No	No
BUFGCE_1	Global Clock MUX Buffer with Clock Enable and Output State 1	No	Primitive	No	Primitive	No	No	No
BUFGDLL	Clock Delay Locked Loop Buffer	Primitive	Primitive	Primitive	Primitive	No	No	No
BUFGMUX	Global Clock MUX Buffer with Output State 0	No	Primitive	No	Primitive	No	No	No
BUFGMUX_1	Global Clock MUX with Output State 1	No	Primitive	No	Primitive	No	No	No
BUFGP	Primary Global Buffer for Driving Clocks or Longlines (Four per PLD Device)	Primitive	Primitive	Primitive	Primitive	No	No	No
BUFGSR	Global Set/Reset Input Buffer	No	No	No	No	Primitive	Primitive	Primitive
BUFGTS	Global 3-State Input Buffer	No	No	No	No	Primitive	Primitive	Primitive
BUFT	Internal 3-State Buffer with Active-Low Enable	Primitive	No	Primitive	Primitive	Primitive[b]	No	No
BUFT4	Internal 3-State Buffer with Active-Low Enable	Macro	No	Macro	Macro	Primitive	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500 /XV/XL	CR XPLA3	CR-II
BUFT8	Internal 3-State Buffer with Active-Low Enable	Macro	No	Macro	Macro	Primitive[c]	No	No
BUFT16	Internal 3-State Buffer with Active-Low Enable	Macro	No	Macro	Macro	Primitive	No	No

a.Not supported for XC9500XL and XC9500XV devices.

b.Not supported for XC9500XL and XC9500XV devices.

c.Not supported for XC9500XL and XC9500XV devices.

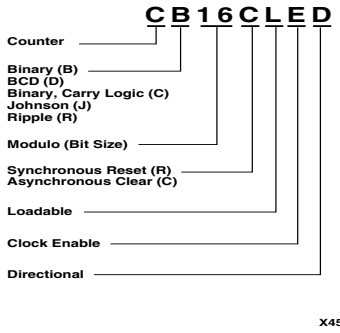
Comparators

Following is a list of comparators.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
COMP2	2-Bit Identity Comparator	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
COMP4	4-Bit Identity Comparator	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
COMP8	8-Bit Identity Comparator	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
COMP16	16-Bit Identity Comparator	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
COMPM2	2-Bit Magnitude Comparator	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
COMPM4	4-Bit Magnitude Comparator	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
COMPM8	8-Bit Magnitude Comparator	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
COMPM16	16-Bit Magnitude Comparator	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
COMPMC8	8-Bit Magnitude Comparator	Macro	Macro	Macro	Macro	No	No	No
COMPMC16	16-Bit Magnitude Comparator	Macro	Macro	Macro	Macro	No	No	No

Counters

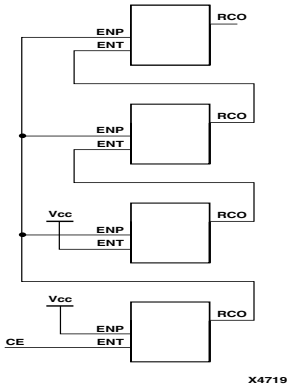
There are six types of counters with various synchronous and asynchronous inputs. The name of the counter defines the modulo or bit size, the counter type, and which control functions are included. The counter naming convention is shown in the following figured:



Counter Naming Convention

A carry-lookahead design accommodates large counters without extra gating. On TTL 7400-type counters with trickle clock enable (ENT), parallel clock enable (ENP), and ripple carry-out (RCO), both the ENT and ENP inputs must be High to count. ENT is

propagated forward to enable RCO, which produces a High output with the approximate duration of the QA output. The following figure illustrates a carry-lookahead design.



Carry-Lookahead Design

The RCO output of the first stage of the ripple carry is connected to the ENP input of the second stage and all subsequent stages. The RCO output of the second stage and all subsequent stages is connected to the ENT input of the next stage. The ENT of the second stage is always enabled/tied to VCC. CE is always connected to the ENT input of the first stage. This cascading method allows the first stage of the ripple carry to be built as a prescaler. In other words, the first stage is built to count very fast.

Note: For counters, do not use TC (or any other gated signal) as a clock. Possible glitches may not always allow for a proper setup time when using gated signals.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
CB2CE	2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CB4CE	4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CB8CE	8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CB16CE	16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CB2CLE	2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear	No	No	No	No	Primitive	Primitive	Primitive
CB4CLE	4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear	No	No	No	No	Primitive	Primitive	Primitive
CB8CLE	8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear	No	No	No	No	Primitive	Primitive	Primitive
CB16CLE	16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear	No	No	No	No	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
CB2CLED	2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear	No	No	No	No	Primitive	Primitive	Primitive
CB4CLED	2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear	No	No	No	No	Primitive	Primitive	Primitive
CB8CLED	2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear	No	No	No	No	Primitive	Primitive	Primitive
CB16CLED	2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear	No	No	No	No	Primitive	Primitive	Primitive
CB2RE	2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CB4RE	4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CB8RE	8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CB16RE	16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CB2RLE	2-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset	No	No	No	Macro	Primitive	Primitive	Primitive
CB4RLE	4-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset	No	No	No	Macro	Primitive	Primitive	Primitive
CB8RLE	8-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset	No	No	No	Macro	Primitive	Primitive	Primitive
CB16RLE	16-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset	No	No	No	Macro	Primitive	Primitive	Primitive
CB2X1	2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asyn-chronous Clear	No	No	No	Macro	Primitive	Primitive	Primitive
CB4X1	4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asyn-chronous Clear	No	No	No	Macro	Primitive	Primitive	Primitive
CB8X1	8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asyn-chronous Clear	No	No	No	Macro	Primitive	Primitive	Primitive
CB16X1	16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asyn-chronous Clear	No	No	No	Macro	Primitive	Primitive	Primitive
CB2X2	2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchro-nous Reset	No	No	No	Macro	Primitive	Primitive	Primitive
CB4X2	4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchro-nous Reset	No	No	No	Macro	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
CB8X2	8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchro-nous Reset	No	No	No	Macro	Primitive	Primitive	Primitive
CB16X2	16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchro-nous Reset	No	No	No	Macro	Primitive	Primitive	Primitive
CBD2CE	2-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD4CE	4-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD8CE	8-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD16CE	16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD2CLE	2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD4CLE	4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD8CLE	8-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD16CLE	16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD2CLED	2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD4CLED	4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD8CLED	8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD16CLED	16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD2RE	2-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD4RE	4-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive

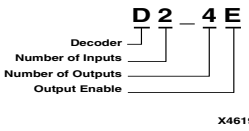
Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
CBD8RE	8-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD16RE	16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD2RLE	2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD4RLE	4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD8RLE	8-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD16RLE	16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD2X1	2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD4X1	4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD8X1	8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD16X1	16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CBD2X2	2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD4X2	4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD8X2	8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CBD16X2	16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CC8CE	8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	No	No	No
CC16CE	16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	No	No	No
CC8CLE	8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
CC16CLE	16-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	No	No	No
CC8CLED	8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	No	No	No
CC16CLED	16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	No	No	No
CC8RE	8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	No	No	No
CC16RE	16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	No	No	No
CD4CE	4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CD4CLE	4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CD4RE	4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CD4RLE	4-Bit Cascadable BCD Counter with Clock Enable And Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CDD4CE	4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CDD4CLE	4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CDD4RE	4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CDD4RLE	4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CD4RE	4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CD4RLE	4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CJ4CE	4-Bit Johnson Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CJ5CE	5-Bit Johnson Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CJ8CE	8-Bit Johnson Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CJ4RE	4-Bit Johnson Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CJ5RE	5-Bit Johnson Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CJ8RE	8-Bit Johnson Counter with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
CJD4CE	4-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CJD5CE	5-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CJD8CE	8-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CJD4RE	4-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CJD5RE	5-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CJD8RE	8-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
CR8CE	8-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CR16CE	16-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
CRD8CE	8-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
CRD16CE	16-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive

Decoders

Decoder names, shown in the following figure, indicate the number of inputs and outputs and whether or not an enable is available. Decoders with an enable can be used as multiplexers.



Decoder Naming Convention

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
D2_4E	2- to 4-Line Decoder/Demultiplexer with Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
D3_8E	3- to 8-Line Decoder/Demultiplexer with Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
D4_16E	4- to 16-Line Decoder/Demultiplexer with Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
DEC_CC4	4-Bit Active Low Decoder	Macro	Macro	Macro	Macro	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
DEC_CC8	8-Bit Active Low Decoder	Macro	Macro	Macro	Macro	No	No	No
DEC_CC16	16-Bit Active Low Decoder	Macro	Macro	Macro	Macro	No	No	No

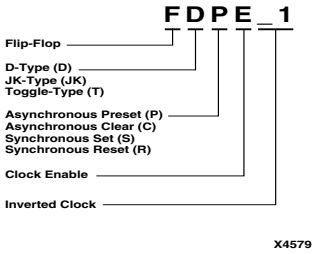
Edge Decoders

Edge decoders are open-drain wired AND gates that are available in different bit sizes.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
DECODE4	4-Bit Active-Low Decoder	Macro	Macro	Macro	Macro	No	No	No
DECODE8	8-Bit Active-Low Decoder	Macro	Macro	Macro	Macro	No	No	No
DECODE16	16-Bit Active-Low Decoder	Macro	Macro	Macro	Macro	No	No	No
DECODE32	32-Bit Active-Low Decoder	Macro	Macro	Macro	Macro	No	No	No
DECODE64	64-Bit Active-Low Decoder	Macro	Macro	Macro	Macro	No	No	No

Flip-Flops

There are three types of flip-flops (D, J-K, toggle) with various synchronous and asynchronous inputs. Some are available with inverted clock inputs and/or the ability to set in response to global set/reset rather than reset. The naming convention shown in the following figure provides a description for each flip-flop. D-type flip-flops are available in multiples of up to 16 in one macro.



Flip-Flop Naming Convention

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
FD	D Flip-Flop	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FD_1	D Flip-Flop with Negative-Edge Clock	Primitive	Primitive	Primitive	Primitive	No	No	No
FD4	Multiple D Flip-Flop	No	No	No	No	Primitive	Primitive	Primitive
FD8	Multiple D Flip-Flop	No	No	No	No	Primitive	Primitive	Primitive
FD16	Multiple D Flip-Flop	No	No	No	No	Primitive	Primitive	Primitive
FD4CE	4-Bit Data Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FD8CE	8-Bit Data Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FD16CE	16-Bit Data Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
FD4RE	4-Bit Data Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FD8RE	8-Bit Data Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FD16RE	16-Bit Data Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FDC	D Flip-Flop with Asynchronous Clear	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDC_1	D Flip-Flop with Negative-Edge Clock and Asynchronous Clear	Primitive	Primitive	Primitive	Primitive	No	No	No
FDCE	D Flip-Flop with Clock Enable and Asynchronous Clear	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDCE_1	D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear	Primitive	Primitive	Primitive	Primitive	No	No	No
FDCP	D Flip-Flop with Asynchronous Preset and Clear	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDCP_1	D Flip-Flop with Negative-Edge Clock and Asynchronous Preset and Clear	Primitive	Primitive	Primitive	Primitive	No	No	No
FDCPE	D Flip-Flop with Clock Enable and Asynchronous Preset and Clear	Primitive	Primitive	Primitive	Primitive	Macro	Macro	Primitive
FDCPE_1	D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset and Clear	Primitive	Primitive	Primitive	Primitive	No	No	No
FDD	Dual Edge Triggered D Flip-Flop	No	No	No	No	No	No	Primitive
FDD4	Multiple Dual Edge Triggered D Flip-Flop	No	No	No	No	No	No	Primitive
FDD8	Multiple Dual Edge Triggered D Flip-Flop	No	No	No	No	No	No	Primitive
FDD16	Multiple Dual Edge Triggered D Flip-Flop	No	No	No	No	No	No	Primitive
FDD4CE	4-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
FDD8CE	8-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
FDD16CE	16-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
FDD4RE	4-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
FDD8RE	8-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
FDD16RE	16-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
FDDC	D Dual Edge Triggered Flip-Flop with Asynchronous Clear	No	No	No	No	No	No	Primitive
FDDCE	Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
FDDCP	Dual Edge Triggered D Flip-Flop Asynchronous Preset and Clear	No	No	No	No	No	No	Primitive
FDDCPE	Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset and Clear	No	No	No	No	No	No	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
FDDP	Dual Edge Triggered D Flip-Flop with Asynchronous Preset	No	No	No	No	No	No	Primitive
FDDPE	Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset	No	No	No	No	No	No	Primitive
FDDR	Dual Edge Triggered D Flip-Flop with Synchronous Reset	No	No	No	No	No	No	Primitive
FDDRCPE	Dual Data Rate D Flip-Flop with Clock Enable and Asynchronous Preset and Clear	No	Primitive	No	Primitive	No	No	No
FDDRE	Dual Edge Triggered D Flip-Flop with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
FDDRSE	Dual Data Rate D Flip-Flop with Clock Enable and Synchronous Reset and Set	No	Primitive	No	Primitive	No	No	No
FDDRS	Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set	No	No	No	No	No	No	Primitive
FDDRSE	Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set and Clock Enable	No	No	No	No	No	No	Primitive
FDDS	Dual Edge Triggered D Flip-Flop with Synchronous Set	No	No	No	No	No	No	Primitive
FDDSE	D Flip-Flop with Clock Enable and Synchronous Set	No	No	No	No	No	No	Primitive
FDDSR	Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset	No	No	No	No	No	No	Primitive
FDDSRE	Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset and Clock Enable	No	No	No	No	No	No	Primitive
FDE	D Flip-Flop with Clock Enable	Primitive	Primitive	Primitive	Primitive	No	No	No
FDE_1	D Flip-Flop with Negative-Edge Clock and Clock Enable	Primitive	Primitive	Primitive	Primitive	No	No	No
FDP	D Flip-Flop with Asynchronous Preset	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDP_1	D Flip-Flop with Negative-Edge Clock and Asynchronous Preset	Primitive	Primitive	Primitive	Primitive	No	No	No
FDPE	D Flip-Flop with Clock Enable and Asynchronous Preset	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDPE_1	D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset	Primitive	Primitive	Primitive	Primitive	No	No	No
FDR	D Flip-Flop with Synchronous Reset	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDR_1	D Flip-Flop with Negative-Edge Clock and Synchronous Reset	Primitive	Primitive	Primitive	Primitive	No	No	No
FDRE	D Flip-Flop with Clock Enable and Synchronous Reset	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDRE_1	D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset	Primitive	Primitive	Primitive	Primitive	No	No	No
FDRS	D Flip-Flop with Synchronous Reset and Set	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDRS_1	D Flip-Flop with Negative-Clock Edge and Synchronous Reset and Set	Primitive	Primitive	Primitive	Primitive	No	No	No
FDRSE	D Flip-Flop with Synchronous Reset and Set and Clock Enable	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
FDRSE_1	D Flip-Flop with Negative-Clock Edge, Synchronous Reset and Set, and Clock Enable	Primitive	Primitive	Primitive	Primitive	No	No	No
FDS	D Flip-Flop with Synchronous Set	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDS_1	D Flip-Flop with Negative-Edge Clock and Synchronous Set	Primitive	Primitive	Primitive	Primitive	No	No	No
FDSE	D Flip-Flop with Clock Enable and Synchronous Set	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
FDSE_1	D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set	Primitive	Primitive	Primitive	No	No	No	No
FDSR	D Flip-Flop with Synchronous Set and Reset	No	No	No	No	Primitive	Primitive	Primitive
FDSRE	D Flip-Flop with Synchronous Set and Reset and Clock Enable	No	No	No	No	Primitive	Primitive	Primitive
FJKC	J-K Flip-Flop with Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FJKCE	J-K Flip-Flop with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FJKCP	J-K Flip-Flop with Asynchronous Clear and Preset	No	No	No	No	Primitive	Primitive	Primitive
FJKCPE	J-K Flip-Flop with Asynchronous Clear and Preset and Clock Enable	No	No	No	No	Primitive	Primitive	Primitive
FJKP	J-K Flip-Flop with Asynchronous Preset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FJKPE	J-K Flip-Flop with Clock Enable and Asynchronous Preset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FJKRSE	J-K Flip-Flop with Clock Enable and Synchronous Reset and Set	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FJKSRE	J-K Flip-Flop with Clock Enable and Synchronous Set and Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTC	Toggle Flip-Flop with Toggle Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTCE	Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTCLE	Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTCLEX	Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTCP	Toggle Flip-Flop with Toggle Enable and Asynchronous Clear and Preset	No	No	No	No	Primitive	Primitive	Primitive
FTCPE	Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset	No	No	No	No	Primitive	Primitive	Primitive
FTCPLE	Loadable Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset	No	No	No	No	Primitive	Primitive	Primitive
FTDCE	Dual Edge Triggered Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
FTDCLE	Dual Edge Triggered Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
FTDCLEX	Dual Edge Triggered Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
FTDCP	Toggle Flip-Flop with Toggle Enable and Asynchronous Clear and Preset	No	No	No	No	Primitive	Primitive	Primitive
FTDRSE	Dual Edge Triggered Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set	No	No	No	No	No	No	Primitive
FTDRSLE	Dual Edge Triggered Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTP	Toggle Flip-Flop with Toggle Enable and Asynchronous Preset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTPE	Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Preset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTPLE	Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Preset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTRSE	Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTRSLE	Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTSRE	Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
FTSRLE	Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive

General

General elements include FPGA configuration functions, oscillators, boundary scan logic, and other functions not classified in other sections.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
BSCAN_SPARTAN2	Spartan-II Boundary Scan Logic Control Circuit	Primitive[a]	No	No	No	No	No	No
BSCAN_SPARTAN3	Spartan-3 Boundary Scan Logic Control Circuit	No	Primitive	No	No	No	No	No
BSCAN_VIRTEX	Virtex Boundary Scan Logic Control Circuit	Primitive[b]	No	Primitive	No	No	No	No
BSCAN_VIRTEX2	Virtex2 Boundary Scan Logic Control Circuit	No	No	No	Primitive	No	No	No
CAPTURE_SPARTAN2	Spartan-II Register State Capture for Bitstream Readback	Primitive	No	No	No	No	No	No
CAPTURE_SPARTAN3	Spartan-3 Register State Capture for Bitstream Readback	No	Primitive	No	No	No	No	No
CAPTURE_VIRTEX	Virtex Register State Capture for Bitstream Readback	No	No	Primitive	No	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
CAPTURE_VIRTEX2	Virtex-II Register State Capture for Bitstream Readback	No	No	No	Primitive	No	No	No
CLK_DIV2	Global Clock Divider	No	No	No	No	No	No	Primitive
CLK_DIV4	Global Clock Divider	No	No	No	No	No	No	Primitive
CLK_DIV6	Global Clock Divider	No	No	No	No	No	No	Primitive
CLK_DIV8	Global Clock Divider	No	No	No	No	No	No	Primitive
CLK_DIV10	Global Clock Divider	No	No	No	No	No	No	Primitive
CLK_DIV12	Global Clock Divider	No	No	No	No	No	No	Primitive
CLK_DIV14	Global Clock Divider	No	No	No	No	No	No	Primitive
CLK_DIV16	Global Clock Divider	No	No	No	No	No	No	Primitive
CLK_DIV2R	Global Clock Divider with Synchronous Reset	No	No	No	No	No	No	Primitive
CLK_DIV4R	Global Clock Divider with Synchronous Reset	No	No	No	No	No	No	Primitive
CLK_DIV6R	Global Clock Divider with Synchronous Reset	No	No	No	No	No	No	Primitive
CLK_DIV8R	Global Clock Divider with Synchronous Reset	No	No	No	No	No	No	Primitive
CLK_DIV10R	Global Clock Divider with Synchronous Reset	No	No	No	No	No	No	Primitive
CLK_DIV12R	Global Clock Divider with Synchronous Reset	No	No	No	No	No	No	Primitive
CLK_DIV14R	Global Clock Divider with Synchronous Reset	No	No	No	No	No	No	Primitive
CLK_DIV16R	Global Clock Divider with Synchronous Reset	No	No	No	No	No	No	Primitive
CLK_DIV2RSD	Global Clock Divider with Synchronous Reset and Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV4RSD	Global Clock Divider with Synchronous Reset and Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV6RSD	Global Clock Divider with Synchronous Reset and Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV8RSD	Global Clock Divider with Synchronous Reset and Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV10RSD	Global Clock Divider with Synchronous Reset and Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV12RSD	Global Clock Divider with Synchronous Reset and Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV14RSD	Global Clock Divider with Synchronous Reset and Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV16RSD	Global Clock Divider with Synchronous Reset and Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV2SD	Global Clock Divider with Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV4SD	Global Clock Divider with Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV6SD	Global Clock Divider with Start Delay	No	No	No	No	No	No	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
CLK_DIV8SD	Global Clock Divider with Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV10SD	Global Clock Divider with Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV12SD	Global Clock Divider with Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV14SD	Global Clock Divider with Start Delay	No	No	No	No	No	No	Primitive
CLK_DIV16SD	Global Clock Divider with Start Delay	No	No	No	No	No	No	Primitive
CLKDLL	Clock Delay Locked Loop	Primitive	No	Primitive	No	No	No	No
CLKDLLE	Clock Delay Locked Loop with Expanded Output	Primitive[c]	No	Primitive[d]	No	No	No	No
CLKDLLHF	High Frequency Clock Delay Locked Loop	Primitive	No	Primitive[e]	No	No	No	No
DCM	Digital Clock Manager	No	Primitive	No	Primitive	No	No	No
GND	Ground-Connection Signal Tag	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
ICAP_VIRTEX2	User Interface to Virtex-II Internal Configuration Access Port	No	No	No	Primitive	No	No	No
JTAGPPC	JTAG Primitive for the Power PC	No	No	No	Primitive[f]	No	No	No
KEEPER	KEEPER Symbol	Primitive	Primitive	Primitive	Primitive	Primitive[g]	No	Primitive
LUT1	1-Bit Look-Up Table with General Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT2	2-Bit Look-Up Table with General Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT3	3-Bit Look-Up Table with General Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT4	4-Bit Look-Up Table with General Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT1_D	1-Bit Look-Up Table with Dual Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT2_D	2-Bit Look-Up Table with Dual Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT3_D	3-Bit Look-Up Table with Dual Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT4_D	4-Bit Look-Up Table with Dual Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT1_L	1-Bit Look-Up Table with Local Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT2_L	2-Bit Look-Up Table with Local Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT3_L	3-Bit Look-Up Table with Local Output	Primitive	Primitive	Primitive	Primitive	No	No	No
LUT4_L	4-Bit Look-Up Table with Local Output	Primitive	Primitive	Primitive	Primitive	No	No	No
PPC405	Primitive for the Power PC Core	No	No	No	Primitive[h]	No	No	No
PULLDOWN	Resistor to GND for Input Pads	Primitive	Primitive	Primitive	Primitive	No	No	No
PULLUP	Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs	Primitive	Primitive	Primitive	Primitive	No	Primitive	Primitive
ROC	Reset On Configuration	Primitive	Primitive	Primitive	Primitive	No	No	No
STARTBUF_architecture	VHDL Simulation of FPGA Designs	Primitive	Primitive	Primitive	Primitive	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
STARTUP_SPARTAN2	Spartan-II User Interface to Global Clock, Reset, and 3-State Controls	Primitive[i]	No	No	No	No	No	No
STARTUP_SPARTAN3	Spartan-3 User Interface to Global Clock, Reset, and 3-State Controls	No	Primitive	No	No	No	No	No
STARTUP_VIRTEX	Virtex User Interface to Global Clock, Reset, and 3-State Controls	Primitive[j]	No	Primitive	No	No	No	No
STARTUP_VIRTEX2	Virtex-II User Interface to Global Clock, Reset, and 3-State Controls	No	No	No	Primitive	No	No	No
TOC	Three-State On Configuration	Primitive	Primitive	Primitive	Primitive	No	No	No
TOCBUF	Three-State On Configuration Buffer	Primitive	Primitive	Primitive	Primitive	No	No	No
VCC	VCC-Connection Signal Tag	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

a.Primitive is supported for Spartan-II, but not for Spartan-IIE, which is supported by BSCAN_VIRTEX

b.Primitive is supported for Spartan-IIE, but not for Spartan-II, which is supported by BSCAN_SPARTAN2.

c. Supported for Spartan-IIE and Virtex-E devices only.

d. Supported for Spartan-IIE and Virtex-E devices only.

e.For Virtex E, use CLKDLLHF in HF mode. In LF mode, both the separate CLKDLLE and CLKDLL primitive can be used.

f.Supported for Virtex-II Pro and Virtex-II Pro X only.

g.Supported for only XC9500XL and XC9500XV.

h.Not supported for Virtex-II. Supported for Virtex-II Pro and Virtex-II Pro X only.

i.The Primitive in the field marked Spartan IIE is supported only for Spartan-II but not for Spartan-IIE, the latter of which is supported by STARTUP_VIRTEX.

j.The Primitive in the Spartan IIE field is supported for Spartan-IIE, but not for Spartan-II, which is supported by STARTUP_SPARTAN2.

Input Latches

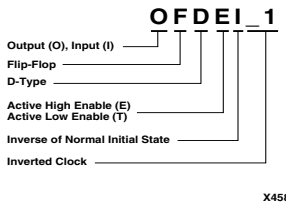
Single and multiple input latches can hold transient data entering a chip. Input latches use the same naming convention as I/O flip-flops.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
ILD	Transparent Input Data Latch	Macro	Macro	Macro	Macro	No	No	No
ILD4	Transparent Input Data Latch	Macro	Macro	Macro	Macro	No	Nob	No
ILD8	Transparent Input Data Latch	Macro	Macro	Macro	Macro	No	No	No
ILD16	Transparent Input Data Latch	Macro	Macro	Macro	Macro	No	No	No
ILD_1	Transparent Input Data Latch with Inverted Gate	Macro	Macro	Macro	Macro	No	No	No
ILDI	Transparent Input Data Latch (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No
ILDI_1	Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No
ILDX	Transparent Input Data Latch	Macro	Macro	Macro	Macro	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
ILDX4	Transparent Input Data Latch	Macro	Macro	Macro	Macro	No	No	No
ILDX8	Transparent Input Data Latch	Macro	Macro	Macro	Macro	No	No	No
ILDX16	Transparent Input Data Latch	Macro	Macro	Macro	Macro	No	No	No
ILDX_1	Transparent Input Data Latch with Inverted Gate	Macro	Macro	Macro	Macro	No	No	No
ILDXI	Transparent Input Data Latch (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No
ILDXI_1	Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No

Input/Output Flip-Flops

Input/Output flip-flops are configured in IOBs. They include flip-flops whose outputs are enabled by 3-state buffers, flip-flops that can be set upon global set/reset rather than reset, and flip-flops with inverted clock inputs. The naming convention specifies each flip-flop function and is illustrated in the following figure.



Input/Output Flip-Flop Naming Convention

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
IFD	Single- and Multiple-Input D Flip-Flop	Macro	Macro	Macro	Macro	No	No	No
IFD_1	Input D Flip-Flop with Inverted Clock	Macro	Macro	Macro	Macro	No	No	No
IFD4	Single- and Multiple-Input D Flip-Flop	Macro	Macro	Macro	Macro	No	No	No
IFD8	Single- and Multiple-Input D Flip-Flop	Macro	Macro	Macro	Macro	No	No	No
IFD16	Single- and Multiple-Input D Flip-Flop	Macro	Macro	Macro	Macro	No	No	No
IFDDRCPE	Dual Data Rate Input D Flip-Flop with Clock Enable and Asynchronous Preset and Clear	No	Primitive	No	Primitive	No	No	No
IFDDRRSE	Dual Data Rate Input D Flip-Flop with Synchronous Reset and Set and Clock Enable	No	Primitive	No	Primitive	No	No	No
IFDI	Input D Flip-Flop (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No
IFDI_1	Input D Flip-Flop with Inverted Clock (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
IFDX	Single- and Multiple-Input D Flip-Flop with Clock Enable	Macro	Macro	Macro	Macro	No	No	No
IFDX_1	Input D Flip-Flop with Inverted Clock and Clock Enable	Macro	Macro	Macro	Macro	No	No	No
IFDX4	Single- and Multiple-Input D Flip-Flop with Clock Enable	Macro	Macro	Macro	Macro	No	No	No
IFDX8	Single- and Multiple-Input D Flip-Flop with Clock Enable	Macro	Macro	Macro	Macro	No	No	No
IFDX16	Single- and Multiple-Input D Flip-Flops with Clock Enable	Macro	Macro	Macro	Macro	No	No	No
IFDXI	Input D Flip-Flop with Clock Enable (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No
ILDXI_1	Input D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No
OFD	Single- and Multiple-Output D Flip-Flops	Macro	Macro	Macro	Macro	No	No	No
OFD4	Single- and Multiple-Output D Flip-Flops	Macro	Macro	Macro	Macro	No	No	No
OFD8	Single- and Multiple-Output D Flip-Flops	Macro	Macro	Macro	Macro	No	No	No
OFD16	Single- and Multiple-Output D Flip-Flops	Macro	Macro	Macro	Macro	No	No	No
OFD_1	Output D Flip-Flop with Inverted Clock	Macro	Macro	Macro	Macro	No	No	No
OFDDRCPE	Dual Data Rate Output D Flip-Flop with Clock Enable and Asynchronous Preset and Clear	No	Primitive	No	Primitive	No	No	No
OFDDRRSE	Dual Data Rate Output D Flip-Flop with Synchronous Reset and Set and Clock Enable	No	Primitive	No	Primitive	No	No	No
OFDDRTCPE	Dual Data Rate D Flip-Flop with Active-Low 3--State Output Buffer, Clock Enable, and Asynchro-nous Preset and Clear	No	Primitive	No	Primitive	No	No	No
OFDDRTRSE	Dual Data Rate D Flip-Flop with Active -Low 3-State Output Buffer, Synchronous Reset and Set, and Clock Enable	No	Primitive	No	Primitive	No	No	No
OFDE	D Flip-Flop with Active-High Enable Output Buffers	Macro	Macro	Macro	Macro	No	No	No
OFDE4	D Flip-Flop with Active-High Enable Output Buffers	Macro	Macro	Macro	Macro	No	No	No
OFDE8	D Flip-Flop with Active-High Enable Output Buffers	Macro	Macro	Macro	Macro	No	No	No
OFDE16	D Flip-Flop with Active-High Enable Output Buffers	Macro	Macro	Macro	Macro	No	No	No
OFDE_1	D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock	Macro	Macro	Macro	Macro	No	No	No
OFDI	Output D Flip-Flop (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
OFDI_1	Output D Flip-Flop with Inverted Clock (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No
OFDT	Single and Multiple D Flip-Flop with Active-Low 3-State Output Buffers	Macro	Macro	Macro	Macro	No	No	No
OFDT4	Single and Multiple D Flip-Flop with Active-Low 3-State Output Buffers	Macro	Macro	Macro	Macro	No	No	No
OFDT8	Single and Multiple D Flip-Flop with Active-Low 3-State Output Buffers	Macro	Macro	Macro	Macro	No	No	No
OFDT16	Single and Multiple D Flip-Flop with Active-Low 3-State Output Buffers	Macro	Macro	Macro	Macro	No	No	No
OFDT_1	D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock	Macro	Macro	Macro	Macro	No	No	No
OFDX	Single- and Multiple-Output D Flip-Flop with Clock Enable	Macro	Macro	Macro	Macro	No	No	No
OFDX4	Single- and Multiple-Output D Flip-Flop with Clock Enable	Macro	Macro	Macro	Macro	No	No	No
OFDX8	Single- and Multiple-Output D Flip-Flop with Clock Enable	Macro	Macro	Macro	Macro	No	No	No
OFDX16	Single- and Multiple-Output D Flip-Flop with Clock Enable	Macro	Macro	Macro	Macro	No	No	No
OFDX_1	Output D Flip-Flop with Inverted Clock and Clock Enable	Macro	Macro	Macro	Macro	No	No	No
OFDXI	Output D Flip-Flop with Clock Enable (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No
OFDXI_1	Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)	Macro	Macro	Macro	Macro	No	No	No

Input/Output Functions

Input/Output Block (IOB) resources are configured into various I/O primitives and macros for convenience, such as output buffers (s) and output buffers with an enable (OBUFEs). Pads used to connect the circuit to PLD device pins are also included.

Virtex, Virtex-E, Spartan-II, Spartan-IIE, Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X have multiple variants (Primitives) to choose from for each SelectIO buffer. The I/O interface for each variant corresponds to a specific I/O standard, and those standards are detailed in Xilinx hardware documentation.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
GT_AURORA_n	Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT_CUSTOM	Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT_ETHERNET_n	Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
GT_FIBRE_CHAN_n	Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT_INFINIBAND_n	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT_XAUI_n	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT10_10GE_n	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT10_10GFC_n	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT10_AURORA_n	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT10_AURORAX_n	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT10_CUSTOM	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT10_OC48_n	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT10_OC192_n	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
GT10_PCI_EXPRESS_n	10-Gigabit Transceiver for High-Speed I/O	No	No	No	Primitive	No	No	No
IBUF	Single- and Multiple-Input Buffer	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IBUF4	Single- and Multiple-Input Buffer	Macro	No	Macro	Macro	Primitive	Primitive	Primitive
IBUF8	Single- and Multiple-Input Buffer	Macro	No	Macro	Macro	Primitive	Primitive	Primitive
IBUF16	Single- and Multiple-Input Buffer	Macro	No	Macro	Macro	Primitive	Primitive	Primitive
IBUFDS	Differential Signaling Input Buffer with Selectable I/O Interface	No	Primitive	No	Primitive	No	No	No
IBUFG	Dedicated Input Buffer with Selectable I/O Interface	Primitive	Primitive	Primitive	Primitive	No	No	No
IBUFGDS	Dedicated Differential Signaling Input Buffer with Selectable I/O Interface	No	Primitive	No	Primitive	No	No	No
IOBUF	Bi-Directional Buffer with Selectable I/0 Interface (multiple primitives)	Primitive	Primitive	Primitive	Primitive	No	No	No
IOBUFDS	3-State Differential Signaling I/O Buffer with Active Low Output Enable	No	Primitive	No	Primitive	No	No	No
IOPAD	Single- and Multiple-Input/Output Pad	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IOPAD4	Single- and Multiple-Input/Output Pad	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
IOPAD8	Single- and Multiple-Input/Output Pad	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
IOPAD16	Single- and Multiple-Input/Output Pad	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
IPAD	Single- and Multiple-Input Pad	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IPAD4	Single- and Multiple-Input Pad	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
IPAD8	Single- and Multiple-Input Pad	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
IPAD16	Single- and Multiple-Input Pad	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OBUF	Single- and Multiple-Output Buffer	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OBUF4	Single- and Multiple-Output Buffer	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OBUF8	Single- and Multiple-Output Buffer	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OBUF16	Single- and Multiple-Output Buffer	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OBUFDS	Differential Signaling Output Buffer with Selectable I/O Interface	No	Primitive	No	Primitive	No	No	No
OBUFE	3-State Output Buffers with Active-High Output Enable	Macro	No	Macro	Macro	Primitive	Primitive	Primitive
OBUFE4	3-State Output Buffers with Active-High Output Enable	Macro	No	Macro	Macro	Primitive	Primitive	Primitive
OBUFE8	3-State Output Buffers with Active-High Output Enable	Macro	No	Macro	Macro	Primitive	Primitive	Primitive
OBUFE16	3-State Output Buffers with Active-High Output Enable	Macro	No	Macro	Macro	Primitive	Primitive	Primitive
OBUFT	Single and Multiple 3-State Output Buffer with Active Low Output Enable	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OBUFT4	Single and Multiple 3-State Output Buffer with Active Low Output Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OBUFT8	Single and Multiple 3-State Output Buffer with Active Low Output Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OBUFT16	Single and Multiple 3-State Output Buffer with Active Low Output Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OBUFTDS	3-State Output Buffer with Differential Signaling, Active-Low Output Enable, and Selectable I/O Interface	No	Primitive	No	Primitive	No	No	No
OPAD	Single- and Multiple-Output Pad	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OPAD4	Multiple-Output Pad	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OPAD8	Multiple-Output Pad	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OPAD16	Multiple-Output Pad	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
UPAD	Connects the I/O Node of an IOB to the Internal PLD Circuit	Primitive	Primitive	Primitive	Primitive	No	No	No

Latches

Latches (LD) are available for all architectures.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
LD	Transparent Data Latch	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
LD_1	Transparent Data Latch with Inverted Gate	Primitive	Primitive	Primitive	Primitive	No	No	No
LD4	Multiple Transparent Data Latch	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
LD8	Multiple Transparent Data Latch	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
LD16	Multiple Transparent Data Latch	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
LDC	Transparent Data Latch with Asynchronous Clear	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
LDC_1	Transparent Data Latch with Asynchronous Clear and Inverted Gate	Primitive	Primitive	Primitive	Primitive	No	No	No
LD4CE	Transparent Data Latch with Asynchronous Clear and Gate Enable	Macro	Macro	Macro	Macro	No	No	No
LD8CE	Transparent Data Latch with Asynchronous Clear and Gate Enable	Macro	Macro	Macro	Macro	No	No	No
LD16CE	Transparent Data Latch with Asynchronous Clear and Gate Enable	Macro	Macro	Macro	Macro	No	No	No
LDCE	Transparent Data Latch with Asynchronous Clear and Gate Enable	Primitive	Primitive	Primitive	Primitive	No	No	No
LDCE_1	Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate	Primitive	Primitive	Primitive	Primitive	No	No	No
LDCP	Transparent Data Latch with Asynchronous Clear and Preset	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
LDCP_1	Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate	Primitive	Primitive	Primitive	Primitive	No	No	No
LDCPE	Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable	Primitive	Primitive	Primitive	Primitive	No	No	No
LDCPE_1	Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate	Primitive	Primitive	Primitive	Primitive	No	No	No
LDE	Transparent Data Latch with Gate Enable	Primitive	Primitive	Primitive	Primitive	No	No	No
LDE_1	Transparent Data Latch with Gate Enable and Inverted Gate	Primitive	Primitive	Primitive	Primitive	No	No	No
LDG	Transparent Datagate Latch	No	No	No	No	No	No	Primitive
LDG4	Multiple Transparent Datagate Latch	No	No	No	No	No	No	Primitive
LDG8	Multiple Transparent Datagate Latch	No	No	No	No	No	No	Primitive
LDG16	Multiple Transparent Datagate Latch	No	No	No	No	No	No	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
LDP	Transparent Data Latch with Asynchronous Preset	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
LDP_1	Transparent Data Latch with Asynchronous Preset and Inverted Gate	Primitive	Primitive	Primitive	Primitive	No	No	No
LDPE	Transparent Data Latch with Asynchronous Preset and Gate Enable	Primitive	Primitive	Primitive	Primitive	No	No	No
LDPE_1	Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate	Primitive	Primitive	Primitive	Primitive	No	No	No

Logic Primitives

Combinatorial logic gates that implement the basic Boolean functions are available in all architectures with up to five inputs in all combinations of inverted and non-inverted inputs, and with six to nine inputs non-inverted.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
AND2	2-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND2B1	2-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND2B2	2-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND3	3-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND3B1	3-Input AND Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
AND3B2	3-Input AND Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
AND3B3	3-Input AND Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
AND4	4-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND4B1	4-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND4B2	4-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND4B3	4-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND4B4	4-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND5	5-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
AND5B1	5-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND5B2	5-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND5B3	5-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND5B4	5-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND5B5	5-Input AND Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND6	6-Input AND Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
AND7	7-Input AND Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
AND8	8-Input AND Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
AND9	9-Input AND Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
AND12	12- Input AND Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	No	No	No
AND16	16- Input AND Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	No	No	No
INV	Single and Multiple Inverters	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
INV4	Single and Multiple Inverters	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
INV8	Single and Multiple Inverters	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
INV16	Single and Multiple Inverters	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
MULT_AND	Fast Multiplier AND	Primitive	Primitive	Primitive	Primitive	No	No	No
NAND2	2-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND2B1	2-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND2B2	2-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND3	3-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND3B1	3-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND3B2	3-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND3B3	3-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND4	4-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
NAND4B1	4-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND4B2	4-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND4B3	4-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND4B4	4-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND5	5-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND5B1	5-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND5B2	5-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND5B3	5-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND5B4	5-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND5B5	5-Input NAND Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND6	6-Input NAND Gate with Inverted and Non-Inverted Inputs.	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
NAND7	7-Input NAND Gate with Inverted and Non-Inverted Inputs.	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
NAND8	8-Input NAND Gate with Inverted and Non-Inverted Inputs.	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
NAND9	9-Input NAND Gate with Inverted and Non-Inverted Inputs.	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
NAND12	12- Input NAND Gate with Non-Inverted Inputs.	Macro	Macro	Macro	Macro	No	No	No
NAND16	16- Input NAND Gate with Non-Inverted Inputs.	Macro	Macro	Macro	Macro	No	No	No
NOR2	2- Input NOR Gate with Inverted and Non-Inverted Inputs.	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR2B1	2- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR2B2	2- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR3	3- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR3B1	3- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
NOR3B2	3- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR3B3	3- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR4	4- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR4B1	4- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR4B2	4- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR4B3	4- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR4B4	4- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR5	5- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR5B1	5- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR5B2	5- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR5B3	5- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR5B4	5- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR5B5	5- Input NOR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR6	6- Input NOR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
NOR7	7- Input NOR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
NOR8	8- Input NOR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
NOR9	9- Input NOR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
NOR12	12-Input NOR Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	No	No	No
NOR16	16-Input NOR Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	No	No	No
OR2	2-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR2B1	2-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
OR2B2	2-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR3	3-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR3B1	3-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR3B2	3-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR3B3	3Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR4	4-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR4B1	4-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR4B2	4-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR4B3	4-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR5B1	5-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR5B2	12-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR5B3	5-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR5B4	5-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR5B5	5-Input OR Gate with Inverted and Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR6	6-Input OR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OR7	6-Input OR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OR8	8-Input OR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OR9	9-Input OR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
OR12	12-Input OR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	No	No	No
OR16	16-Input OR Gate with Inverted and Non-Inverted Inputs	Macro	Macro	Macro	Macro	No	No	No
ORCY	OR with Carry Logic	No	No	No	Primitive	No	No	No
SOP3	Sum of Products	Macro	Macro	Macro	Macro	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
SOP3B1A	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP3B1B	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP3B2A	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP3B2B	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP3B3	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP4	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP4B3	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP4B4	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP4B1	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP4B2A	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
SOP4B2B	Sum of Products	Macro	Macro	Macro	Macro	No	No	No
XNOR2	2-Input XNOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XNOR3	3-Input XNOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XNOR4	4-Input XNOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XNOR5	5-Input XNOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XNOR6	6-Input XNOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XNOR7	7-Input XNOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XNOR8	8-Input XNOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XNOR9	9-Input XNOR Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
XOR2	2-Input XOR Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
XOR3	3-Input XOR Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
XOR4	4-Input XOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XOR5	5-Input XOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XOR6	6-Input XOR Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
XOR7	7-Input XOR Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
XOR8	8-Input XOR Gate with Non-Inverted Inputs	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
XOR9	9-Input XOR Gate with Non-Inverted Inputs	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
XORCY	XOR for Carry Logic with General Output	Primitive	Primitive	Primitive	Primitive	No	No	No
XORCY_D	XOR for Carry Logic with Dual Output	Primitive	Primitive	Primitive	Primitive	No	No	No
XORCY_L	XOR for Carry Logic with Local Output	Primitive	Primitive	Primitive	Primitive	No	No	No

Map Elements

Map elements are used in conjunction with logic symbols to constrain the logic to particular CLBs or particular F function generators.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
FMAP	F Function Generator Partitioning Control Symbol	Primitive	Primitive	Primitive	Primitive	No	No	No

Memory Elements

In the Virtex, Virtex-E, Spartan-II, and Spartan-IIE, Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X architectures, a number of static RAMs are defined as primitives. These 16- or 32-word RAMs are 1, 2, 4, and 8 bits wide.

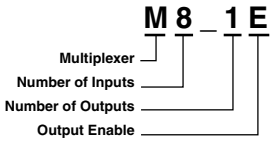
The Virtex, Virtex-E, Spartan-II, and Spartan-IIE, Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X architectures have dedicated blocks of on-chip 4096-bit single-port and dual-port synchronous RAM. Each port is configured to a specific data width. There are five single-port block RAM primitives and 30 dual-port block RAM primitives.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
RAM16X1D	16-Deep by 1-Wide Static Dual Port Synchronous RAM	Primitive	Primitive	Primitive	Primitive	No	No	No
RAM16X1D_1	16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock	Primitive	Primitive	Primitive	Primitive	No	No	No
RAM16X1S	16-Deep by 1-Wide Static Synchronous RAM	Primitive	Primitive	Primitive	Primitive	No	No	No
RAM16X1S_1	16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock	Primitive	Primitive	Primitive	Primitive	No	No	No
RAM16X2D	16-Deep by 2-Wide Static Dual Port Synchronous RAM	Macro	No	Macro	Macro	No	No	No
RAM16X2S	16-Deep by 2-Wide Static Synchronous RAM	Macro	Primitive	Macro	Primitive	No	No	No
RAM16X4D	16-Deep by 4-Wide Static Dual Port Synchronous RAM	Macro	No	Macro	Macro	No	No	No
RAM16X4S	16-Deep by 4-Wide Static Synchronous RAM	Macro	Primitive	Macro	Primitive	No	No	No
RAM16X8D	16-Deep by 8-Wide Static Dual Port Synchronous RAM	Macro	No	Macro	Macro	No	No	No
RAM16X8S	16-Deep by 8-Wide Static Synchronous RAM	Macro	No	Macro	Primitive	No	No	No
RAM32X1D	32-Deep by 1-Wide Static Dual Static Port Synchronous RAM	No	No	No	Primitive	No	No	No
RAM32X1D_1	32-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock	No	No	No	Primitive	No	No	No
RAM32X1S	32-Deep by 1-Wide Static Synchronous RAM	Primitive	Primitive	Primitive	Primitive	No	No	No
RAM32X1S_1	32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock	Primitive	Primitive	Primitive	Primitive	No	No	No
RAM32X2S	32-Deep by 2-Wide Static Synchronous RAM	Macro	Primitive	Macro	Primitive	No	No	No
RAM32X4S	32-Deep by 4-Wide Static Synchronous RAM	Macro	No	Macro	Primitive	No	No	No

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
RAM32X8S	32-Deep by 8-Wide Static Synchronous RAM	Macro	No	Macro	Primitive	No	No	No
RAM64X1D	64-Deep by 1-Wide Dual Port Static Synchronous RAM	No	No	No	Primitive	No	No	No
RAM64X1D_1	64-Deep by 1-Wide Dual Port Static Synchronous RAM with Negative-Edge Clock	No	No	No	Primitive	No	No	No
RAM64X1S	64-Deep by 1-Wide Static Synchronous RAM	No	Primitive	No	Primitive	No	No	No
RAM64X1S_1	64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock	No	Primitive	No	Primitive	No	No	No
RAM64X2S	64-Deep by 2-Wide Static Synchronous RAM	No	No	No	Primitive	No	No	No
RAM128X1S	128-Deep by 1-Wide Static Synchronous RAM	No	No	No	Primitive	No	No	No
RAM128X1S_1	128-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock	No	No	No	Primitive	No	No	No
RAMB4_Sm_Sn	4096-Bit Dual-Port Synchronous Block RAM with Port Width (m or n) Configured to 1, 2, 4, 8, or 16 Bits	Primitive	No	Primitive	No	No	No	No
RAMB4_Sn	4096-Bit Single-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 8, or 16 Bits	Primitive	No	Primitive	No	No	No	No
RAMB16_Sm_Sn	16384-Bit Data Memory and 2048-Bit Parity Memory, Dual-Port Synchronous Block RAM with Port Width (m or n) Configured to 1, 2, 4, 9, 18, or 36 Bits	No	Primitive	No	Primitive	No	No	No
RAMB16_Sn	16384-Bit Data Memory and 2048-Bit Parity Memory, Single-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 9, 18, or 36 Bits	No	Primitive	No	Primitive	No	No	No
ROC	Reset On Configuration	Primitive	Primitive	Primitive	Primitive	No	No	No
ROCBUF	Reset On Configuration Buffer	Primitive	Primitive	Primitive	Primitive	No	No	No
ROM16X1	16-Deep by 1-Wide ROM	Primitive	Primitive	Primitive	Primitive	No	No	No
ROM32X1	32-Deep by 1-Wide ROM	Primitive	Primitive	Primitive	Primitive	No	No	No
ROM64X1	64-Deep by 1-Wide ROM	No	Primitive	No	Primitive	No	No	No
ROM128X1	128-Deep by 1-Wide ROM	No	Primitive	No	Primitive	No	No	No
ROM256X1	256-Deep by 1-Wide ROM	No	Primitive	No	Primitive	No	No	No

Multiplexers

The multiplexer naming convention shown in the following figure indicates the number of inputs and outputs and whether or not an enable is available.



Multiplexer Naming Convention

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
M2_1	2-to-1 Multiplexer	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
M2_1B1	2-to-1 Multiplexer with D0 Inverted	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
M2_1B2	2-to-1 Multiplexer with D0 and D1 Inverted	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
M2_1E	2-to-1 Multiplexer with Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
M4_1E	4-to-1 Multiplexer with Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
M8_1E	8-to-1 Multiplexer with Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
M16_1E	16-to-1 Multiplexer with Enable	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
MUXCY	2-to-1 Multiplexer for Carry Logic with General Output	Primitive	Primitive	Primitive	Primitive	No	No	No
MUXCY_D	2-to-1 Multiplexer for Carry Logic with Dual Output	Primitive	Primitive	Primitive	Primitive	No	No	No
MUXCY_L	2-to-1 Multiplexer for Carry Logic with Local Output	Primitive	Primitive	Primitive	Primitive	No	No	No
MUXF5	2-to-1 Lookup Table Multiplexer with General Output	Primitive	Primitive	Primitive	Primitive	No	No	No
MUXF5_D	2-to-1 Lookup Table Multiplexer with Dual Output	Primitive	Primitive	Primitive	Primitive	No	No	No
MUXF5_L	2-to-1 Lookup Table Multiplexer with Local Output	Primitive	Primitive	Primitive	Primitive	No	No	No
MUXF6	2-to-1 Lookup Table Multiplexer with General Output	Primitive	Primitive	Primitive	Primitive	No	No	No
MUXF6_D	2-to-1 Lookup Table Multiplexer with Dual Output	Primitive	Primitive	Primitive	Primitive	No	No	No
MUXF6_L	2-to-1 Lookup Table Multiplexer with Local Output	Primitive	Primitive	Primitive	Primitive	No	No	No
MUXF7	2-to-1 Lookup Table Multiplexer with General Output	No	Primitive	No	Primitive	No	No	No
MUXF7_D	2-to-1 Lookup Table Multiplexer with Dual Output	No	Primitive	No	Primitive	No	No	No
MUXF7_L	2-to-1 Lookup Table Multiplexer with Local Output	No	Primitive	No	Primitive	No	No	No
MUXF8	2-to-1 Lookup Table Multiplexer with General Output	No	Primitive	No	Primitive	No	No	No
MUXF8_D	2-to-1 Lookup Table Multiplexer with Dual Output	No	Primitive	No	Primitive	No	No	No
MUXF8_L	2-to-1 Lookup Table Multiplexer with Local Output	No	Primitive	No	Primitive	No	No	No

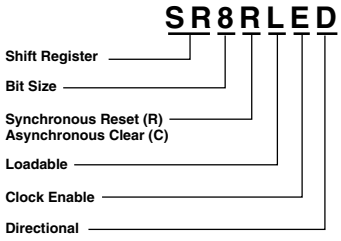
Shifters

Shifters are barrel shifters (BRLSHFT) of four and eight bits.

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
BRLSHFT4	4-Bit Barrel Shifter	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
BRLSHFT8	8-Bit Barrel Shifter	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive

Shift Registers

Shift registers are available in a variety of sizes and capabilities. The naming convention shown in the following figure illustrates available features.



Shift Register Naming Convention

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
SR4CE	4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR8CE	8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR16CE	16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR4CLE	4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR8CLE	8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR16CLE	16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR4CLED	4-Bit Shift Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR8CLED	8-Bit Shift Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR16CLED	16-Bit Shift Register with Clock Enable and Asynchronous Clear	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR4RE	4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
SR8RE	8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR16RE	16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR4RLE	4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR8RLE	8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR16RLE	16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR4RLED	4-Bit Shift Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR8RLED	8-Bit Shift Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SR16RLED	16-Bit Shift Register with Clock Enable and Synchronous Reset	Macro	Macro	Macro	Macro	Primitive	Primitive	Primitive
SRD4CE	4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
SRD8CE	8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
SRD16CE	16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
SRD4CLE	4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
SRD8CLE	8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
SRD16CLE	16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
SRD4CLED	4-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
SRD8CLED	8-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
SRD16CLED	16-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear	No	No	No	No	No	No	Primitive
SRD4RE	4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive

Design Element	Description	Spartan-II, IIE	Spartan-3	Virtex, E	Virtex II, Pro, Pro X	XC9500/XV/XL	CR XPLA3	CR-II
SRD8RE	8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
SRD16RE	16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
SRD4RLE	4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
SRD8RLE	8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
SRD16RLE	16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
SRD4RLED	4-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
SRD8RLED	8-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
SRD16RLED	16-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset	No	No	No	No	No	No	Primitive
SRL16	16-Bit Shift Register Look-Up Table (LUT)	Primitive	Primitive	Primitive	Primitive	No	No	No
SRL16_1	16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock	Primitive	Primitive	Primitive	Primitive	No	No	No
SRL16E	16-Bit Shift Register Look-Up Table (LUT) with Clock Enable	Primitive	Primitive	Primitive	Primitive	No	No	No
SRL16E_1	16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock and Clock Enable	Primitive	Primitive	Primitive	Primitive	No	No	No
SRLC16	16-Bit Shift Register Look-Up Table (LUT) with Carry	No	Primitive	No	Primitive	No	No	No
SRLC16_1	16-Bit Shift Register Look-Up Table (LUT) with Carry and Negative-Edge Clock	No	Primitive	No	Primitive	No	No	No
SRLC16E	16-Bit Shift Register Look-Up Table (LUT) with Carry and Clock Enable	No	Primitive	No	Primitive	No	No	No
SRLC16E_1	16-Bit Shift Register Look-Up Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable	No	Primitive	No	Primitive	No	No	No