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AN ORDINARY OP AMP CAN PROVIDE WIDE VOLTAGE SWINGS, BUT YOU MUST CONSIDER DESIGN ISSUES AND TRADE-OFFS.

Bootstrapping your op amp yields wide voltage swings

Getting 100V p-p from a monolithic op amp is just one example of what you can achieve by bootstrapping power supplies. "Bootstrapping" in this context is simply a method of controlling a device's supply voltages based on its output.

In the circuit of **Figure 1**, the system supply voltages, V_{CC} and V_{EE}, are fixed, but the device supply voltages, V_{CO} and V_{EO}, change dynamically as a function of V_{OUT}. The op amp can then cover peak-to-peak voltage swings far greater than the total voltage you apply across its supply rails.

The maximum voltage that you can apply across a monolithic op amp's supply rails, which the manufacturer's IC process determines, is generally around 30 to 40V. **Figure 2** illustrates some results in which the voltage difference, $V_{CO} - V_{EO}$, remains constant at approximately 30, and the absolute voltages, V_{CO} and V_{EO}, swing more than 70V to follow V_{OUT}. Two emitter followers and two resistor pairs generate V_{CO} and V_{EO} (**Figure 1**). (The two diodes shown are added merely to improve output voltage swing as described in the following circuit analysis.)

WHY BOOTSTRAP?

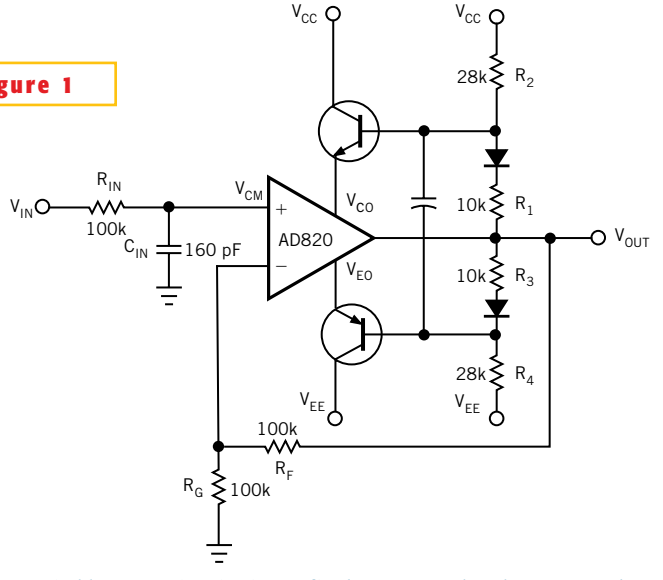
Op amps offer a simple and effective alternative to discrete-transistor designs and have proved their usefulness in a range of applications. However, some applications require output-voltage swings greater than those that a standard monolithic op amp can generate.

The most direct approach to achieving these wide voltage swings is to design the amplifier using discrete transistors. This approach allows you the flexibility to customize the amplifier for the application. You can also easily achieve high output power with this method. However, discrete-transistor designs require more of a designer's time and effort than other approaches and require more parts, complicating manufacturing. It is also difficult to achieve precision in these designs because of device matching and temperature gradients.

High-voltage op-amp modules provide an alternative that considerably eases a designer's task. These devices are just as easy to use as monolithic op amps but are generally in the form of hybrid modules, thereby allowing high-voltage (and often high-power) operation. One strong advantage of these modules over discrete designs is that they have factory-specified performance, relieving the designer's task in characterizing performance. The most significant disadvantage of these hybrid modules is their cost. Also, far more monolithic op amps than hybrid op amps are available. A hybrid often cannot meet the performance demands of a design. In this case, bootstrapping techniques open the list of available devices to many hundreds.

Bootstrapping designs require more effort but are significantly lower cost than high-voltage op-amp modules. An all-discrete design might offer you still lower cost, but the additional design and characterization effort you must make often offsets

Figure 1



A typical bootstrapping circuit uses fixed system-supply voltages, V_{CC} and V_{EE}, but the device-supply voltages, V_{CO} and V_{EO} change as a function of the output voltage.

this cost reduction. A variety of monolithic op amps is available, and each features fully factory-specified performance that you can apply even when a bootstrapping network surrounds the op amp. Extending the voltage range of standard op amps by bootstrapping offers you flexibility and maintains a "canned" set of performance parameters.

For any high-voltage-amplifier design, you should consider all three techniques. This article offers a detailed look at bootstrapping, the least documented method of the three (**Table 1**).

HOW DOES BOOTSTRAPPING WORK?

Ignoring the diode drops and V_{BE} drops for a moment, you can express V_{CO} and V_{EO} in **Figure 1** as:

$$V_{CO} = \frac{V_{CC}R_1 + V_{OUT}R_2}{R_1 + R_2}; \quad (1)$$

$$V_{EO} = \frac{V_{EE}R_3 + V_{OUT}R_4}{R_3 + R_4}. \quad (2)$$

Next, add the effects of transistor V_{BE}, but omit the optional diodes from the circuit, and you get a more realistic representation of the device supply voltages:

$$V_{CO} = \frac{V_{CC}R_1 + V_{OUT}R_2}{R_1 + R_2} - 0.6; \quad (3)$$

$$V_{EO} = \frac{V_{EE}R_3 + V_{OUT}R_4}{R_3 + R_4} + 0.6. \quad (4)$$

In this case, you solve for the maximum output voltage that you can achieve (with an ideal rail-to-rail op amp) by letting $V_{CO}=V_{OUT}$ and solving for V_{OUT}, which yields the following result:

$$\text{MAX } V_{OUT} = V_{CC} - 0.6\left(1 + \frac{R_2}{R_1}\right). \quad (5)$$

By adding diodes to compensate for transistor V_{BE}, the device supply voltages become:

$$V_{CO} = \frac{(V_{CC} - 0.6)R_1 + V_{OUT}R_2}{R_1 + R_2}; \quad (6)$$

$$V_{EO} = \frac{(V_{EE} + 0.6)R_3 + V_{OUT}R_4}{R_3 + R_4}. \quad (7)$$

In this case, the maximum output voltage that you can achieve with an ideal rail-to-rail op amp is:

$$\text{MAX } V_{OUT} = V_{CC} - 0.6. \quad (8)$$

Thus, the peak output voltage increases by $0.6\times(R_2/R_1)$V.

In a symmetrical system (in which ground is equidistant between V_{CC} and V_{EE}), let $R_3=R_1$ and $R_4=R_2$. Making this substitution in **equations 6** and **7**, you can see that the difference between V_{CO} and V_{EO} is constant if you assume that V_{CC} and V_{EE} are constant.

$$V_{CO} - V_{EO} = \frac{R_1}{R_1 + R_2}(V_{CC} - V_{EE} - 1.2). \quad (9)$$

So, for the example in **Figure 2**, where V_{CC}=60V, V_{EE}=−60V, R_1=10 kΩ, and R_2=28 kΩ, the voltage across the op amp remains constant at about 31V throughout the 100V p-p swing of the output.

As with all op-amp applications, you must ensure that the voltage at the noninverting input always remains within the device's common-mode input range. Whereas this task is trivial in standard op-amp circuits with fixed power supplies, it requires more insight for bootstrapping configurations, in which the op-amp supply rails change with the output. Even as V_{CO} and V_{EO} change, V_{IN} must always remain between them (**Figure 2**). You must guarantee this situation by design, or a latched condition might occur. To ensure that your design meets input common-mode range under all conditions, you must address dc conditions, transient conditions, phase reversal, and power-up conditions.

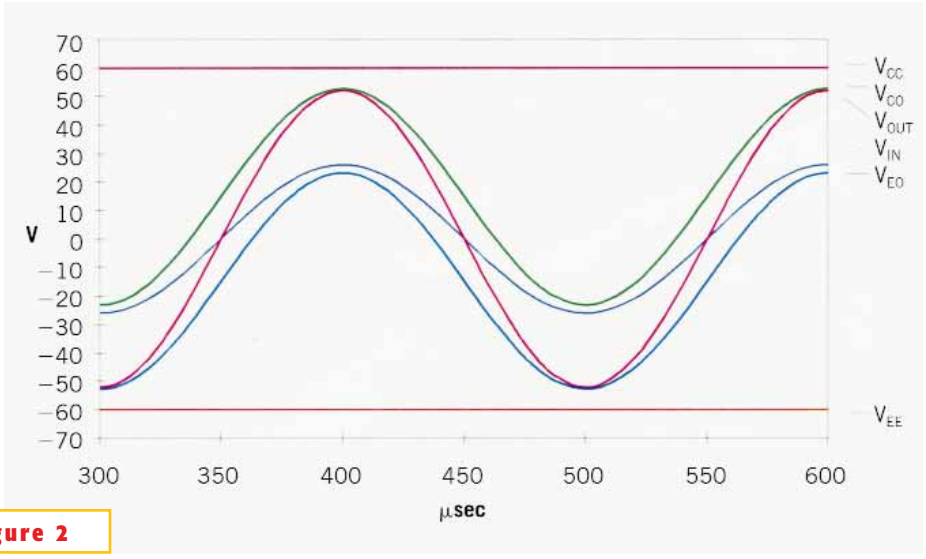


Figure 2

This simulation shows the circuit of Figure 1, providing a 100V p-p sine-wave using an AD820 op amp.

DC CONDITIONS

When considering dc gain, remember that the feedback network of a bootstrapped op-amp circuit works in the same way as that of any other op-amp gain stage. The gain of the **Figure 1** circuit is simply $A_V=V_{OUT}/V_{IN}=1+R_F/R_G$. In configurations in which $V_{CC}-V_{EE}$ is less than twice $V_{CO}-V_{EO}$, you can run the circuit at any gain, including inverting gains. But for wider system supply rails and to achieve wider output swings, you must use a noninverting configuration and carefully select gain. If you set gain too high, you will exceed the op amp's input common-mode range, which will likely result in latch-up of the bootstrap network. A larger gain than that shown

TABLE 1–TECHNIQUES FOR ACHIEVING HIGH-VOLTAGE AMPLIFICATION

	Cost	Design effort	Parts count	Factory specs	Power drive	No. of options
High-voltage op-amp module	Poor	Great	Great	Great	Good	Poor
Bootstrapping with monolithic op amp	Good	Good	Good	Great	Poor	Great
Discrete-transistor monolithic op amp	Great	Poor	Poor	Poor	Great	Great

in **Figure 2** would cause V_{CO} to exceed V_{CM} at its peak and V_{CO} to exceed V_{CM} on the negative side. This situation clearly violates the op amp's input common-mode range in that both power supplies are farther from ground than its input. Luckily, you can easily avoid this condition. With a low enough gain, the output stage saturates before the input stage, and the power-supply rails stop increasing before they exceed the input (**Figure 3**).

Assuming that you have a symmetrical system with positive gain (in which R_G is "grounded" halfway between V_{CC} and V_{EE}, the following two **equations** are sufficient to ensure that you avoid the above condition:

$$A_V \le \frac{V_{CC}-0.6}{V_{CC}-0.6-(V_{CO}-V_{EO})+V_{IHRL}}, \quad (10)$$

and

$$A_V \le \frac{V_{EE}+0.6}{V_{EE}+0.6+(V_{CO}-V_{EO})-V_{IHRH}}. \quad (11)$$

V_{IHRH} is the op amp's input head-room voltage—the difference between its positive power supply and its resulting maximum common-mode input voltage—on the high side, and V_{IHRL} is the input head-room voltage on the low side.

You can achieve greater gains than those that the above **equations** allow by cascading multiple stages. Alternatively, you can configure one stage to operate at higher gains using a later-described method.

TRANSIENT CONDITIONS

Once you select gain to keep V_{CM} within the op amp's common-mode input range under dc conditions, you must consider transient signals. The op amp's output has a finite slew rate, and its supplies are a function of its output. Thus, a step function at the op amp's input can easily exceed the amp's supply range. You should not directly apply a square wave to the op amp because it would exceed the device's supplies when the op amp was just beginning to slew. To avoid the latched condition that this situation might cause, place a slew limit on the signal feeding the amplifier to limit transients to less than or equal to the op amp's slew rate (**Figure 4**). To guarantee adequate limitation with a simple RC filter, choose the following RC time constant:

$$R_{IN}C_{IN} \ge \frac{V_{STEP}}{SR}, \quad (12)$$

where SR is the op amp's slew rate and V_{STEP} represents the maximum step size that the signal source can generate.

PHASE REVERSAL

The problem in the above-described dc conditions occurs when both V_{CO} and V_{EO} are farther from ground than V_{CM}. Another problem can occur if V_{CM} exceeds the supply rails. Adding a series resistor is usually sufficient to avoid problems under this condition by limiting the current into the saturated input node. However, some op amps are subject to phase reversal when you drive their input stage to one of the supply rails. When this situation happens, the op amp's output slews to the opposite rail and stays there until the input stage recovers from saturation. In a bootstrapped circuit, the op amp's supply rails slew along with its output, leaving the input far outside the supply rails. This situation can likely cause an unrecoverable condition, potentially destroying the op amp in the process.

If you choose an op amp that is subject to phase reversal, then you must be sure to limit the input amplitude so that the input voltage, V_{CM}, never exceeds the op amp's common-mode input-voltage range. This situation seems identical to the concern with the aforementioned dc conditions, but the dc-gain problem occurs when V_{CM} is *closer* to ground than either supply rail. Phase reversal is a problem when V_{CM} is *farther* from ground than either supply rail.

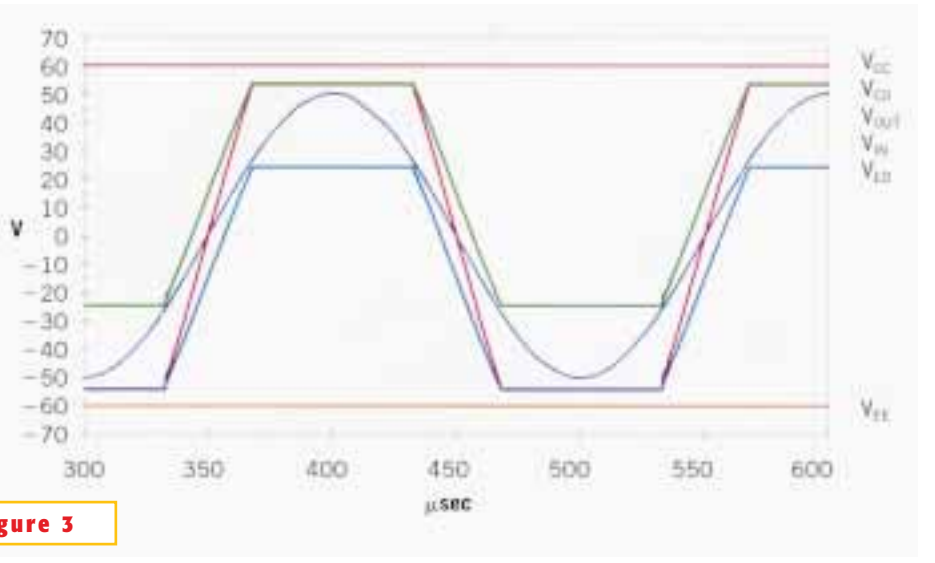


Figure 3

If you properly select gain, the amplifier's output will saturate before its input common-mode range is violated.

POWER-UP CONDITIONS

Because bootstrapped amplifiers are sensitive to latch-up, you must pay additional attention to power-supply sequencing of these circuits. For instance, if the positive rail comes up a few milliseconds before the negative rail, it can send the device supply voltages, V_{CO} and V_{EO}, toward the positive rail while the input remains at ground, thereby violating the op amp's input common-mode range. The best way to avoid the latch-up condition that this situation can cause is to keep the input at ground potential and simultaneously bring the power supplies up (**Figure 5**).

EXPANDING POSSIBILITIES

The common theme of the above points of concern is the op amp's input common-mode range. With proper attention to this detail, you can create bootstrapping circuits with wide-ranging configurations that go far beyond these simple examples.

Consider, for instance, a design with high gain *and* wide output swing. If you need greater gain from a single stage than the gain you can achieve with the circuit in **Figure 1**, then you may find the circuit in **Figure 6** useful. In this configuration,

V_{CM} remains within the op amp's input common-mode range, whereas V_{IN} is much lower in magnitude (**Figure 7**). The gain from V_{CM} to V_{OUT} is the largest possible gain you can achieve based on **equations 14 and 15**, which are identical to **equations 10 and 11**:

$$A_{OUT/CM} = \frac{V_{OUT}}{V_{CM}} = 1 + \frac{R_F}{R_G}, \quad (13)$$

$$A_{OUT/CM} \le \frac{V_{CC} - 0.6}{V_{CC} - 0.6 - (V_{CO} - V_{EO}) + V_{IHRL}}, \quad (14)$$

and

$$A_{OUT/CM} \le \frac{V_{EE} + 0.6}{V_{EE} + 0.6 + (V_{CO} - V_{EO}) - V_{IHRH}}. \quad (15)$$

If a negative value appears on the right side of these inequalities, then you can operate the circuit in **Figure 1** at any gain, and you need not add R_B to the circuit. Otherwise, set $A_{OUT/CM}$ to the highest gain that the above inequalities allow. You can then increase the overall gain of the stage from V_{IN} to V_{OUT} to virtually any gain by adding the resistor, R_B. The expression for this overall gain is:

$$A_{OUT/IN} = \frac{V_{OUT}}{V_{IN}} = \frac{R_G R_B + R_F R_B}{R_G R_B - R_F R_{IN}} = \frac{1 + \frac{R_F}{R_G}}{1 - \frac{R_F}{R_G}\frac{R_{IN}}{R_B}}. \quad (16)$$

But for you to solve for R_{IN} and R_B, it is easier to express the relation in terms of the two gains:

$$\frac{R_{IN}}{R_B} = \frac{A_{OUT/IN} - A_{OUT/CM}}{A_{OUT/IN}(A_{OUT/CM} - 1)}. \quad (17)$$

The condition for **equations 16** and **17** is that $A_{OUT/IN}$ must be greater than $A_{OUT/CM}$ and thereby that R_B/R_{IN} must be greater than R_F/R_G. If you do not meet this condition, the gain equation will "blow up," indicating the circuit's instability.

As with the first example, this circuit requires slew-rate limiting for transient signals. If the slew rate of the incoming signal exceeds $1+R_{IN}/R_B$ times the slew rate of the op amp, then you should add C_{IN} to form a slew-limiting RC time constant,

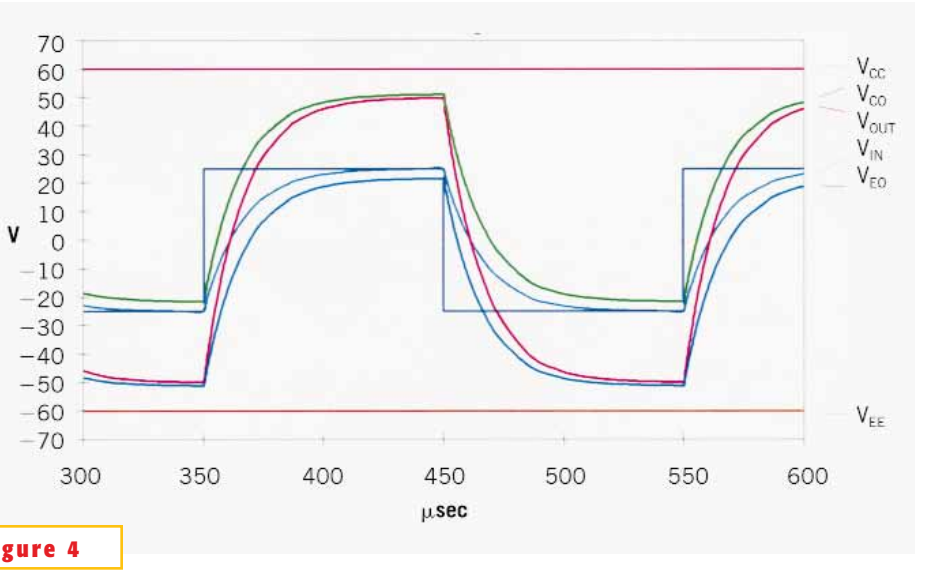


Figure 4

By slew-limiting the amplifier's input, you can avoid transient induced latch-up.

$$\frac{R_B R_{IN}}{R_B + R_{IN}} C_{IN} \ge \frac{R_B}{R_{IN} + R_B} \frac{V_{STEP}}{SR}, \quad (18)$$

which simplifies to:

$$R_{IN} C_{IN} \ge \frac{V_{STEP}}{SR}. \quad (19)$$

This **equation** is exactly the same as **Equation 12** in the first example. However, a simple $R_{IN}C_{IN}$ time constant no longer describes the pole that C_{IN} introduces. The pole frequency of the circuit in **Figure 6** includes the effects of all four resistors in the two feedback networks:

$$f_P = \frac{1 - \frac{R_F}{R_G}\frac{R_{IN}}{R_B}}{2\pi C_{IN} R_{IN}} = \frac{1}{2\pi C_{IN} R_{IN}} - \frac{R_F}{2\pi C_{IN} R_G R_B}. \quad (20)$$

To limit noise bandwidth, you should place f_p as low as possible without affecting desired signals.

OFFSETS, NOISE, AND NONIDEAL BEHAVIOR

Because of the two feedback networks, an error analysis of the circuit in **Figure 6** is somewhat more complex than for a basic op-amp gain stage. Because the mechanics of the error analysis are beyond the scope of this article, the following **equations** omit derivations. For consistency, all errors are referred to the output. To obtain input-referred errors, you simply divide by the signal gain given in **Equation 16**.

You can define the noise gain of an op-amp stage as the amplification from the op amp's input voltage noise to the output of the gain stage. Noise gain is also the gain that amplifies the op amp's input offset voltage. At low frequencies, including dc, the noise gain of the circuit in **Figure 6** is:

$$A_N = \frac{V_{OUT(NOISE)}}{V_{NOISE}} = \frac{(R_F + R_G)(R_B + R_{IN})}{R_G R_B - R_F R_{IN}}, \quad (21)$$

where V_{NOISE} can be either the op amp's input offset voltage (for dc analysis) or the op amp's input-voltage noise. For wideband voltage-noise analysis, the following pole and zero further define this transfer function from V_{NOISE} to V_{OUT}:

$$f_P = \frac{1}{2\pi C_{IN} R_{IN}} - \frac{R_F}{2\pi C_{IN} R_G R_B}; \quad (22)$$

$$f_Z = \frac{1}{2\pi C_{IN} R_{IN}} + \frac{1}{2\pi C_{IN} R_B}. \quad (23)$$

To determine output error due to op-amp offset voltage, you simply multiply the op amp's V_{OS} by the circuit's dc noise gain, A_N (**Equation 21**). You should use the same approach with the op amp's low-frequency (1/f) noise to refer it to the output. Solving for wideband rms output noise is more complex, but you can simplify the task if f_p and f_Z are far enough

apart to let you assume a single-pole noise roll-off. In this case, simply multiply the op amp's input voltage-noise density by $A_N\sqrt{1.57f_p}$ to obtain the resulting output-referred rms noise voltage (**Reference 1**).

The effects of the op amp's input bias currents and current noise are similar to those of offset voltage and voltage noise in that you translate them into output-referred voltage errors. One difference between these effects is that, in the case of current errors, both the inverting and noninverting inputs induce separate errors in the output. You can sum—as a "root sum of squares" for noise—all output-referred errors to obtain a total output error.

For dc and low frequencies, you translate the input current errors to output referred voltage errors using the following **equations**:

$$V_{OUT(NOISE+)} = -\frac{R_{IN}R_B(R_F+R_G)}{R_GR_B-R_FR_{IN}}I_{NOISE+}; \quad (24)$$

$$V_{OUT(NOISE-)} = \frac{R_FR_G(R_B+R_{IN})}{R_GR_B-R_FR_{IN}}I_{NOISE-}, \quad (25)$$

where I_{NOISE+} is the input current noise or input bias current at the noninverting input, I_{NOISE-} is the same for the inverting input, and $V_{OUT(NOISE+)}$ and $V_{OUT(NOISE-)}$ are the output-referred errors that result from each.

Again, for wideband-noise analysis, you must consider the effects of C_{IN}. For both the noninverting and inverting current-noise transfer functions, a pole appears at:

$$f_P = \frac{R_GR_B-R_{IN}R_F}{2\pi C_{IN}R_{IN}R_GR_B}, \quad (26)$$

which applies to **equations 24** and **25**. For the inverting current noise only, a zero appears at:

$$f_Z = \frac{R_B+R_{IN}}{2\pi C_{IN}R_{IN}}, \quad (27)$$

which applies only to **Equation 25**.

As with voltage-noise analysis, you can simplify the transfer function by assuming a single-pole roll-off. In this case, to determine the rms output noise resulting from input current noise, you can simply multiply the values obtained from **equations 24** and **25** for wideband noise density by $A_N\sqrt{1.57f_p}$ where f_p comes from **Equation 26**.

You have considered offset voltage and two bias currents as sources of dc error and voltage noise and two current noises as sources of noise, and you have referred each source of error to the output. Now, you must sum these errors. For dc errors, this summing takes the form of a simple sum of the magnitude of each error term. But the noise errors add instead as a root sum of squares; that is:

$$V_{TOTAL} = \sqrt{V_1^2 + V_2^2 + V_3^2}. \quad (28)$$

In most cases, either the op amp's voltage noise or one of its current noises dominates the total output noise. The smaller output-referred noise terms generally make a negligible contribution to total noise. However, you should also consider the Johnson noise of the signal path resistors, R_F, R_G, R_{IN}, and R_B (**Refer-**

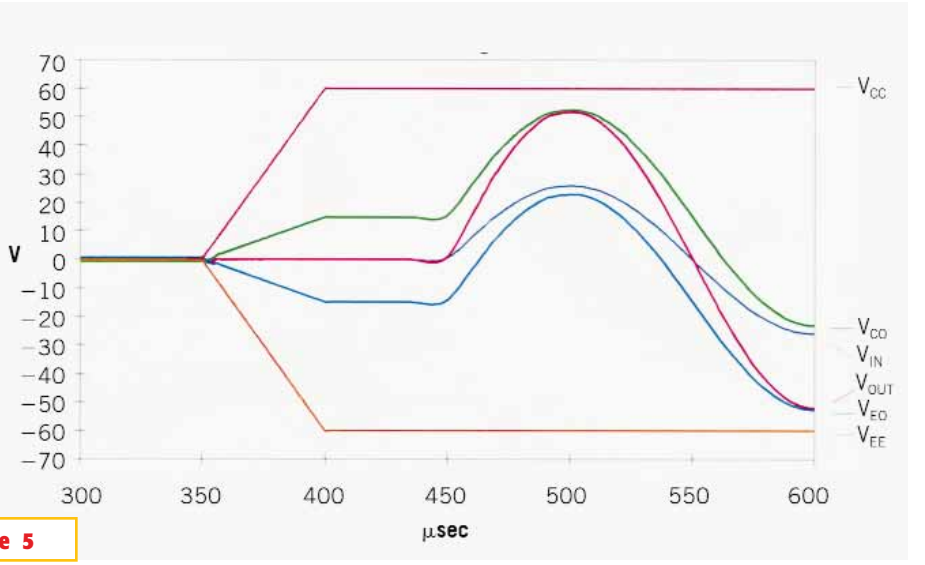


Figure 5

Careful attention to power-supply sequencing can prevent power-on latch-up.

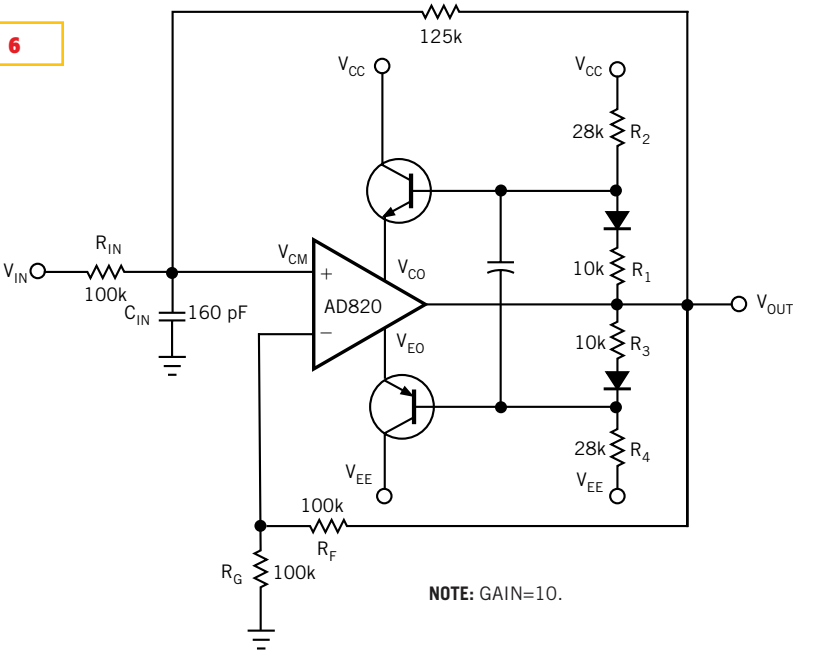


Figure 6

You can slightly modify the basic design of the circuit in Figure 1 to achieve higher gains.

ence 1). As with the other noise sources, you should refer these noises to the output and add them as a root sum of squares with the other output noise values.

LOW DEVICE-SUPPLY VOLTAGE

It may be intuitively clear that it is best to set the op amp's device supply voltage, $V_{CO} - V_{EO}$, near its maximum specified operating voltage when you are bootstrapping for wide signal swings. But to explicitly show how a device's supply voltage affects performance, consider the following configurations. Both have ±60V system power supplies, and both require a gain of 10. However, the device supply is 30V in one case and 10V in the other (see **tables 2** and **3**, respectively, at www.ednmag.com). To design these two circuits, you select R_1 and R_2 using **Equation 9** to achieve the desired device supply voltage. You then choose R_F and R_G to achieve a gain as high as possible from V_{CM} to V_{OUT} and to meet the conditions of **equations 14** and **15.** For this example, assume op-amp input head room of 1V from each rail in both cases. **Equation 17** then gives us the ratio of R_{IN}/R_B that will result in a gain of 10 from V_{IN} to V_{OUT}, and the two circuits are complete. To determine the noise gain of each, use the component values in **Equation 21**. The results of this exercise show that, by reducing by one-third the device's supply voltage, you almost quadruple the output error.

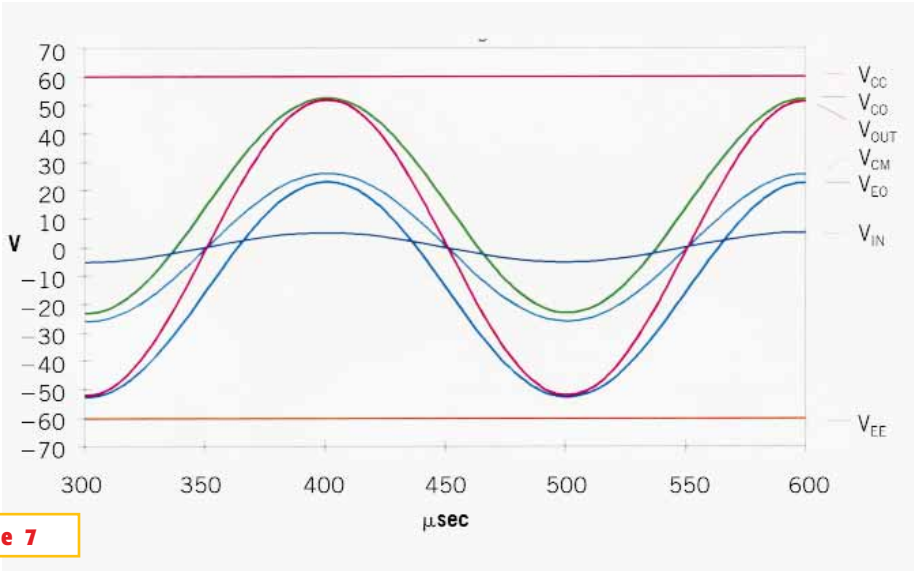


Figure 7

This simulation of the circuit in Figure 6 shows a gain of 10 from V_{IN} to V_{OUT} but a gain of only 2 from V_{CM} to V_{OUT}.

OP-AMP SELECTION

Bootstrapping is a way to use just about any monolithic op amp to output wide signal swings. Even so, you should choose an op amp that can operate with a fairly high supply voltage to begin with; the above comparison shows the advantage of this approach. Hundreds of commonly available op amps operate from 30 or 40V power supplies, so avoid choosing one with a maximum V_{CC} of only 5 or 10V. Beyond that, individual system requirements determine what precision, speed, and other parameters the op amp should offer. Some important parameters to consider include the following:

Output current drive: At high-voltage swings, even a 2-kΩ load can pull significant current.

Input bias current: Large-value resistors in feedback paths make it useful to have a FET input stage.

Slew rate: Slew-rate limiting can distort large-magnitude ac signals.

Table 4 at www.ednmag.com shows a few op amps from Analog Devices suitable for bootstrapping, including both FET and bipolar input stage devices. This list is not comprehensive. Each bootstrapping application has a unique set of requirements for op-amp parameters, so if what you require doesn't appear on this list, look through various vendors' op-amp offerings. Regardless of your application, the choice of op amp requires knowledge of design requirements. Use the equations to answer the following questions:

What slew rate does your design need? (See **equations 19** and **20**.)

How will offset voltage and bias current affect output error? (See **equations 21**, **24**, and **25**.)

Will a rail-to-rail input stage or wider device supply (maximum V_S) significantly improve performance? (See **equations 9**, **14**, **15**, **17**, **21**, **24**, and **25**.)

Also keep in mind that a FET input stage can allow you to use larger value resistors in the feedback network with minimal impact on total output error.

CONSIDER A COMPOSITE APPROACH

When looking at the op amps in **Table 4**, you might notice that the devices with the greatest output current drive, I_{OUT}, are not those with the best dc precision, V_{OS} and I_B. This situation is largely true for all op amps. However, an alternative exists for precision applications needing more than a few tens of milliamps of output current drive. By connecting two op amps in a composite configuration (**Figure 8**), you can use the slew rate and output current drive capabilities of one device and the dc precision of the other. Because the input amp globally closes the feedback loop, the imprecise output amp can provide the necessary muscle without adding error to the system.

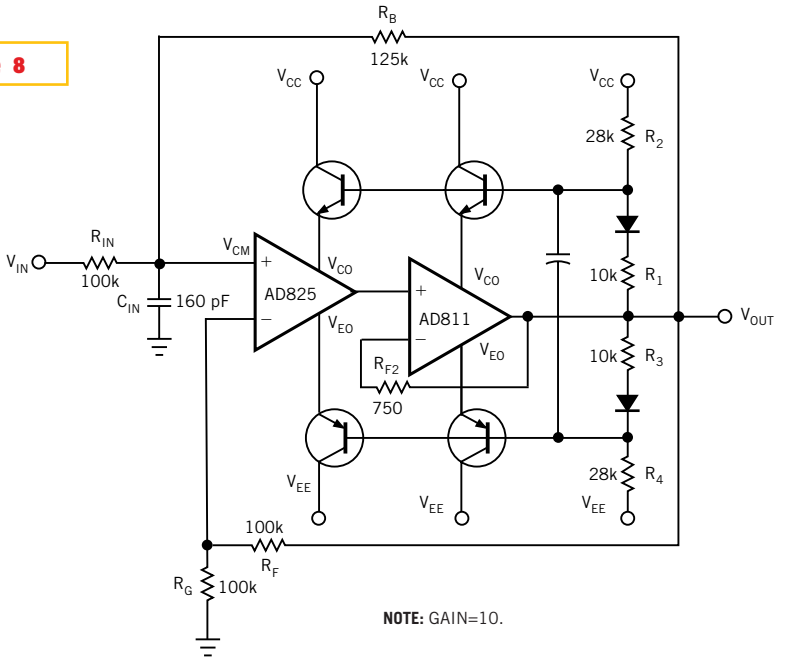
The feedback network, consisting of R_F, R_G, R_B, R_{IN}, and C_{IN}, and the bootstrap network, R_1 through R_4 plus two diodes in **Figure 8**, are the same as those in **Figure 6**. Further, the **equations** for calculating component values and error terms apply equally to both **figures**. The only component value in **Figure 8** that the **Figure 6** analysis omits is the new feedback resistor, R_{F2}. Anyone familiar with current feedback op amps will recognize the importance of this resistor. If you use an op amp other than the AD811 you have to choose the value of R_{F2} based on the op amp's data sheet, in which a table of recommended values for different gains generally appears. Values larger than those recommended reduce the op amp's bandwidth and slew rate. Values

smaller than those recommended degrade stability, possibly resulting in oscillations. If you use a voltage-feedback op amp as the output device, the value of R_{F2} can be as low as 0Ω or a shorted connection.

Table 5 (at www.ednmag.com) shows a few op amps that fit well into **Figure 8**'s circuit. An AD825 or OP97 performs well as the input device, and an AD811 or AD815 current-feedback device offers advantages in the output stage. Current-feedback op amps are generally poor choices for bootstrapping because of their sensitivity to feedback-network impedance. However, they make excellent output amps in this composite circuit because they connect in a simple unity-gain mode, and the input amp handles the high-impedance global-feedback paths.

The output current drive, I_{OUT}, of the input amp makes no difference because the output op amp drives the load (**Table 5**). Also, the input offset voltage, V_{OS}, of the output amp causes no output error because the input amp closes the global-feedback loop. By carefully selecting two op amps for a composite configuration, you can achieve performance that is unavailable from any single device.

Figure 8



A two-stage composite amplifier lets you combine the advantages of two op amps.

TIE UP LOOSE ENDS

You must now consider the transistors that form the bootstrapping network itself. You have as much flexibility in selecting these transistors as you have in selecting the op amps. The primary concerns are:

- Breakdown voltages, V_{CB} and V_{CE} (an important parameter for obvious reasons);
- βor h_{FE}: Higher beta allows larger value resistors for R_1 through R_4.
- Power dissipation: In most cases, the transistors must dissipate more power than the op amps.

Tests for this article use ZTX653 and ZTX753 from Zetex (www.zetex.com). These transistors have h_{FE} greater than 100 and breakdown voltages greater than 100V. Their power dissipation is not of great concern for test purposes, because the test circuits were not driving significant loads. In place of the diodes in series with R_1 and R_3, the tests simply used these same transistors in a "diode-connected" configuration.

You can use MOSFETs instead of bipolar transistors. The primary disadvantage of MOSFETs in these circuits is head room. Therefore, if your design doesn't require that its output voltages approach the system supply rails, then MOSFETs might be a good choice. When you use MOSFETs, you should, if possible, replace the diodes that are in series with R_1 and R_3 with a few series diodes to approximate the MOSFET's V_{GS} voltage. Alternatively, you can diode-connect a second pair of MOSFETs in place of the diodes to achieve the same basic function.

As with most analog circuits, lack of adequate power-supply decoupling can appreciably degrade performance, especially when transient signals need accurate amplification. Unlike typical op-amp circuits, however, a bootstrapped circuit has local power supplies, V_{CO} and V_{EO}, that move dynamically with signal voltage. Therefore, you should not decouple these nodes directly to ground. The best place for local bypass capacitors, in this case, is between the bases of the two bootstrap-network transistors (**figures 1**, **6**, and **8**). In addition to this local decoupling of the device supplies, V_{CO} and V_{EO}, you should decouple the system supplies, V_{CC} and V_{EE}, directly to ground. □

REFERENCE

1. *Linear Design Seminar*, Analog Devices Inc, 1995, Section 1.

AUTHOR BIOGRAPHIES

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TABLE 2 - KEY DESIGN PARAMETERS FOR A 30V DEVICE SUPPLY CONFIGURATION

parameter		value
$R_1 = R_3$	=	10KΩ
$R_2 = R_4$	=	28KΩ
V_{C0}-V_{EO}	=	31V
$A_{OUT/CM}$	=	2.0
R_F	=	100KΩ
R_G	=	100KΩ
$A_{OUT/IN}$	=	10.0
R_{IN}	=	100KΩ
R_B	=	125KΩ
A_N	=	**18**

TABLE 3 - KEY DESIGN PARAMETERS FOR A 10V DEVICE SUPPLY CONFIGURATION

parameter		value
$R_1 = R_3$	=	10KΩ
$R_2 = R_4$	=	107KΩ
V_{C0}-V_{EO}	=	10V
$A_{OUT/CM}$	=	1.182
R_F	=	18.2KΩ
R_G	=	100KΩ
$A_{OUT/IN}$	=	10.24
R_{IN}	=	243KΩ
R_B	=	50KΩ
A_N	=	**60**

TABLE 4 - SOME BOOTSTRAP FRIENDLY OP AMPS AND THEIR KEY PARAMETERS

part #	type	V_{OS}	I_B	V_{IHRH}	V_{IHRL}	V_{OHRH}	V_{OHRL}	I_{OUT}	GBP	SR	maxV_S
AD711	FET	300µV	15pA	0.5V	3.5V	1.1V	1.7V	25mA	4MHz	20V/µs	36V
AD820	FET	100µV	2pA	1V	-0.2V	0.01V	0.005V	15mA	1.9MHz	3V/µs	36V
AD825*	FET	1mV	10pA	1.5V	1.5V	1.6V	1.6V	26mA	46MHz	140V/µs	36V
AD843*	FET	1mV	50pA	3V	2V	3.5V	2.4V	50mA	24MHz	250V/µs	36V
AD845	FET	700µV	750pA	4.5V	2V	2.5V	2.5V	25mA	16MHz	100V/µs	36V
OP176	FET	1mV	350nA	4.5V	4.5V	1.5V	1.5V	40mA	10MHz	25V/µs	44V
OP42	FET	1.5mV	130pA	2.5V	2.5V	3.1V	2.5V	25mA	10MHz	50V/µs	40V
AD817*	BIP	500µV	3.3µA	0.7V	1.6V	1.3V	1.3V	50mA	50MHz	350V/µs	36V
AD841*	BIP	800µV	3.5µA	3V	3V	5V	5V	50mA	40MHz	300V/µs	36V
AD847*	BIP	500µV	3.3µA	0.7V	1.6V	1.4V	1.4V	20mA	50MHz	300V/µs	36V
OP07*	BIP	30µV	1nA	1V	1V	2V	2V	25mA	600KHz	0.3V/µs	44V
OP113*	BIP	150µV	600nA	1V	0V	1V	0.5V	20mA	3.4MHz	1.2V/µs	36V
OP177*	BIP	10µV	2nA	1V	1V	1V	1V	25mA	600KHz	300V/µs	44V
OP183*	BIP	100µV	300nA	1.5V	0V	0.75V	0.09V		5KHz	15V/µs	36V
OP184*	BIP	175µV	80nA	0V	0V	0.15V	0.15V	10mA	4.25MHz	4V/µs	36V
OP193*	BIP	150µV	20nA	1V	0V	0.86V	0.28V	10mA	35KHz	0.015V/µs	36V
OP27*	BIP	30µV	15nA	2.7V	2.7V	2.2V	2.2V	25mA	8MHz	2.8V/µs	44V
OP77*	BIP	50µV	1.2nA	1V	1V	1V	1V	25mA	600MHz	300V/µs	44V
OP90*	BIP	125µV	4nA	1V	0V	0.8V	0.01V	20mA	20KHz	0.012V/µs	36V
OP97*	BIP	30µV	30pA	1V	1V	1V	1V	20mA	900KHz	0.2V/µs	40V

***** Device is immune to potential phase reversal.

TABLE 5 - SOME COMPOSITE-FRIENDLY OP AMPS AND THEIR KEY PARAMETERS

part #	type	V_{OS}	I_{B+}	V_{IHRH}	V_{IHRL}	V_{OHRH}	V_{OHRL}	I_{OUT}	GBP	SR	maxV_S
AD825*	FET	1mV	10pA	1.5V	1.5V	1.6V	1.6V	26mA	46MHz	140V/µs	36V
OP97*	BIP	30µV	30pA	1V	1V	1V	1V	20mA	900KHz	0.2V/µs	40V
AD811*	CF	3mV	2µA	2V	2V	3V	3V	100mA	140MHz	2500V/µs	36V
AD815*	CF	10mV	2µA	1.5V	1.5V	1V	1V	750mA	120MHz	900V/µs	36V

***** Device is immune to potential phase reversal.