IMT 902 Microstep Constant Current Driver for 2 Motors

- 2 stepping motors are controlled by a single driver IC
- Output voltage 40 V max
- Output current 1.5 A /phase max
- Two pairs of built-in 4-bit DACs for micro steps
- Two pairs of built-in 16-bit shift and latch registers
- 36-pin power flat package (HSOP36-P-450-0.65)
- Low On-resistance of R_{on} = 0.5 Ω (T_j = 25°C @ 1.0 A: Typ.)
- Chopping frequency can be set by external capacitors and resistors. High speed chopping possible at 100 kHz or higher
- Built-in charge pump circuit (two ext. capacitors)

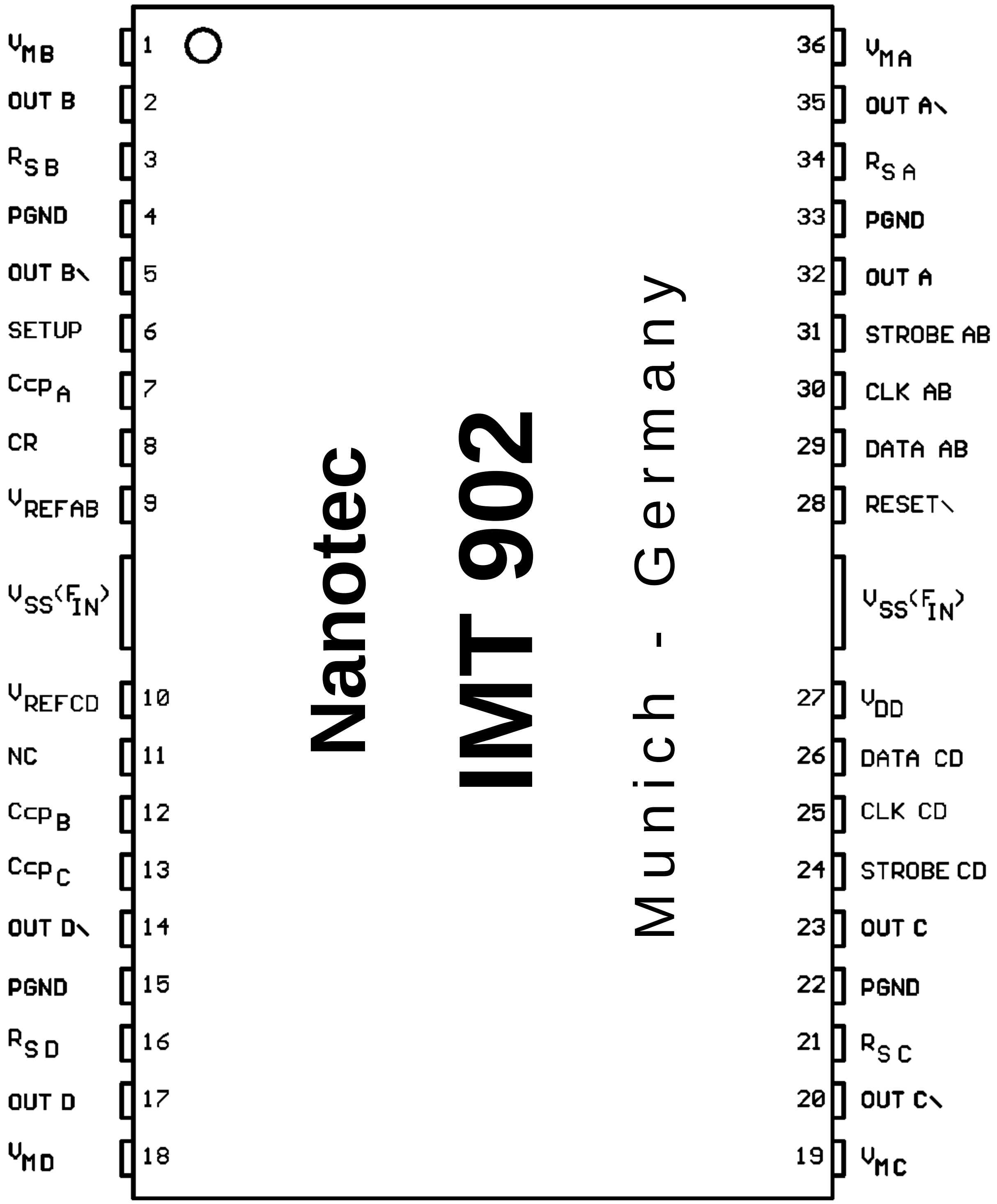
RECOMMENDED AND MAXIMUM OPERATING CONDITIONS
(T_a = 0 to 85°C)

Characteristic	Sym.	Test Condition	Min.	Typ.	Max.	Peak	Unit
Logic Supply Voltage	V_{DD}	-	4.5	5.0	5.5	7.0	V
Output Voltage	V_M	V_{DD} = 5,0 V	20	24	34	40	V
Output Current	I_{Out} (1)	T_a = 25° C / Phase (one motor)	-	1.1	1.3	1.5	A
	I_{Out} (2)	T_a = 25° C / phase (two motors)	-	1.1	1.3	1.5	A
Logic Input Voltage	V_{IN}	-	GND	-	V_{DD}	V_{DD}+0.4	V
Clock Frequency	f_{CLK}	V_{DD} = 5,0 V	1.0	6.25	25	-	MHz
Chopping Frequency	f_{chop}	V_{DD} = 5,0 V	40	100	150	-	KHz
Reference Voltage	V_{ref}	V_M = 24 V, Torque = 100%	2.0	3.0	V_{DD}	-	V
Current Detect Pin Voltage	V_{RS}	V_{DD} = 5,0 V	0	± 1.0	± 1.5	± 4.5	V
Power Dissipation	P_D	V_{IN} 7V or less	-	-	1.4		W
		Measured for IC	-	-	3.2		
Operating Temp.	T_{OPR}				- 40 ...+ 85		°C
Storage Temp.	T_{STG}				- 50 ...+ 150		°C
Junction Temp.	T_J				+ 150		°C

Note: when using the IC, pay attention to thermal conditions.

PIN ASSIGNMENT:

(top view)



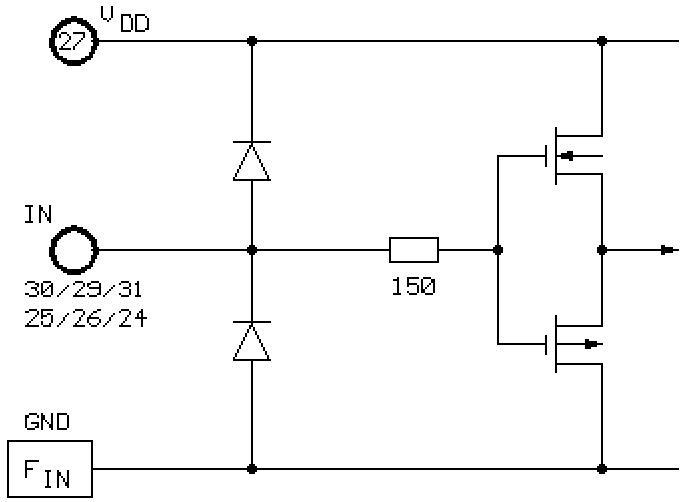
PIN DESCRIPTION:

Pin No.	Pin Symbol	Description
1	**$V_{M\ B}$**	Power Supply for output B block
2	**OUT B**	Output B pin
3	$R_{S\ B}$	Channel B current pin
4	**PGND**	Power GND pin
5	**OUT B**	Output B\\ pin
6	LGND	Logic GND pin
7	Ccp A	Capacitor pin for charge pump (Ccp 1) (Capacitor C2, see Pg. 5)
8	CR	External C/R (osc) pin (sets chopping frequency)
9	$V_{REF\ AB}$	V_{ref} input pin AB
F_{IN}	**V_{SS} (F_{IN})**	Logic GND pin
10	$V_{REF\ CD}$	V_{ref} input pin CD
11	NC	Non conection
12	Ccp B	Capacitor pin for charge pump (Ccp 2) (Capacitor C1, see Pg. 5)
13	Ccp C	Capacitor pin for charge pump (Ccp 3) (Capacitor C1, see Pg. 5)
14	**OUT D**	Output D\\ pin
15	**PGND**	Power GND pin
16	$R_{S\ D}$	Channel D current pin
17	**OUT D**	Output D pin
18	**$V_{M\ D}$**	Power Supply for output D block
19	**$V_{M\ C}$**	Power Supply for output C block
20	**OUT C**	Output C\\ pin
21	$R_{S\ C}$	Channel C current pin
22	**PGND**	Power GND pin
23	**OUT C**	Output C pin
24	STROBE CD	CD STROBE (latch) signal input pin
25	CLK CD	CD clock input pin
26	DATA CD	CD serial data signal input pin
27	V_{DD}	Power pin for logic block
F_{IN}	**V_{SS} (F_{IN})**	Logic GND pin
28	RESET\\	Output reset signal input pin
29	DATA AB	AB serial data signal input pin
30	CLK AB	AB clock input pin
31	STROBE AB	AB STROBE (latch) signal input pin
32	**OUT A**	Output A pin
33	**PGND**	Power GND pin
34	$R_{S\ A}$	Channel A current pin
35	**OUT A**	Output A\\ pin
36	**$V_{M\ A}$**	Power Supply for output A block

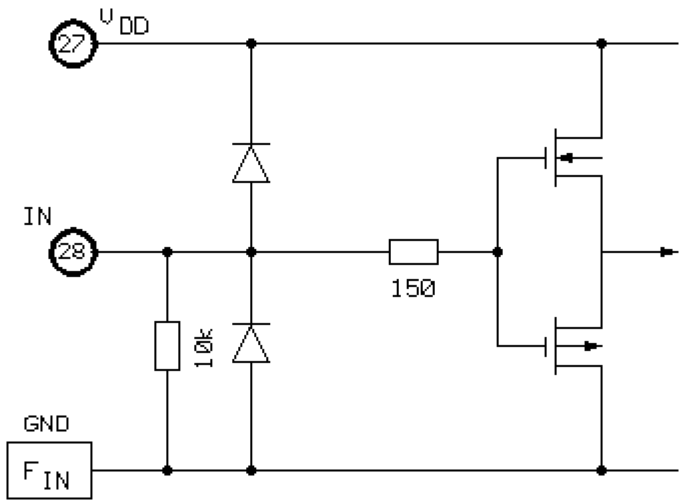
Note: All GND pins and F_{IN} pins must be grounded. Since F_{IN} also functions as a heat sink, take the heat dissipation into consideration when designing the board.

Input equivalent circuit:

1) Logic input circuit (CLK, DATA, STROBE)



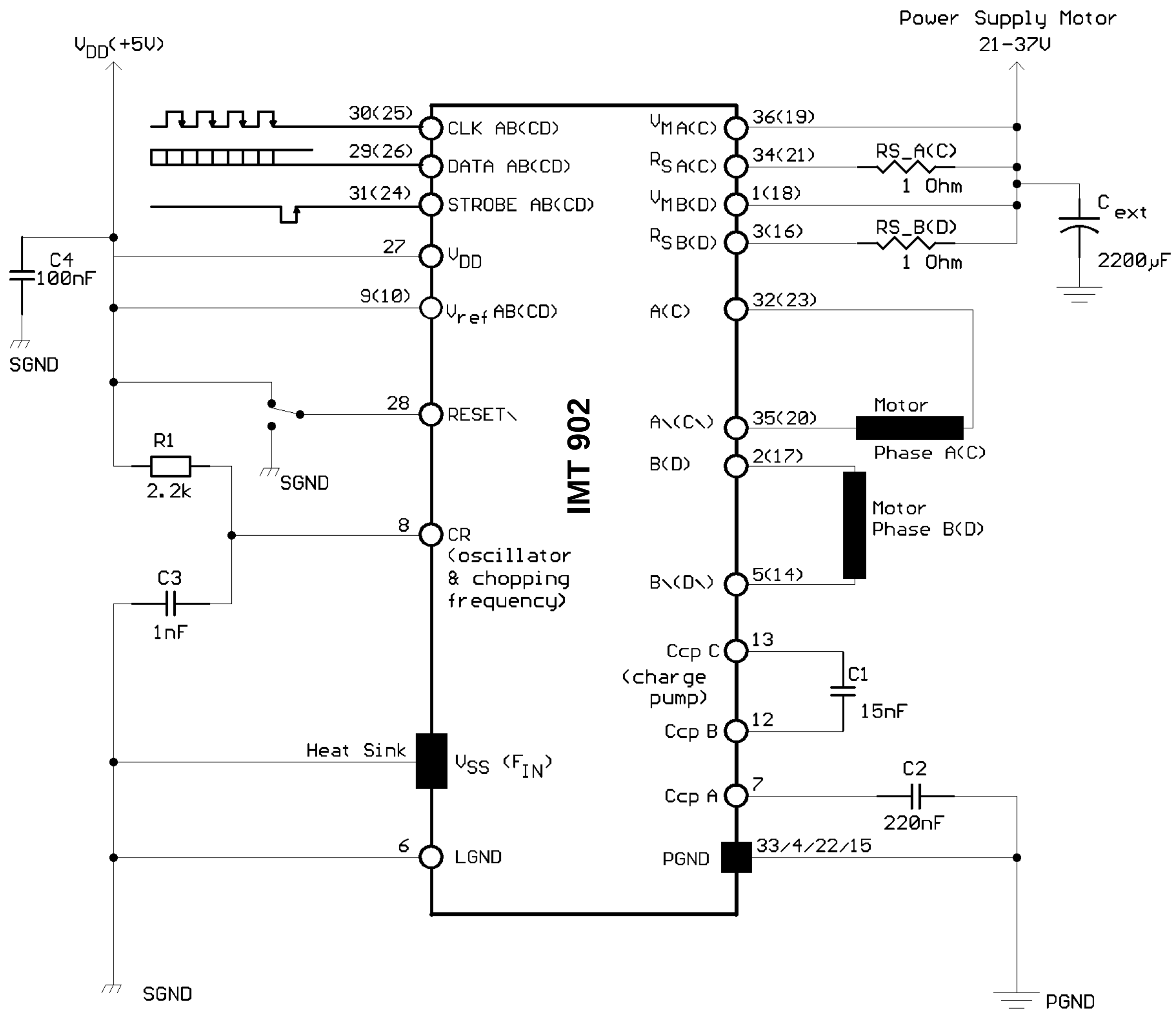
2) Input circuit (RESET\)



Note: The RESET\ pin is pulled down. Do not use this pin open.

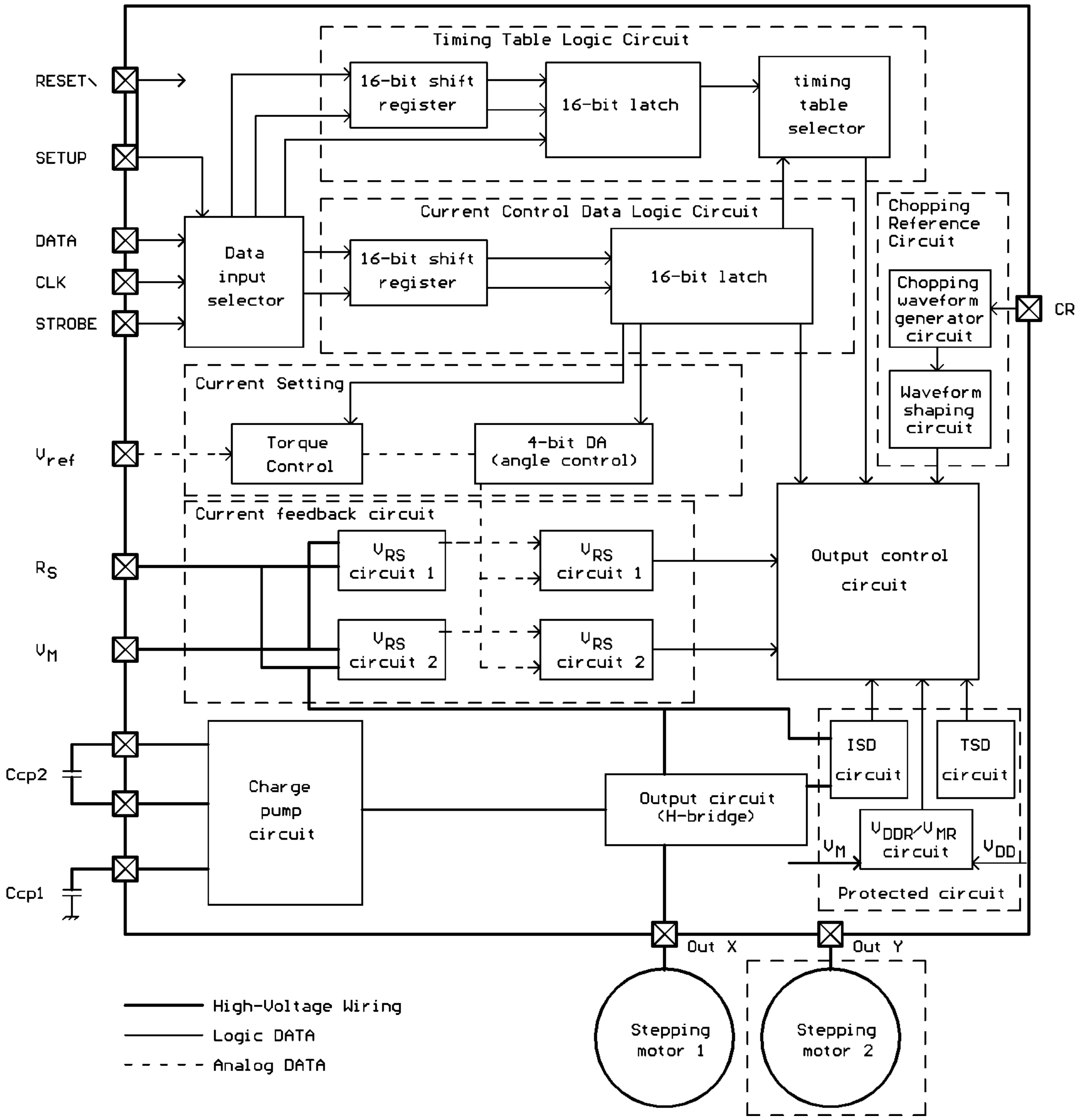
Application example:

(A/B unit only. C/D unit in brackets)



Block Diagram:

(A/B unit, C/D unit is the same as A/B unit)



Calculation of set current:

Determining R_S and V_{ref} determines the set current value.

$$I_{OUT} = \frac{V_{ref}(V) * HoldCurrent(=1.0/0.85/0.7/0.5)}{5 * R_S(\Omega)}$$

For example:

To input V_{ref} = 5.0 V and hold current = 100 % (= 1.0) and to output I_{out} = 1A,

R_S = 1 Ω (1 W or more) is required.

Calculation of CR oscillation frequency (Chopping reference frequency)**:**

The CR oscillation frequency and f_{chop} can be calculated by the following formulas:

$$f_{CR} = \frac{1}{C * (0.523R + 313.8)}[Hz]$$

$$f_{chop} = \frac{f_{CR}}{8}[Hz]$$

For example:

When Cosc = 1 nF (=C3) and Rosc = 2200 Ω (= R1) are connected to the CR pin, the oscillation frequency is calculated as 682 kHz.
At this time the chopping frequency f_{chop} is f_{CR}/8 = 85.4 kHz.

IC Power Dissipation:

Power consumed by the Power Transistor (calculated with $R_{DS\ ON} = 0.6\ \Omega$):

$$P(\text{out}) = 2(Tr) * I_{out}(A) * V_{DS}(V) = 2 * I_{out}^2 * R_{DSon}$$

Power consumed by the logic block:

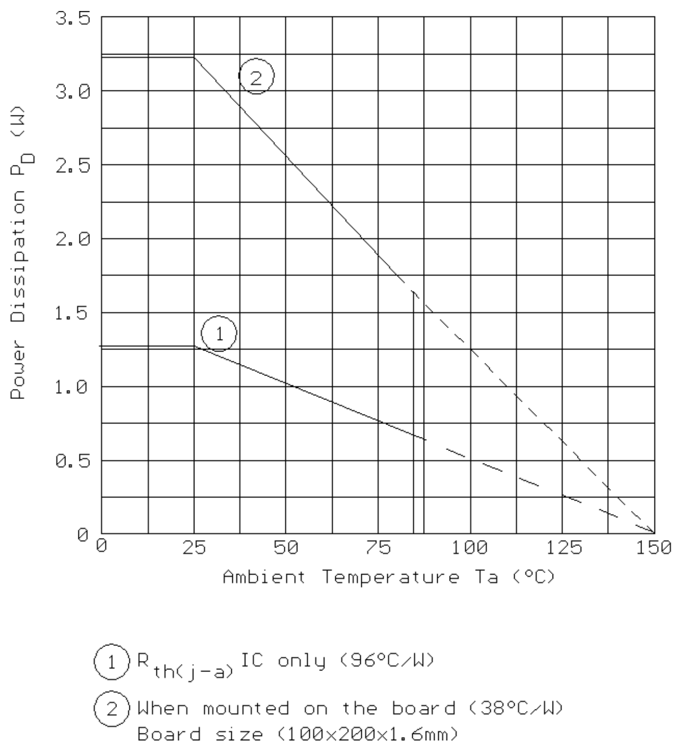
Operating mode / unit when V_{DD} is connected to 5V and V_M is connected to 24V:

$$P = 5(V) * 0.002(A) + 24(V) * 0.0125(A) = \underline{\underline{0.31(W)}}$$

Standby mode (RESET\=L) / unit:

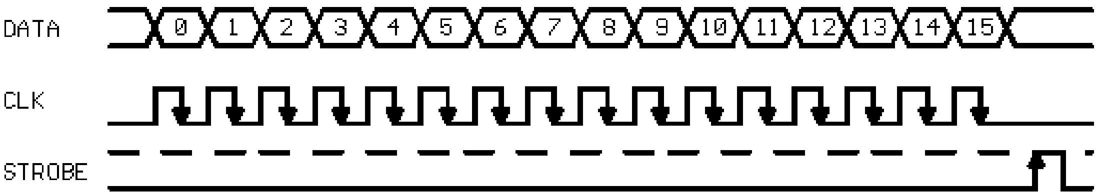
$$P(\text{standby}) = 24(V) * 0.006(A) + 5(V) * 0.002(A) = \underline{\underline{0.154(W)}}$$

PD-Ta (Package power dissipation)



Signal functions:

Serial data input setting:



Data input to the serial pin are 16-bit data transfered from DATA 0 to DATA 15.
Data are input and transfered at the following timings:

At clock falling edge: data input
At clock rising edge: data transfer

After data are transferred, all data are latched on the rising edge of the STROBE signal. As long as STROBE is not rising, the signal can be either low or high during data transfer.

Serial input signals (for A/B, C/D is the same as A/B):

DATA No.	NAME	FUNCTIONS
0 LSB	Hold Current 0	DATA No. 0,1: HH: 100% LH: 85%
1	Hold Current 1	HL: 70% LL: 50%
2	Decay Mode B_0	00: Slow Decay 01: Mixed Decay 37.5 %
3	Decay Mode B_1	10: Mixed Decay 75% 11:Fast DEcay
4	Current B_0	Used for setting current.
5	Current B_1	(LLLL = output all off mode)
6	Current B_2	4-bit current B data
7	Current B_3	(steps can be devidied into 16 by 4-bit data)
8	Phase B	Phase information: High = OUT B High, OUT B\ Low
9	Decay Mode A_0	00: Slow Decay 01: Mixed Decay 37.5 %
10	Decay Mode A_1	10: Mixed Decay 75% 11:Fast DEcay
11	Current A_0	Used for setting current.
12	Current A_1	(LLLL = output all off mode)
13	Current A_2	4-bit current A data
14	Current A_3	(steps can be devidied into 16 by 4-bit data)
15 MSB	Phase A	Phase information: High = OUT A High, OUT A\ Low

Hold Current Functions (= current down; DATA No. 0, 1)

Hold Current 0	Hold Current 1	Comparator reference voltage ratio
H	H	100%
L	H	85%
H	L	70%
L	L	50%

Decay Mode Functions (DATA No. 2, 3)

Decay Mode X_1	Decay Mode X_0	Function
L	L	Slow Decay 0%
L	H	Mixed Decay 37.5%
H	L	Mixed Decay 75%
H	H	Fast Decay 100%

Current Ax (Bx) functions (Data No. 4 to 7 and 11 to 14)

STEP	SET ANGLE	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
16	90.0	H	H	H	H	L	L	L	L
15	84.4	H	H	H	H	L	L	L	H
14	78.8	H	H	H	L	L	L	H	L
13	73.1	H	H	L	H	L	L	H	H
12	67.5	H	H	L	L	L	H	L	L
11	61.2	H	L	H	H	L	H	L	H
10	56.3	H	L	H	L	L	H	H	L
9	50.6	H	L	L	H	L	H	H	H
8	45.0	H	L	L	L	H	L	L	L
7	39.4	L	H	H	H	H	L	L	H
6	33.8	L	H	H	L	H	L	H	L
5	28.1	L	H	L	H	H	L	H	H
4	22.5	L	H	L	L	H	H	L	L
3	16.9	L	L	H	H	H	H	L	H
2	11.3	L	L	H	L	H	H	H	L
1	5.6	L	L	L	H	H	H	H	H
0	0.0	L	L	L	L	H	H	H	H

By inputting the above current data, 16-microstep drive is possible.

Phase functions (Data No. 8 and 15)

INPUT	FUNCTION
H	Positive polarity (A = H, A\ = L)
L	Negative polarity (A = L, A\ = H)

Serial input signal functions

INPUT						ACTION
CLK	STROBE	DATA	RESET\	V_{DDR} Or V_{MR}	TSD [1] / ISD[2]	
↑	X	X	H	H	L	No change in shift register
↓	X	H	H	H	L	H level is input to shift register
↓	X	L	H	H	L	L level is input to shift register
X	↑	X	H	H	L	Shift register data are latched
X	X	X	L	X	L	Output off, charge pump halted
X	X	X	X	L	L	Output off, charge pump halted (only V_{DDR})
X	X	X	H	H	H	Output off, charge pump halted Restored when Reset\ goes from low to high

X: Don't care

V_{DDR}: (return voltage V_{DD} and V_M) H when the operable range (3V typical) or higher and L when lower.

[1] TSD:(Thermal shut down circuit):
When the IC junction temperature reaches the specified value and the TSD circuit is activated, the internal reset circuit is activated switching the outputs of both motors off. When the temperature is set between 130 to 170°C (max), the TSD circuit operates. When the TSD circuit is activated, the function data latched at that time are cleared. Output is halted until the reset is released. While the TSD circuit is in operation, the charge pump is halted.
Even if the TSD circuit is activated and RESET goes H ⇒ L ⇒ H instantaneously, the IC is not reset until the IC junction temperature drops 35°C (typ.) below the TSD operating temperature (hysteresis function)

[2] ISD: (Overcurrent protection circuit)
When current exceeding the specified value flows to the output, the internal reset circuit is activated switching the outputs of both shafts to off. When the ISD circuit is activated, the function data latched at that time are cleared. Until the reset signal is input, the overcurrent protection circuit remains activated. During ISD the charge pump is halted. For failsafe operation be sure to add a fuse to the power supply.

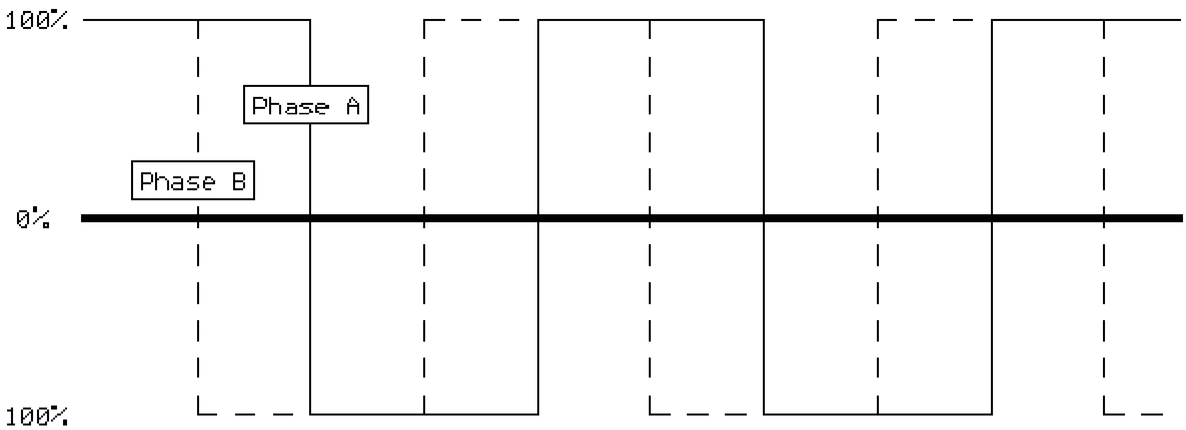
Application operation input data:

<u>1/1 – Step</u>

	Hold Current 0	Hold Current 1	Decay B_0	Decay B_1	B_0	B_1	B_2	B_3	Phase B	Decay A_0	Decay A_1	A_0	A_1	A_2	A_3	Phase A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
2	1	1	1	0	1	1	1	1	0	1	0	1	1	1	1	1
3	1	1	1	0	1	1	1	1	0	1	0	1	1	1	1	0
4	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) reqires input of the STROBE signal. Hold Current is set to 100%.

Output current waveform of 2-phase excitation sine wave:

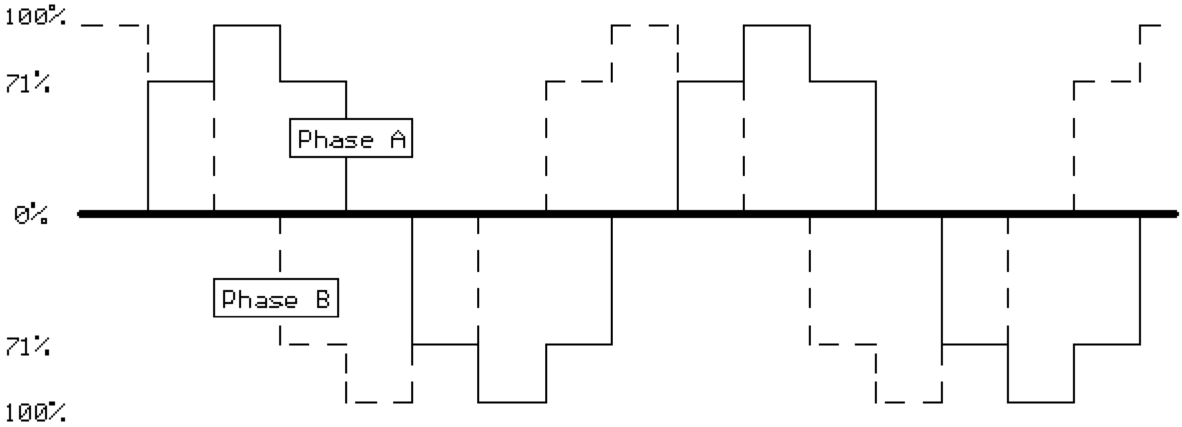


<u>1/2 – Step</u>

	Hold Current 0	Hold Current 1	Decay B_0	Decay B_1	B_0	B_1	B_2	B_3	Phase B	Decay A_0	Decay A_1	A_0	A_1	A_2	A_3	Phase A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1
2	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1
3	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1
4	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1
5	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	0
6	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0
7	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	0
8	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) reqires input of the STROBE signal. Hold Current is set to 100%.

Output current waveform of 1-2 phase excitation sine wave:



1/4 – Step

	Hold Current 0	Hold Current 1	Decay B_0	Decay B_1	B_0	B_1	B_2	B_3	Phase B	Decay A_0	Decay A_1	A_0	A_1	A_2	A_3	Phase A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1
2	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	1
3	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1
4	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	1
5	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1
6	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1
7	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1
8	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1
9	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1
10	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	0
11	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0
12	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	0
13	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	0
14	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	0
15	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	0
16	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) reqires input of the STROBE signal. Hold Current is set to 100%.

1/8 – Step

	Hold Current 0	Hold Current 1	Decay B_0	Decay B_1	B_0	B_1	B_2	B_3	Phase B	Decay A_0	Decay A_1	A_0	A_1	A_2	A_3	Phase A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1
2	1	1	1	0	0	1	1	1	1	1	0	0	1	0	0	1
3	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	1
4	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	1
5	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1
6	1	1	1	0	0	1	1	0	1	1	0	0	1	0	1	1
7	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	1
8	1	1	1	0	0	1	0	0	1	1	0	0	1	1	1	1
9	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1
10	1	1	1	0	0	1	0	0	0	1	0	0	1	1	1	1
11	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1
12	1	1	1	0	0	1	1	0	0	1	0	0	1	0	1	1
13	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1
14	1	1	1	0	0	1	0	1	0	1	0	0	1	1	0	1
15	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1
16	1	1	1	0	0	1	1	1	0	1	0	0	1	0	0	1
17	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1
18	1	1	1	0	0	1	1	1	0	1	0	0	1	0	0	0
19	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	0
20	1	1	1	0	0	1	0	1	0	1	0	0	1	1	0	0
21	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0
22	1	1	1	0	0	1	1	0	0	1	0	0	1	0	1	0
23	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	0
24	1	1	1	0	0	1	0	0	0	1	0	0	1	1	1	0
25	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	0
26	1	1	1	0	0	1	0	0	1	1	0	0	1	1	1	0
27	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	0
28	1	1	1	0	0	1	1	0	1	1	0	0	1	0	1	0
29	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	0
30	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	0
31	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0
32	1	1	1	0	0	1	1	1	1	1	0	0	1	0	0	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) reqires input of the STROBE signal. Hold Current is set to 100%.

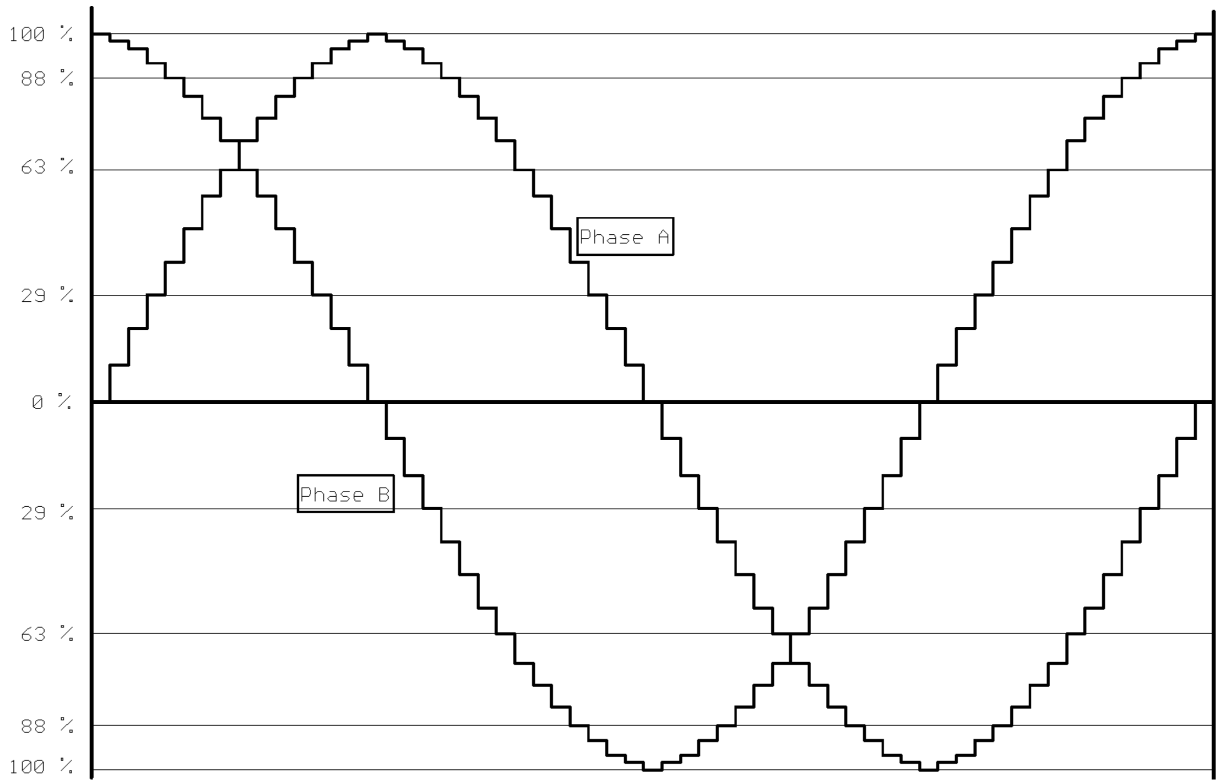
1/16 – Step

	Hold Current 0	Hold Current 1	Decay B_0	Decay B_1	B_0	B_1	B_2	B_3	Phase B	Decay A_0	Decay A_1	A_0	A_1	A_2	A_3	Phase A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1
2	1	1	1	0	1	1	1	1	1	1	0	1	0	0	0	1
3	1	1	1	0	0	1	1	1	1	1	0	0	1	0	0	1
4	1	1	1	0	1	0	1	1	1	1	0	1	1	0	0	1
5	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	1
6	1	1	1	0	1	1	0	1	1	1	0	1	0	1	0	1
7	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	1
8	1	1	1	0	1	0	0	1	1	1	0	1	1	1	0	1
9	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1
10	1	1	1	0	1	1	1	0	1	1	0	1	0	0	1	1
11	1	1	1	0	0	1	1	0	1	1	0	0	1	0	1	1
12	1	1	1	0	1	0	1	0	1	1	0	1	1	0	1	1
13	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	1
14	1	1	1	0	1	1	0	0	1	1	0	1	0	1	1	1
15	1	1	1	0	0	1	0	0	1	1	0	0	1	1	1	1
16	1	1	1	0	1	0	0	0	1	1	0	1	1	1	1	1
17	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1
18	1	1	1	0	1	0	0	0	0	1	0	1	1	1	1	1
19	1	1	1	0	0	1	0	0	0	1	0	0	1	1	1	1
20	1	1	1	0	1	1	0	0	0	1	0	1	0	1	1	1
21	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1
22	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	1
23	1	1	1	0	0	1	1	0	0	1	0	0	1	0	1	1
24	1	1	1	0	1	1	1	0	0	1	0	1	0	0	1	1
25	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1
26	1	1	1	0	1	0	0	1	0	1	0	1	1	1	0	1
27	1	1	1	0	0	1	0	1	0	1	0	0	1	1	0	1
28	1	1	1	0	1	1	0	1	0	1	0	1	0	1	0	1
29	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1
30	1	1	1	0	1	0	1	1	0	1	0	1	1	0	0	1
31	1	1	1	0	0	1	1	1	0	1	0	0	1	0	0	1
32	1	1	1	0	1	1	1	1	0	1	0	1	0	0	0	1
33	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1
34	1	1	1	0	1	1	1	1	0	1	0	1	0	0	0	0
35	1	1	1	0	0	1	1	1	0	1	0	0	1	0	0	0
36	1	1	1	0	1	0	1	1	0	1	0	1	1	0	0	0
37	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	0
38	1	1	1	0	1	1	0	1	0	1	0	1	0	1	0	0
39	1	1	1	0	0	1	0	1	0	1	0	0	1	1	0	0
40	1	1	1	0	1	0	0	1	0	1	0	1	1	1	0	0
41	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0
42	1	1	1	0	1	1	1	0	0	1	0	1	0	0	1	0
43	1	1	1	0	0	1	1	0	0	1	0	0	1	0	1	0
44	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	0
45	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	0
46	1	1	1	0	1	1	0	0	0	1	0	1	0	1	1	0

47	1	1	1	0	0	1	0	0	0	1	0	0	1	1	1	0
48	1	1	1	0	1	0	0	0	0	1	0	1	1	1	1	0
49	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	0
50	1	1	1	0	1	0	0	0	1	1	0	1	1	1	1	0
51	1	1	1	0	0	1	0	0	1	1	0	0	1	1	1	0
52	1	1	1	0	1	1	0	0	1	1	0	1	0	1	1	0
53	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	0
54	1	1	1	0	1	0	1	0	1	1	0	1	1	0	1	0
55	1	1	1	0	0	1	1	0	1	1	0	0	1	0	1	0
56	1	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0
57	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	0
58	1	1	1	0	1	0	0	1	1	1	0	1	1	1	0	0
59	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	0
60	1	1	1	0	1	1	0	1	1	1	0	1	0	1	0	0
61	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0
62	1	1	1	0	1	0	1	1	1	1	0	1	1	0	0	0
63	1	1	1	0	0	1	1	1	1	1	0	0	1	0	0	0
64	1	1	1	0	1	1	1	1	1	1	0	1	0	0	0	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) reqires input of the STROBE signal. Hold Current is set to 100%.

Output current waveform of pseudo sine wave:



Electrical Characteristics:

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Voltage	High	$V_{IN (H)}$	CLK, RESET\, STROBE, DATA Pins	2.0	V_{DD}	V_{DD} +0.4	V
Input Voltage	Low	$V_{IN (L)}$	CLK, RESET\, STROBE, DATA Pins	GND - 0.4	GND	0.8	V
Input Current 1		$I_{IN1 (H)}$	CLK, STROBE, DATA Pins	-	-	1.0	µA
Input Current 1		$I_{IN1 (L)}$	CLK, STROBE, DATA Pins	-	-	1.0	µA
Input Current 2		$I_{IN2 (H)}$	RESET\, (SETUP H)	-	-	700	µA
Input Current 2		$I_{IN2 (L)}$	RESET\, (SETUP H)	-	-	700	µA
Power Dissipation (V_{DD} pin)		$I_{DD\ 1}$	V_{DD}=5V (STROBE, RESET\, DATA = L) logic, output all off	-	3.0	6.0	mA
Power Dissipation (V_{DD} pin)		$I_{DD\ 2}$	Output open, f_{CLK}=6.25MHz Logic active, V_{DD}=5V Charge pump=charged	-	4.0	80	mA
Power Dissipation (V_M pin)		IM 1	Output open (STROBE, RESET\, DAT = L) Logic, output all off Charge pump = no operation	-	5.0	6.0	mA
Power Dissipation (V_M pin)		IM 2	Output open, f_{CLK} = 6.25 MHz, logic active, V_{DD}=5V, V_M=24V,output off Charge pump=charged	-	12	20	mA
Power Dissipation (V_M pin)		IM 3	Output open, f_{CLK} = 6.25 MHz, logic active, 100kHz chopping, output open, charge pump=charged, Ccp1=0.22µF, Ccp2=0.01µF	-	30	40	mA
Output Standby Current	Upper	I_{OH}	V_{RS}=V_M=24V, V_{Out}=0V, RESET\=H, DATA all L	-400	-	-	µA
Output Bias Current	Upper	I_{OB}	V_{RS}=V_M=24V, V_{Out}=24V, RESET\=H, DATA all L	-200			µA
Output Leakage Current	Lower	I_{OL}	V_{RS}=V_M=Ccp A=V_{OUT}=24V, RESET\ = L	-	-	1.0	µA
Comparator Referece Voltage Ratio	High	$V_{RS (H)}$	V_{ref}=3.0 V, Hold Current=(H.H)=100%	-	100	-	%
Comparator Referece Voltage Ratio	Mid High	$V_{RS (MH)}$	V_{ref}=3.0 V, Hold Current =(H.L)=85%	83	85	87	%
Comparator Referece Voltage Ratio	Mid low	$V_{RS (ML)}$	V_{ref}=3.0 V, Hold Current =(L.H)=70%	68	70	72	%
Comparator Referece Voltage Ratio	Low	$V_{RS (L)}$	V_{ref}=3.0 V, Hold Current =(L.L)=50%	48	50	52	%

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output current differential	ΔI_{Out1}	Differences between output current channels I_{Out} = 1000mA	-5	-	5	%
Output current setting differential	ΔI_{Out2}	I_{Out}=1000mA	-5	-	5	%
RS pin current	IRS	V_{RS}=24V, V_M=24V, RESET\=L (reset status)	-	-	10	μA
Output transistor drain-source on-resistance	$R_{ON\ (D\text{-}S)\ 1}$	I_{Out}=1.0A, V_{DD}=5V, T_j=25°C,Drain-Source	-	0.5	0.6	Ω
	$R_{ON\ (D\text{-}S)\ 1}$	I_{Out}=1.0A, V_{DD}=5V, T_j=25°C,Source-Drain	-	0.5	0.6	
	$R_{ON\ (D\text{-}S)\ 2}$	I_{Out}=1.0A, V_{DD}=5V, T_j=105°C,Drain-Source	-	0.5	0.75	
	$R_{ON\ (D\text{-}S)\ 2}$	I_{Out}=1.0A, V_{DD}=5V, T_j=105°C,Source-Drain	-	0.5	0.75	
V_{ref} input voltage	V_{ref}	V_M=24V, V_{DD}=5V, RESET\=H output on	2.0	-	V_{DD}	V
V_{ref} input current	I_{ref}	RESET\=H, output off, V_M=24V, V_{DD}=5V V_{ref}=3.0V	0	-	100	μA
TSD temperature	T_jTSD	V_M=24V, V_{DD}=5V	130	-	170	°C
TSD return temperature difference	ΔT_jTSD	T_jTSD=130 to 170°C	-	T_j TSD -35		°C
V_{DD} return voltage	V_{DDR}	V_M=24V, RESET\=H, STROBE=H	2.0	-	4.0	V
V_M return voltage	V_{MR}	V_{DD}=5V, RESET\=H, STROBE=H	2.0	-	4.0	V
Over current protected circuit operation current	I_{SD}	V_{DD}=5V, V_M=24V, f_{chop}=100 kHz set	-	2.6	-	A

AC Characteristics:

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Clock frequency	f_{CLK}	-	1.0	-	25	MHz
Minimum clock pulse width	$t_{w(clk)}$	-	40	-	-	ns
	$t_{wp(clk)}$	-	20	-	-	
	$t_{wn(clk)}$	-	20	-	-	
Minimum STROBE pulse width	t_{STROBE}	-	40	-	-	ns
	$t_{STROBE\ (H)}$	-	20	-	-	
	$t_{STROBE\ (L)}$	-	20	-	-	
Data setup time	t_{su}SIN-CLK	-	20	-	-	ns
	t_{su}ST-CLK	-	20	-	-	
Data hold time	t_hSIN-CLK	-	20	-	-	ns
	t_hCLK-ST	-	20	-	-	
Output transistor switching characteristics	t_r	Output load 6.8mH/5.7Ω	-	0.1	-	μs
	t_f		-	0.1	-	
	$t_{pLH\ (ST)}$	STROBE (L ⇒ H) to V_{Out} Output load 6.8mH/5.7Ω	-	15	-	
	$t_{pHL\ (ST)}$		-	10	-	
	$t_{pLH\ (CR)}$	CR to V_{Out} Output load 6.8mH/5.7Ω	-	1.2	-	
	$t_{pHL\ (CR)}$		-	2.5	-	
Noise rejection dead band time	t_{BLNK}	I_{out}=1.0A	200	300	400	ns
CR reference signal oscillation frequency	f_{CR}	C_{osc}=560pF, R_{osc}=3.6kΩ	-	736	-	kHz
Chopping frequency range	$f_{chop\ (min)}$ $f_{chop\ (typ)}$ $f_{chop\ (max)}$	Output active (I_{out}=1.0A) Step fixed, Ccp1=0.22μF, Ccp2=0.01μF	40	100	150	kHz
Chopping frequency	f_{chop}	Output active (I_{out}=1.0A)	-	100	-	kHz
Charge pump rise time	t_{ONG}	Ccp2=0.22μF, Ccp=0.01μF V_M=24V, V_{DD}=5V Reset\ = L ⇒ H	-	2	4	ms

Package Dimensions :

Unit: mm

HSOP36-P-450-0.65