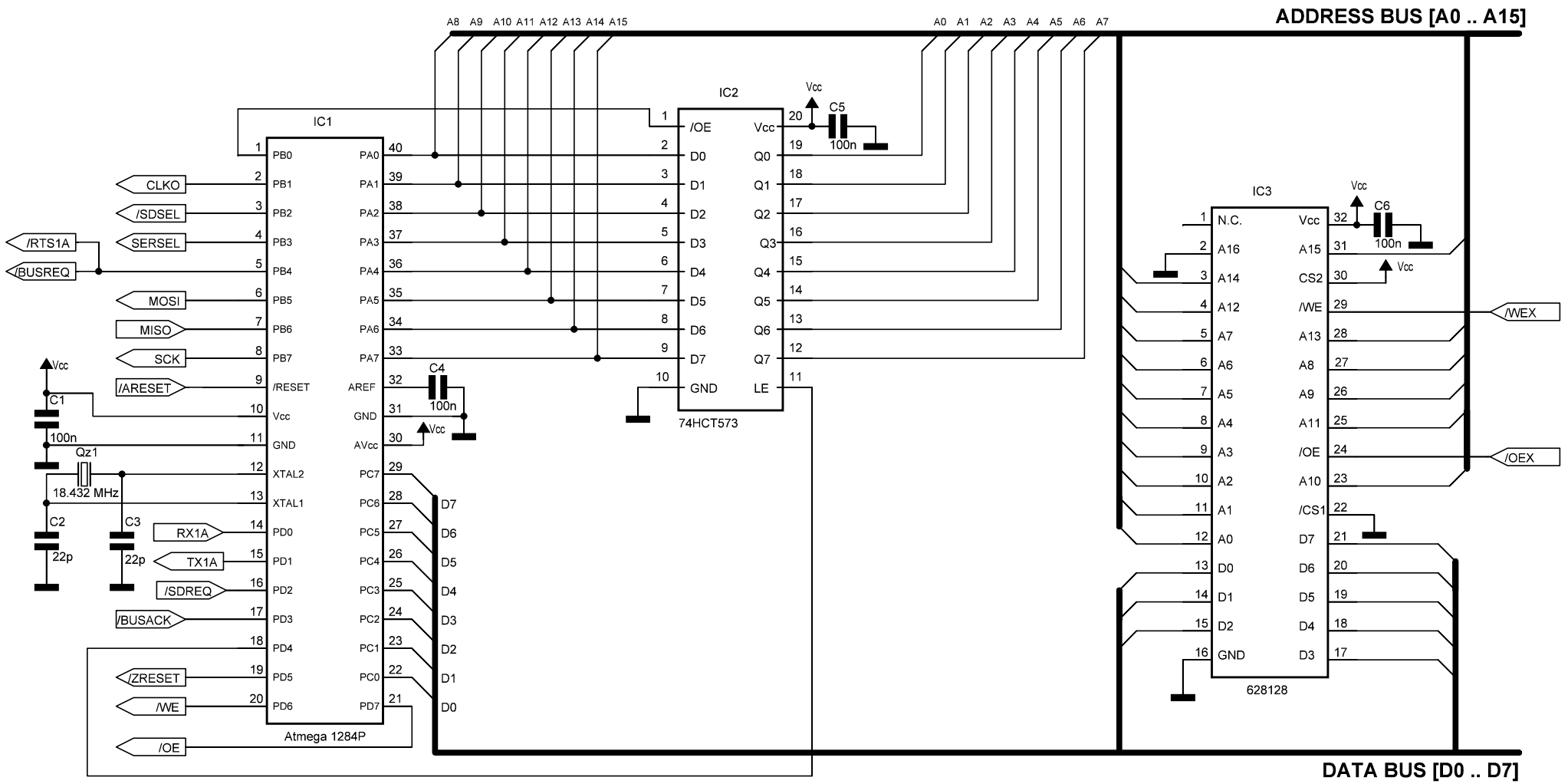

Notes:

1) The Fuse Bit CKOUT must be set so the Atmega will output its clock at pin B1.
2) The JTAGEN must be disabled, JTAG pins used for normal I/O
3) recommended Fuse settings (Low, High, Extended): BF, D9, FF
4) PB4 has dual usage: /RTS while the Atmega is in control, /BUSREQ otherwise

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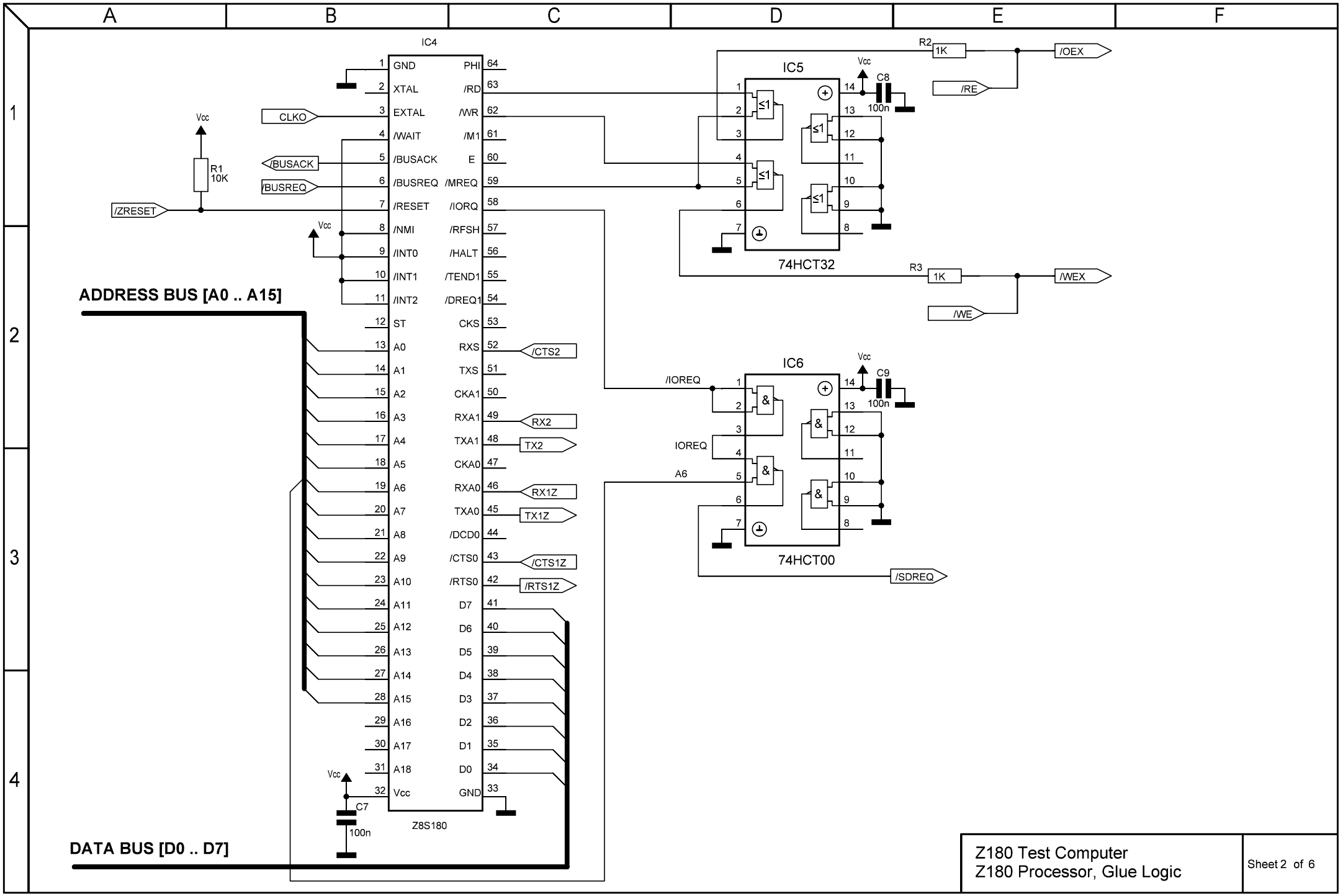
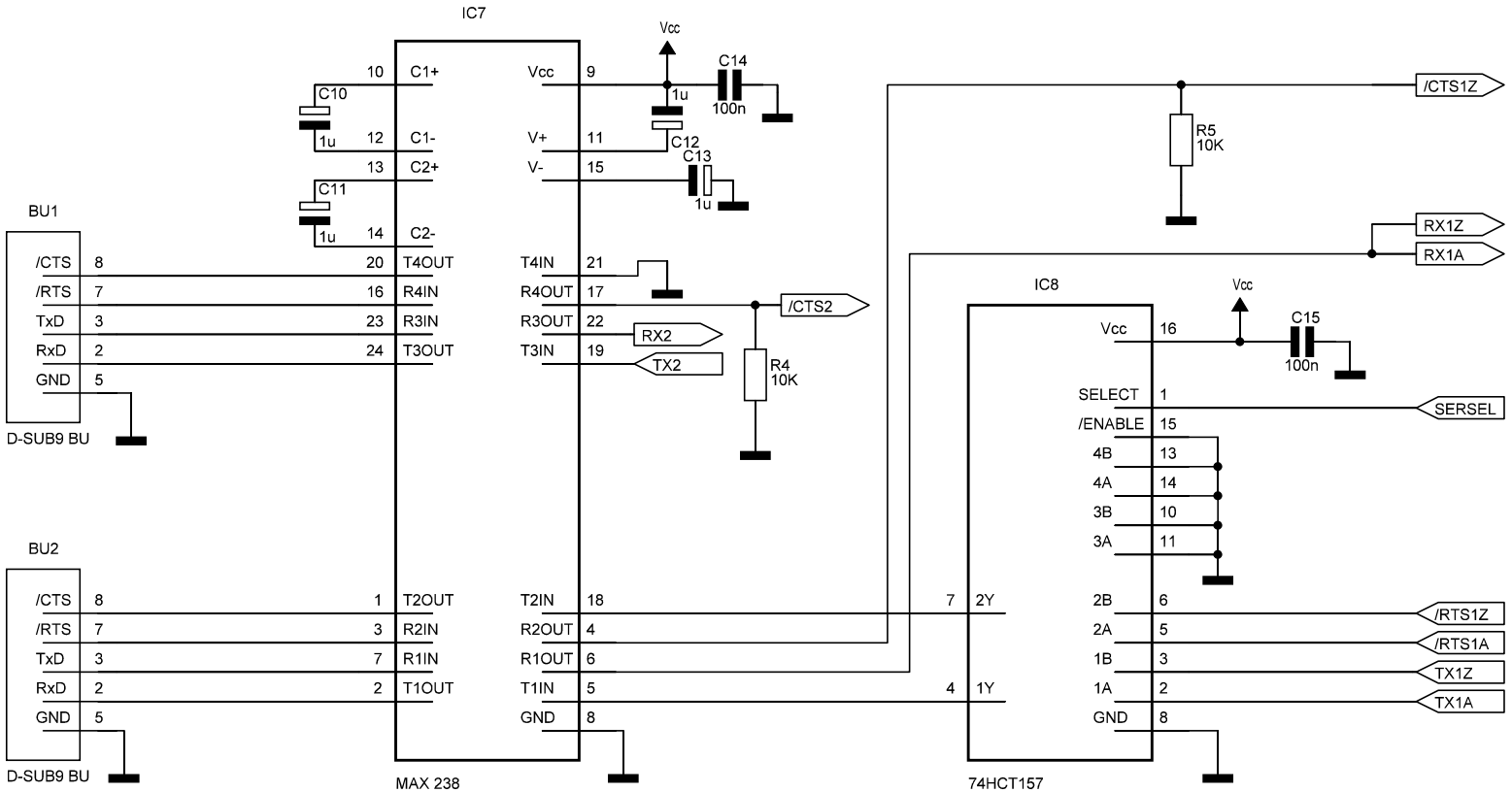
Z180 Test Computer
Atmega Control Processor, SRAM

Sheet 1 of 6

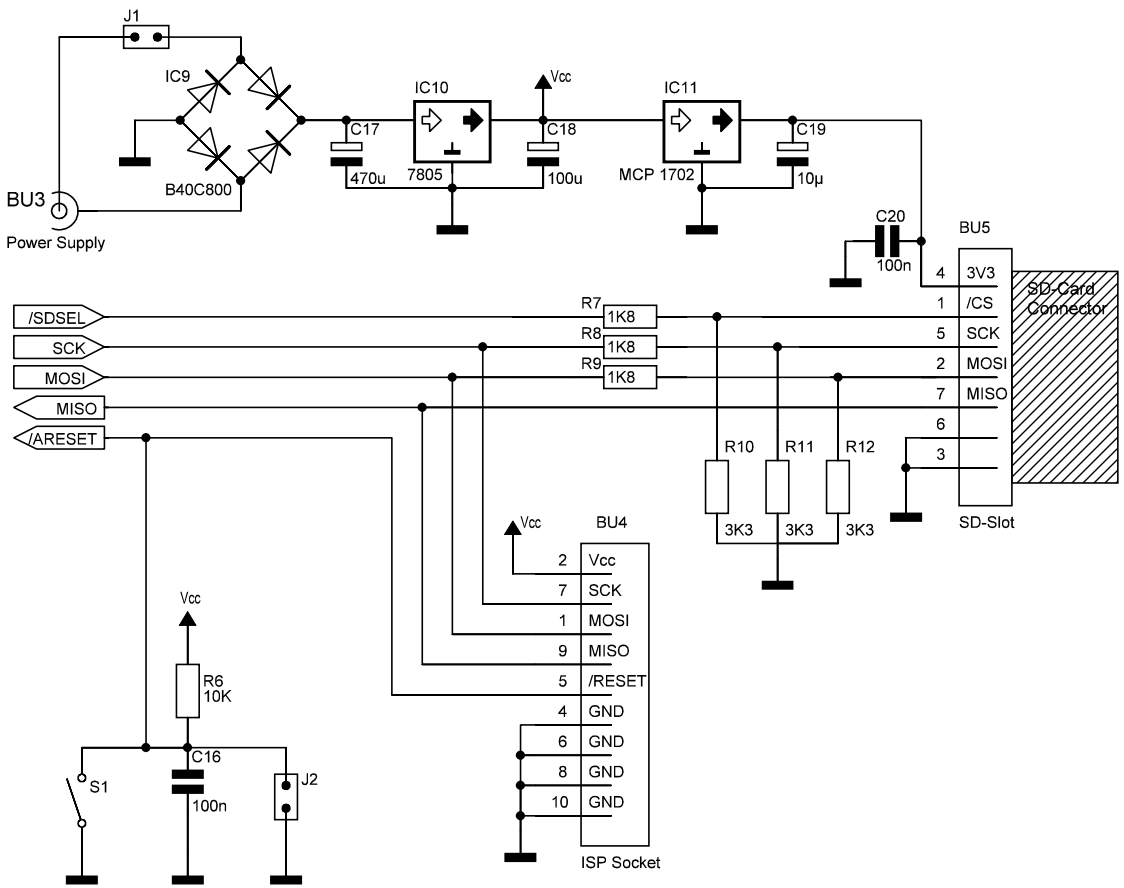

A
B
C
D
E
F
1
2
3
4
IC4
GND
XTAL
EXTAL
/WAIT
/BUSACK
/BUSREQ
/RESET
/NMI
/INT0
/INT1
/INT2
ST
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
Vcc
PHI
/RD
/WR
/M1
E
/MREQ
/IORQ
/RFSH
/HALT
/TEND1
/DREQ1
CKS
RXS
TXS
CKA1
RXA1
TXA1
CKA0
RXA0
TXA0
/DCD0
/CTS0
/RTS0
D7
D6
D5
D4
D3
D2
D1
D0
GND
Z8S180
CLKO
/BUSACK
/BUSREQ
/ZRESET
/CTS2
RX2
TX2
RX1Z
TX1Z
/CTS1Z
/RTS1Z
Vcc
R1
10K
C7
100n
ADDRESS BUS [A0 .. A15]
DATA BUS [D0 .. D7]
IC5
74HCT32
R2
1K
/OEX
/RE
C8
100n
R3
1K
/WEX
/WE
IC6
74HCT00
/IOREQ
IOREQ
A6
/SDREQ
C9
100n
Z180 Test Computer
Z180 Processor, Glue Logic
Sheet 2 of 6



Notes:

1) The capacitor at the V- pin of the MAX must be connected with its + pin to GND.
   This is intentional, no drawing mistake.
2) For the signal names of the serial interface #1 A at the last position indicates
   the Atmega, Z indicates the Z180

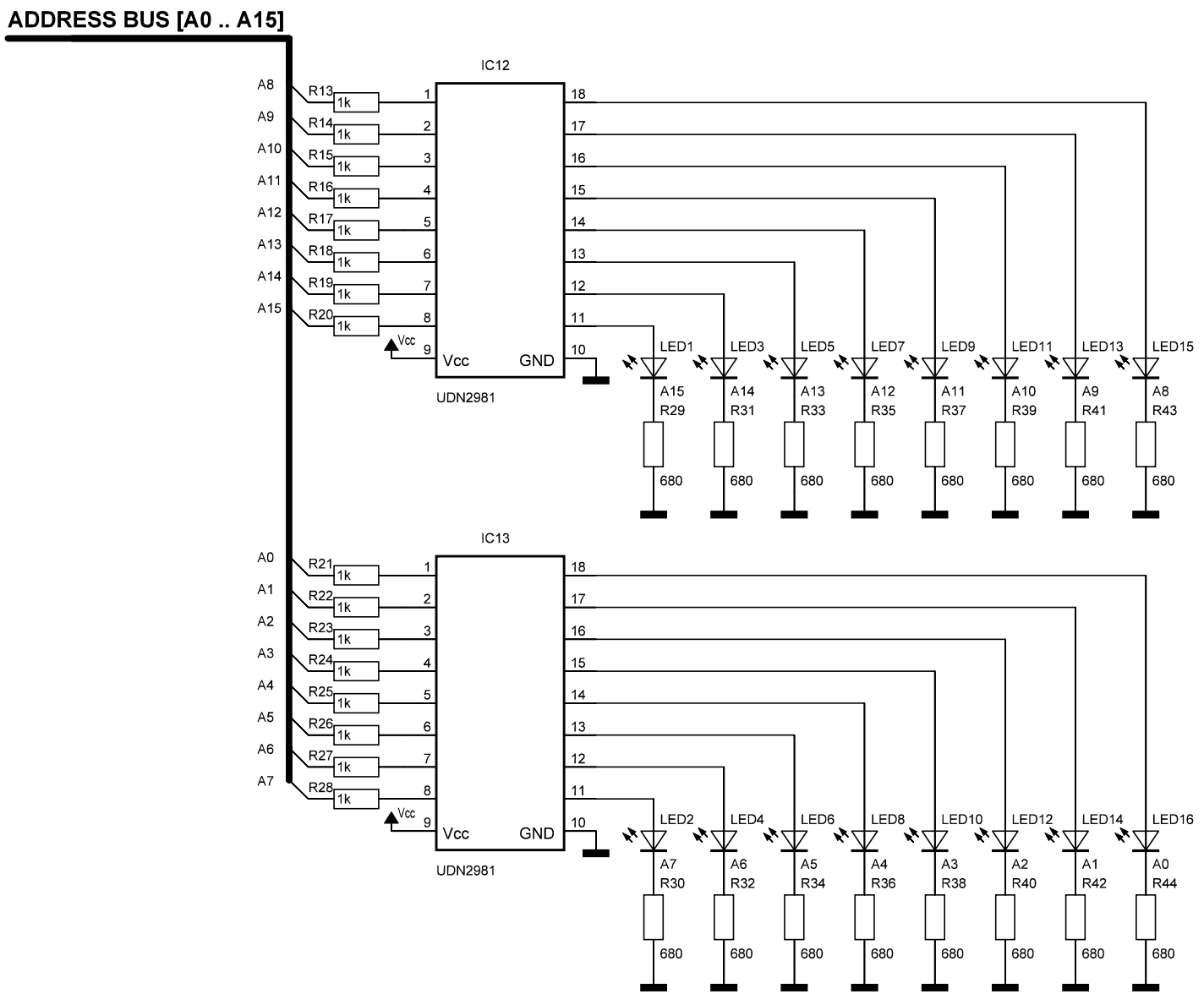
Z180 Test Computer Serial Interfaces	Sheet 3 of 6



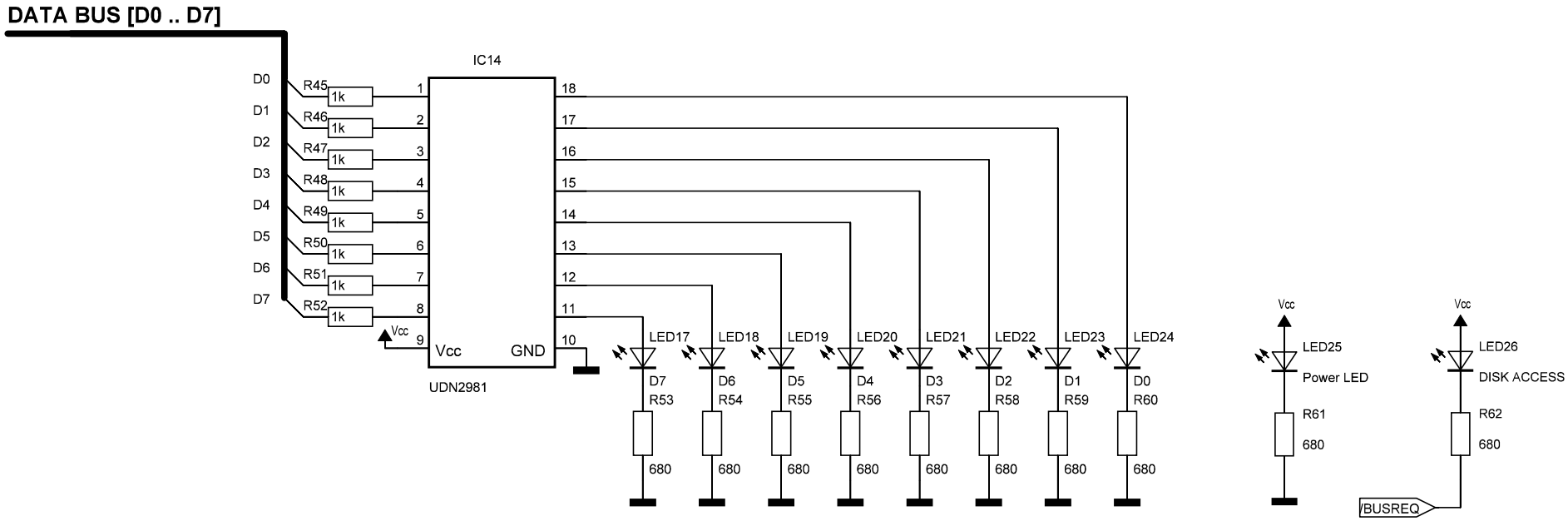
Notes:

1) Jumper J1 to be either closed or connected to external On/Off switch.
2) Jumper J2 to bei either left open or connected to external reset button.

Z180 Test Computer Power Supply, SD-Card Interface	Sheet 4 of 6



Z180 Test Computer Address Bus LED Indicators	Sheet 5 of 6



Z180 Test Computer Data Bus & misc. LED Indicators	Sheet 6 of 6