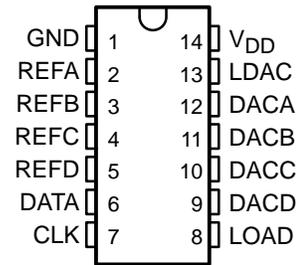


TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081C – NOVEMBER 1994 – REVISED FEBRUARY 1996

- Four 8-Bit Voltage Output DACs
- 5-V Single-Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable 1 or 2 Times Output Range
- Simultaneous-Update Facility
- Internal Power-On Reset
- Low Power Consumption
- Half-Buffered Output

N OR D PACKAGE
(TOP VIEW)



applications

- Programmable Voltage Sources
- Digitally-Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

description

The TLC5620C and TLC5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5620C and TLC5620I are over a simple 3-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises 8 bits of data, 2 DAC select bits and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs are updated simultaneously through control of the LDAC terminal. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-terminal small-outline (D) package allows digital control of analog functions in space-critical applications. The TLC5620C is characterized for operation from 0°C to 70°C. The TLC5620I is characterized for operation from -40°C to 85°C. The TLC5620C and TLC5620I do not require external trimming.

AVAILABLE OPTIONS

PACKAGE		
T _A	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLC5620CD	TLC5620CN
-40°C to 85°C	TLC5620ID	TLC5620IN



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

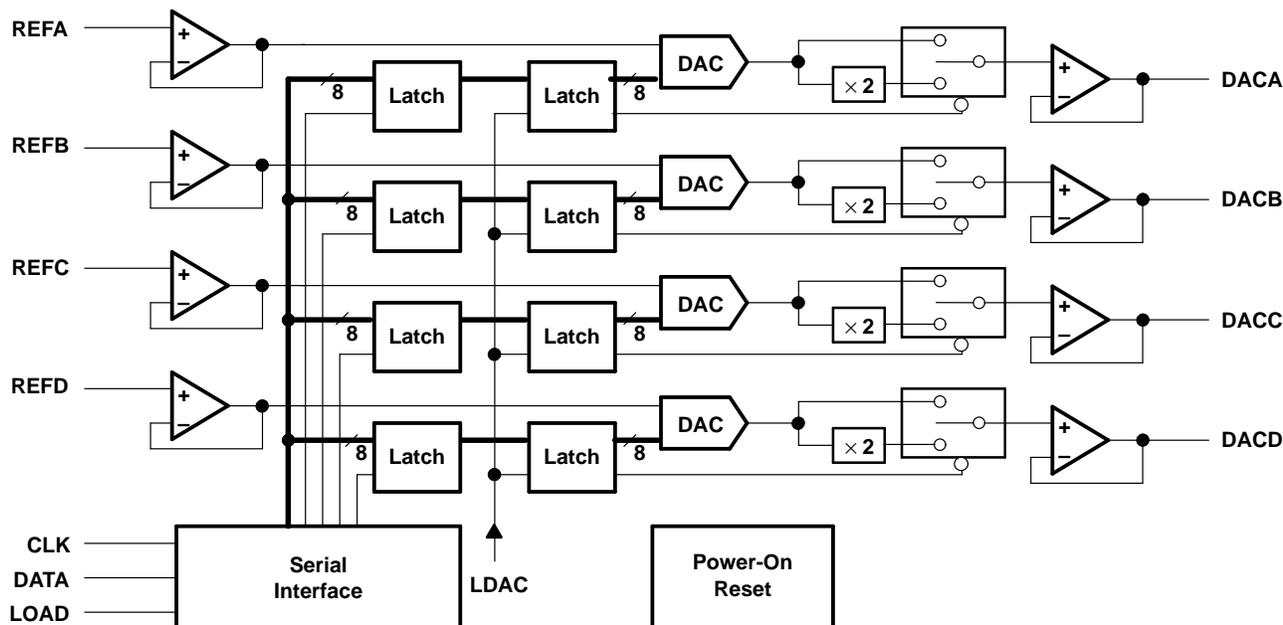
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TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	7	I	Serial interface clock, data enters on the negative edge
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial-interface digital-data input
GND	1	I	Ground return and reference terminal
LDAC	13	I	DAC-update latch control
LOAD	8	I	Serial interface load control
REFA	2	I	Reference voltage input to DACA
REFB	3	I	Reference voltage input to DACB
REFC	4	I	Reference voltage input to DACC
REFD	5	I	Reference voltage input to DACD
VDD	14	I	Positive supply voltage

detailed description

The TLC5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 2. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always present a high-impedance load to the reference source.



detailed description (continued)

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain.

On powerup, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is 0 or 1 within the serial control word.

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated and LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered most significant bit (MSB) first. Data transfers using two 8-clock cycle periods are shown in Figures 3 and 4.

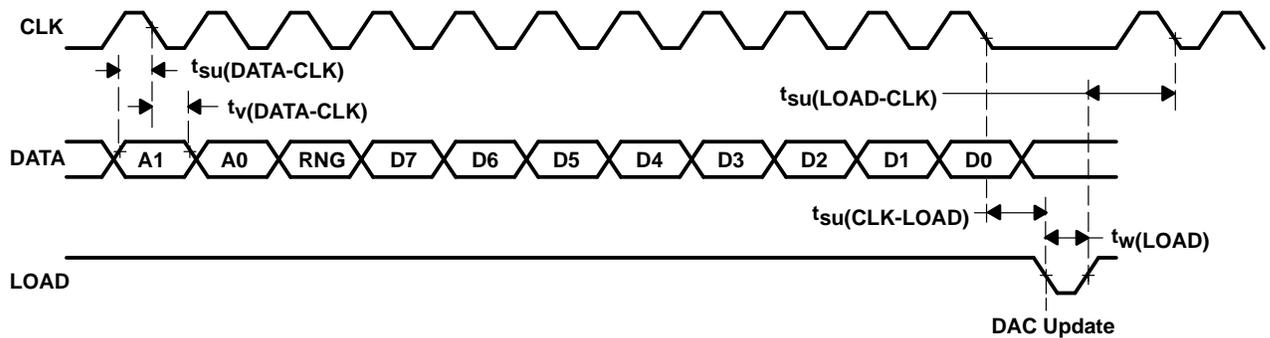


Figure 1. LOAD-Controlled Update (LDAC = Low)

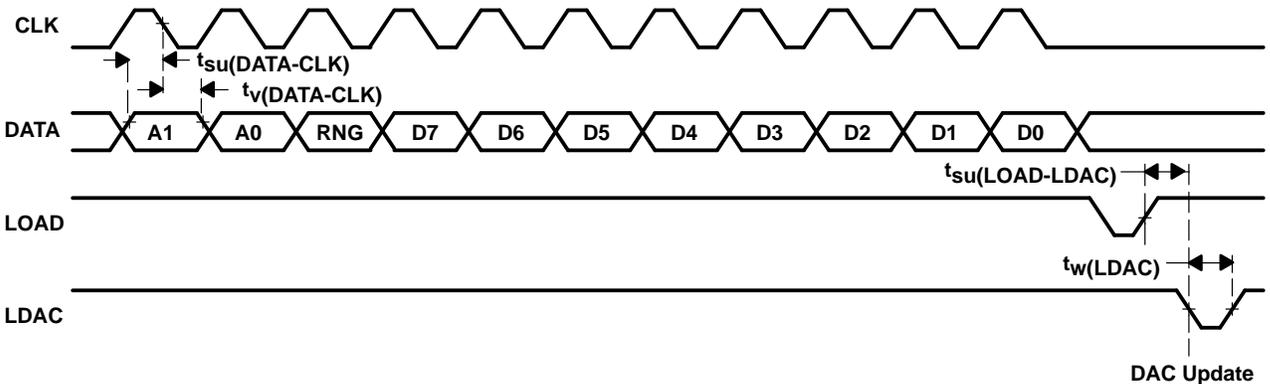


Figure 2. LDAC-Controlled Update

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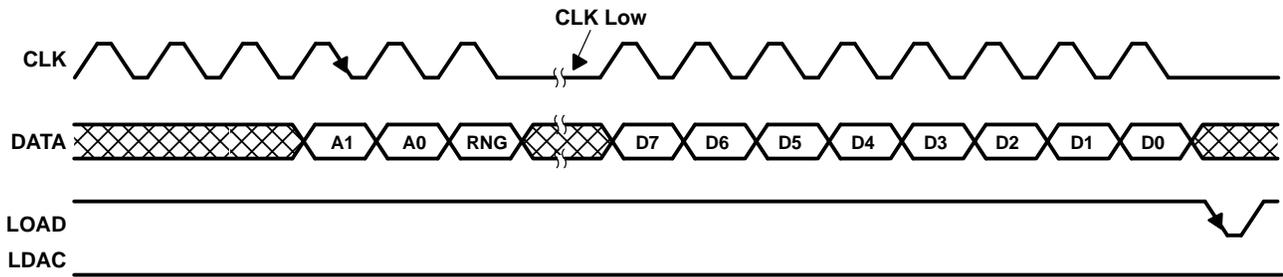


Figure 3. Load-Controlled Update Using 8-Bit Serial Word (LDAC = Low)

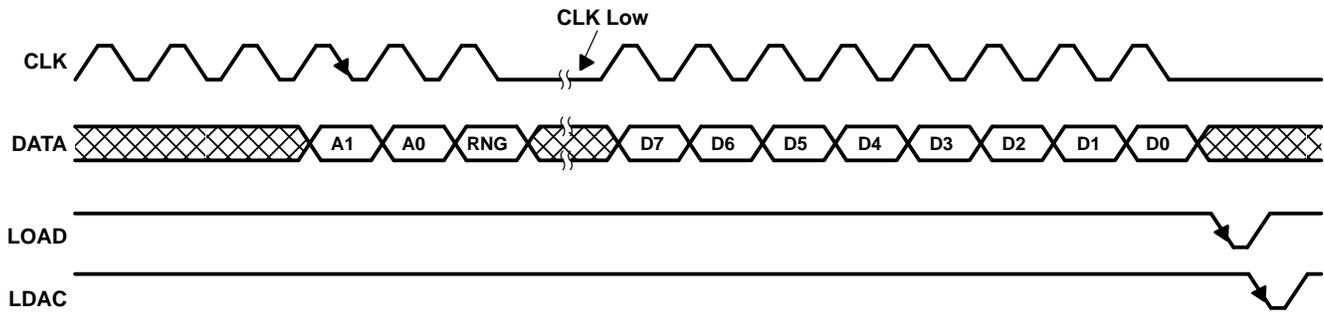


Figure 4. LDAC-Controlled Update Using 8-Bit Serial Word



TLC5620C, TLC5620I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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data interface (continued)

Table 1 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 1. Serial Input Decode

A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

Table 2. Ideal Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	$(1/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$(127/256) \times \text{REF} (1+\text{RNG})$
1	0	0	0	0	0	0	0	$(128/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	$(255/256) \times \text{REF} (1+\text{RNG})$



TLC5620C, TLC5620I

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linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, with a negative voltage offset, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive to a negative voltage.

So when the output offset voltage is negative, the output voltage remains at 0 V until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in the transfer function shown in Figure 5.

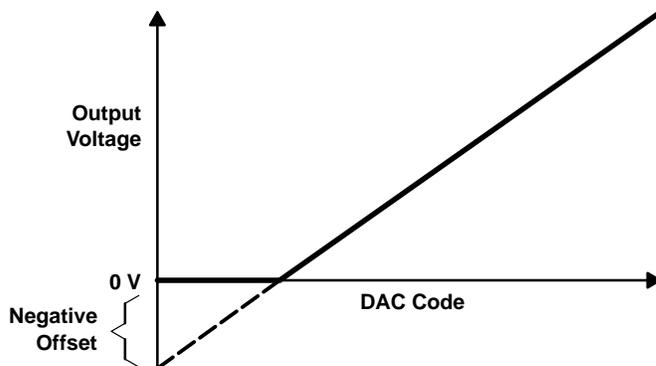


Figure 5. Effect of Negative Offset (Single Supply)

This negative offset error, not the linearity error, produces the breakpoint. The transfer function would have followed the dotted line if the output buffer could drive to a negative voltage.

For a DAC, linearity is measured between the zero-input code (all inputs are 0) and the full-scale code (all inputs are 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full-scale code and the lowest code which produces a positive output voltage.

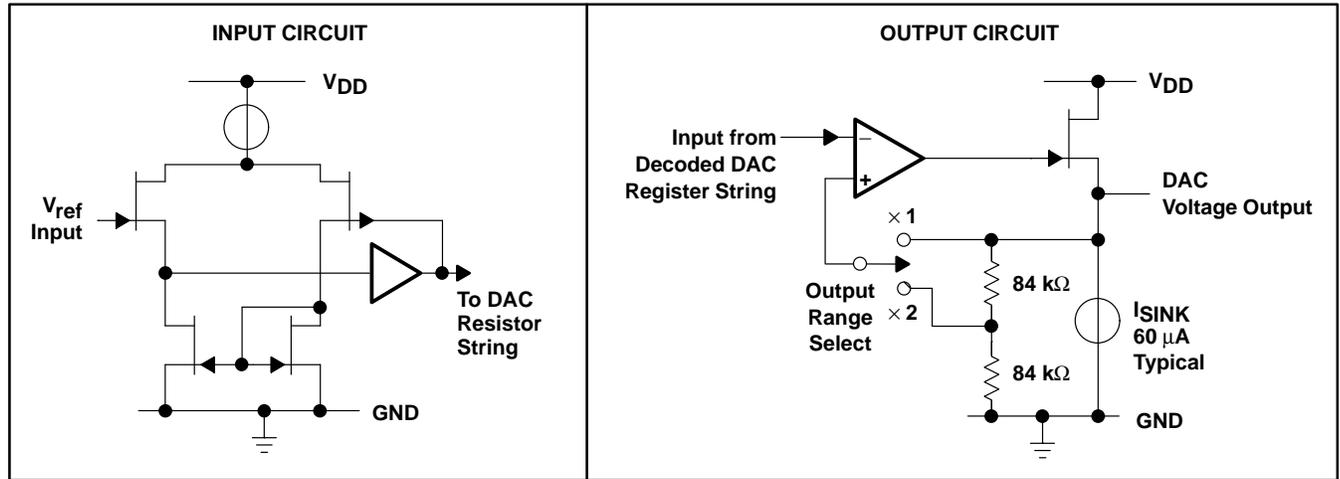
The code is calculated from the maximum specification for the negative offset.



TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ($V_{DD} - GND$)	7 V
Digital input voltage range	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Reference input voltage range, V_{ID}	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Operating free-air temperature range, T_A : TLC5620C	$0^\circ C$ to $70^\circ C$
TLC5620I	$-40^\circ C$ to $85^\circ C$
Storage temperature range, T_{stg}	$-50^\circ C$ to $150^\circ C$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$230^\circ C$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75		5.25	V
High-level digital input voltage, V_{IH}	$0.8 V_{DD}$			V
Low-level digital input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref} [A B C D]			$V_{DD} - 1.5$	V
Analog full-scale output voltage, $R_L = 10 k\Omega$		3.5		V
Load resistance, R_L	10			$k\Omega$
Setup time, data input, $t_{su}(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Valid time, data input valid after $CLK\downarrow$, $t_v(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Setup time, CLK eleventh falling edge to $LOAD$, $t_{su}(CLK-LOAD)$ (see Figure 1)	50			ns
Setup time, $LOAD\uparrow$ to $CLK\downarrow$, $t_{su}(LOAD-CLK)$ (see Figure 1)	50			ns
Pulse duration, $LOAD$, $t_w(LOAD)$ (see Figure 1)	250			ns
Pulse duration, $LDAC$, $t_w(LDAC)$ (see Figure 2)	250			ns
Setup time, $LOAD\uparrow$ to $LDAC\downarrow$, $t_{su}(LOAD-LDAC)$ (see Figure 2)	0			ns
CLK frequency			1	MHz
Operating free-air temperature, T_A	TLC5620C	0	70	$^\circ C$
	TLC5620I	-40	85	$^\circ C$



TLC5620C, TLC5620I

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref} = 2\text{ V}$, $\times 1$ gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			± 10	μA
I_{IL}	Low-level digital input current	$V_I = 0\text{ V}$			± 10	μA
$I_{O(sink)}$	Output sink current	Each DAC output	20			μA
$I_{O(source)}$	Output source current		2			mA
C_i	Input capacitance			15		pF
	Reference input capacitance			15		
I_{DD}	Supply current	$V_{DD} = 5\text{ V}$			2	mA
I_{ref}	Reference input current	$V_{DD} = 5\text{ V}$, $V_{ref} = 2\text{ V}$			± 10	μA
E_L	Linearity error (end point corrected)	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 1)			± 1	LSB
E_D	Differential-linearity error	$V_{ref} = 2\text{ V}$, $\times 1$ gain (see Note 2)			± 0.9	LSB
E_{ZS}	Zero-scale error	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 3)	0		30	mV
	Zero-scale-error temperature coefficient	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 4)		10		$\mu\text{V}/^\circ\text{C}$
E_{FS}	Full-scale error	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 5)			± 60	mV
	Full-scale-error temperature coefficient	$V_{ref} = 2\text{ V}$, $\times 2$ gain (see Note 6)		± 25		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	See Notes 7 and 8		0.5		mV/V

- NOTES:
1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
 2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
 3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
 4. Zero-scale-error temperature coefficient is given by: $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 5. Full-scale error is the deviation from the ideal full-scale output ($V_{ref} - 1\text{ LSB}$) with an output load of 10 k Ω .
 6. Full-scale-temperature coefficient is given by: $FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
 7. Zero-scale-error rejection ratio (ZSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
 8. Full-scale-error rejection ratio (FSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref} = 2\text{ V}$, $\times 1$ gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$		1		$\text{V}/\mu\text{s}$
Output settling time	To 0.5 LSB, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Note 9		10		μs
Large-signal bandwidth	Measured at -3 dB point		100		kHz
Digital crosstalk	$\text{CLK} = 1\text{-MHz}$ square wave measured at DACA-DACD		-50		dB
Reference feedthrough	See Note 10		-60		dB
Channel-to-channel isolation	See Note 11		-60		dB
Reference input bandwidth	See Note 12		100		kHz

- NOTES:
9. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of 00 hex to FF hex or FF hex to 00 hex. For TLC5620C: $V_{DD} = 5\text{ V}$, $V_{ref} = 2\text{ V}$ and range = $\times 2$. For TLC5620I: $V_{DD} = 3\text{ V}$, $V_{ref} = 1.25\text{ V}$ and range $\times 2$.
 10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
 11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
 12. Reference bandwidth is the -3 dB bandwidth with an input at $V_{ref} = 1.25\text{ V}$ dc + 2 V_{pp} , with a full-scale digital-input code.



PARAMETER MEASUREMENT INFORMATION

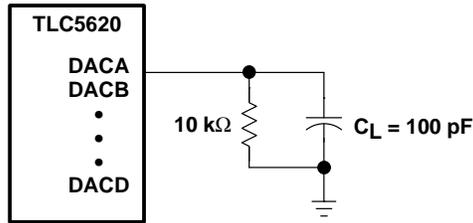


Figure 6. Slewing Settling Time and Linearity Measurements

TYPICAL CHARACTERISTICS

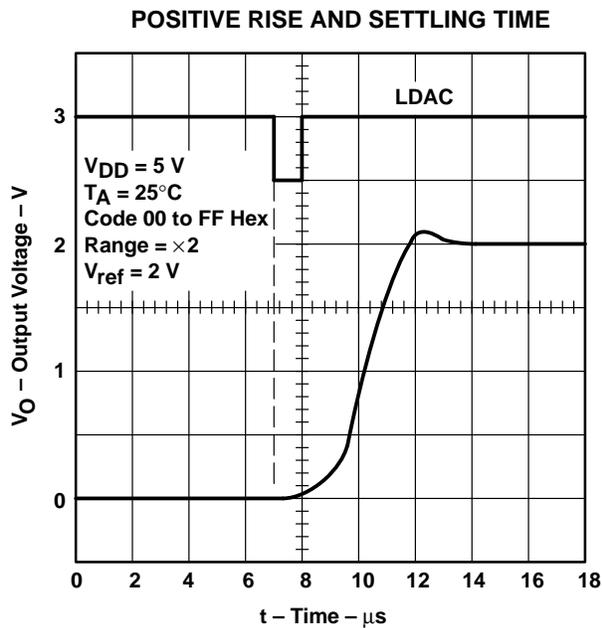


Figure 7

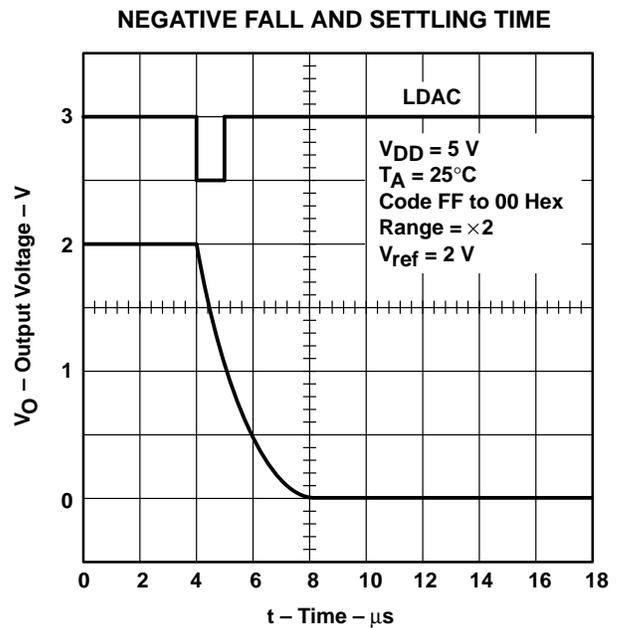


Figure 8

TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

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TYPICAL CHARACTERISTICS

**DAC OUTPUT VOLTAGE
vs
LOAD**

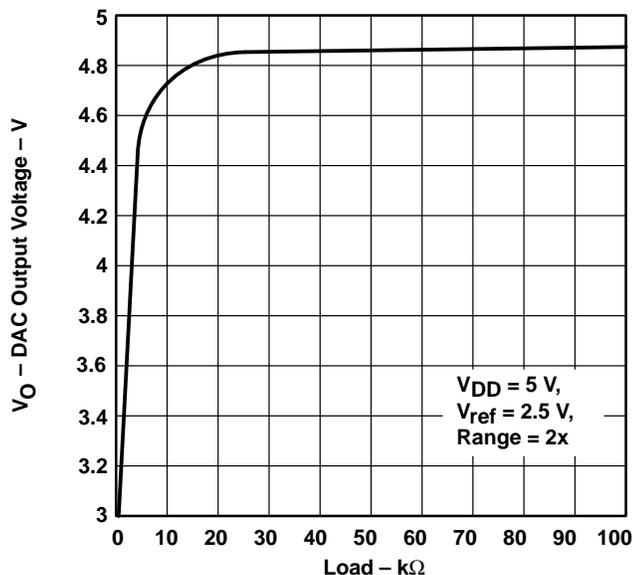


Figure 9

**DAC OUTPUT VOLTAGE
vs
LOAD**

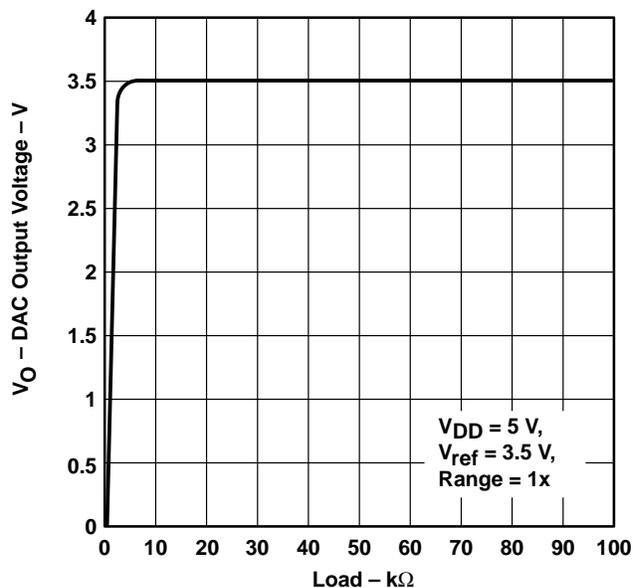


Figure 10

**OUTPUT SOURCE CURRENT
vs
OUTPUT VOLTAGE**

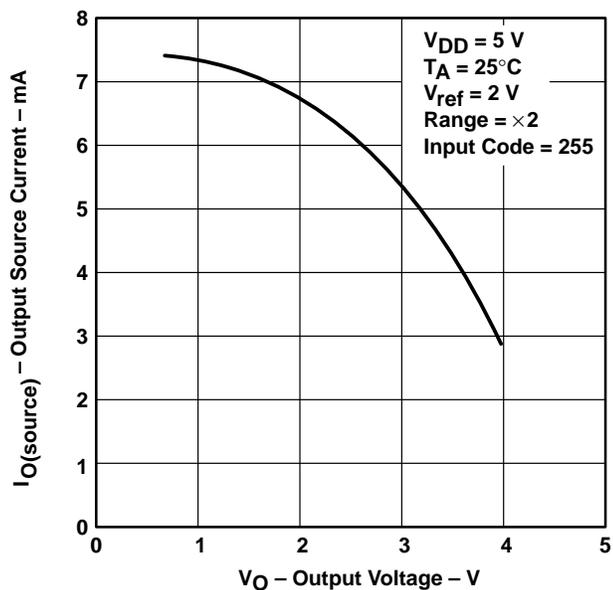


Figure 11

**SUPPLY CURRENT
vs
TEMPERATURE**

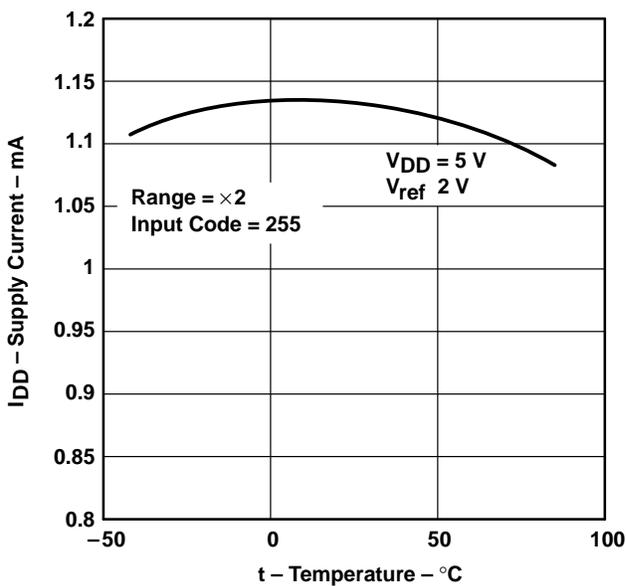


Figure 12



TYPICAL CHARACTERISTICS

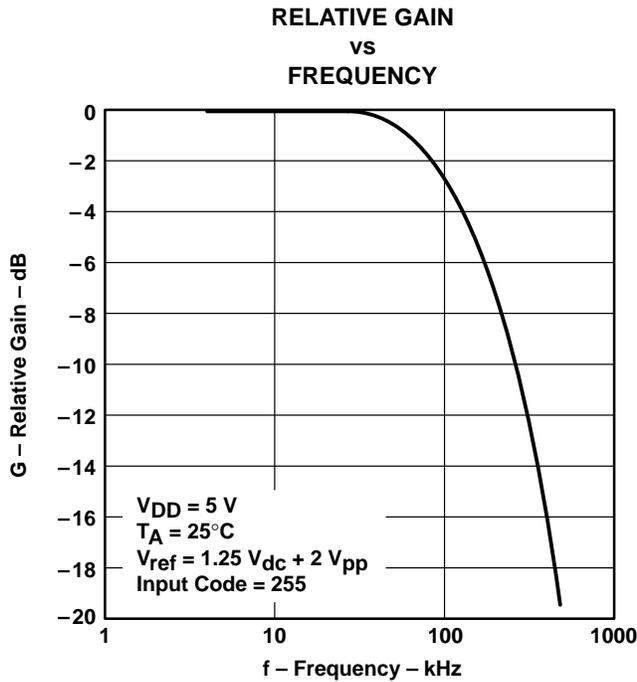


Figure 13

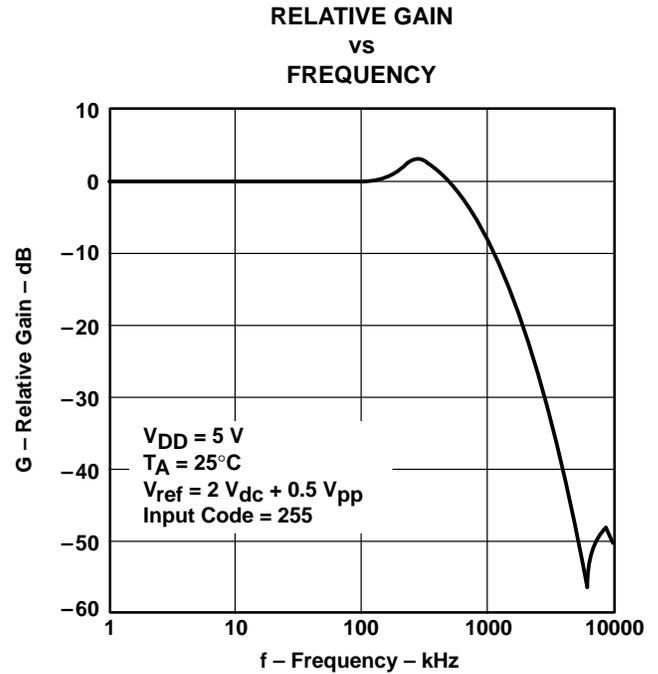
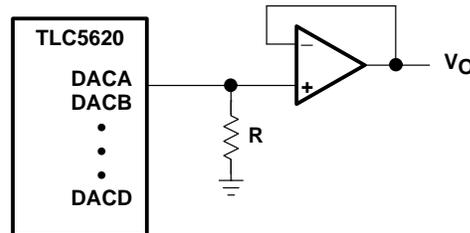


Figure 14

APPLICATION INFORMATION



NOTE A: Resistor $R \geq 10 \text{ k}\Omega$

Figure 15. Output Buffering Scheme

TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

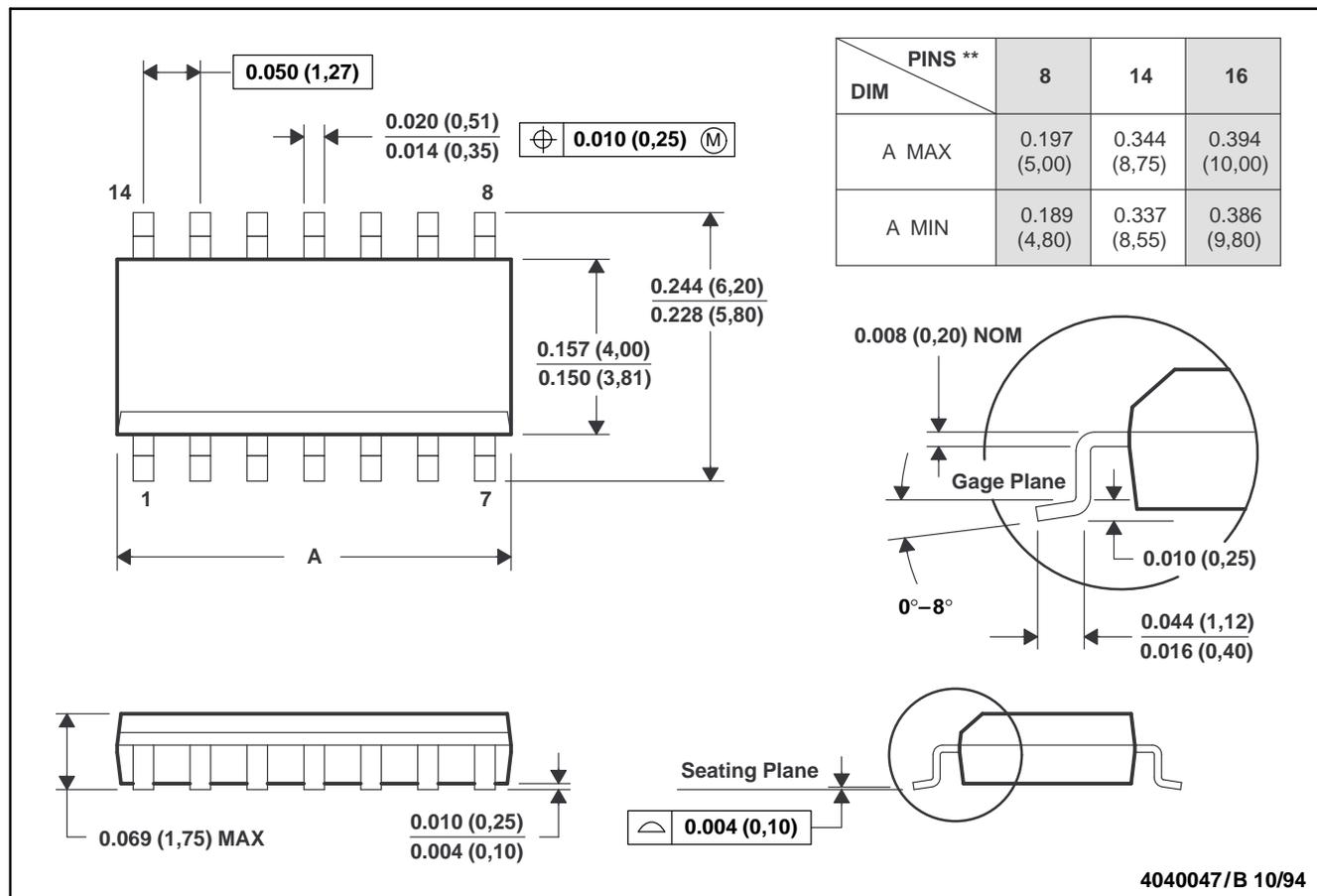
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MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Four center pins are connected to die mount pad.
 E. Falls within JEDEC MS-012



TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

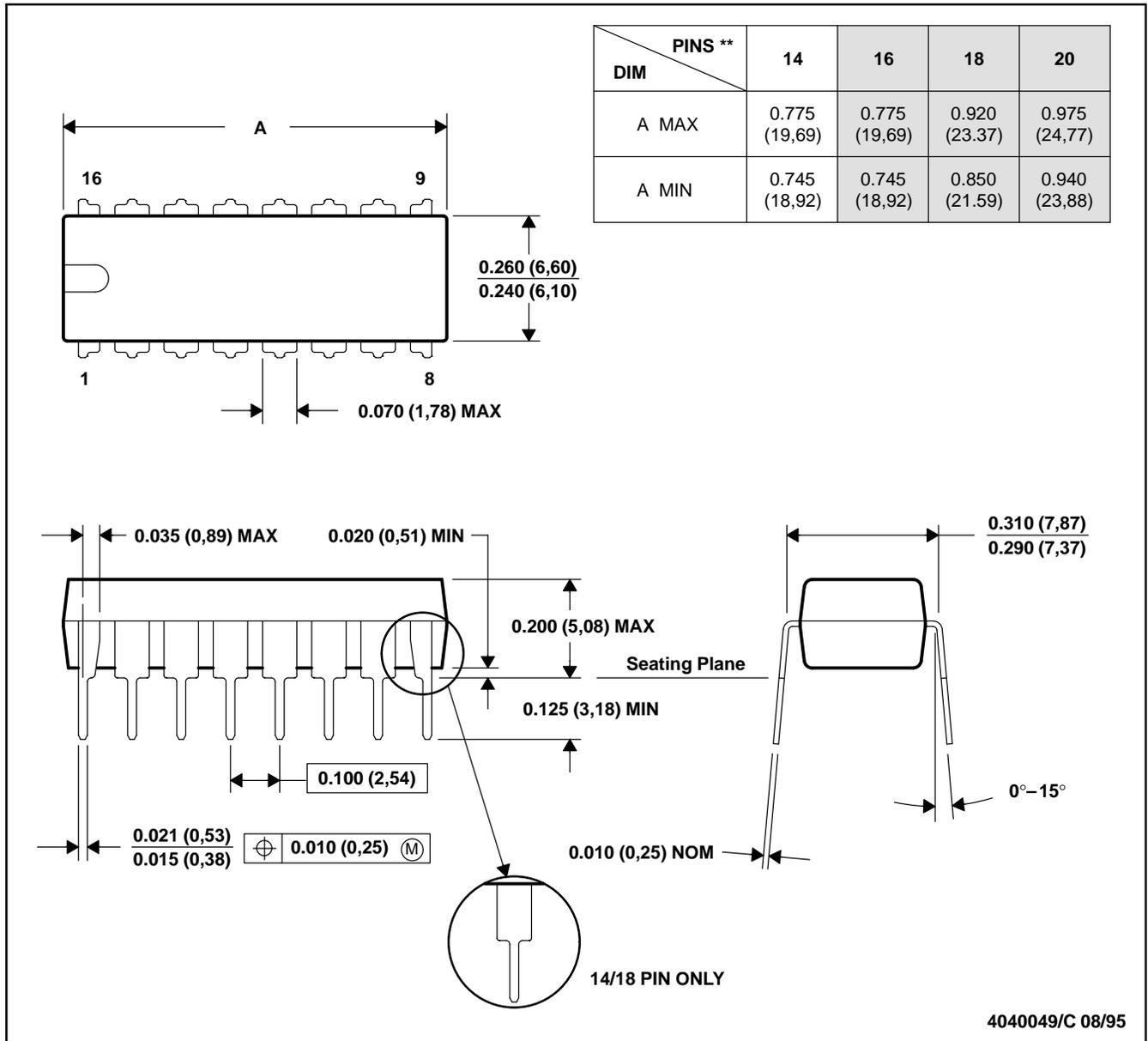
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MECHANICAL DATA

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)



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