APPLICATION NOTES
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XAPP Application Notes

- List
- Newest Application Notes NEW!
- Summaries

Get Acrobat to view the PDF files below.

Title	Size	Summary	Family	Design
Loadable Binary Counters	40 KB	XAPP004	XC3000	VIEW*logic* OrCAD
Register Based FIFO	60 KB	XAPP005	XC3000	VIEW*logic* OrCAD
Boundary Scan Emulator for XC3000	80 KB	XAPP007	XC3000	VIEW*logic* OrCAD
Complex Digital Waveform Generator	10 KB	XAPP008	FPGAs	
Harmonic Frequency Synthesizer and FSK Modulator	20 KB	XAPP009	FPGAs	VIEW*logic* OrCAD
Bus Structured Serial Input/Output Device	20 KB	XAPP010	XC4000	
LCA Speed Estimation: Asking the Right Question	10 KB	XAPP011	FPGAs	
Quadrature Phase Detector	20 KB	XAPP012	XC3000	
Using the Dedicated Carry Logic in XC4000E	100 KB	XAPP013	XC4000	
Ultra-Fast Synchronous Counters	40 KB	XAPP014	FPGAs	VIEW*logic* OrCAD
Using the XC4000 Readback Capability	60 KB	XAPP015	XC4000	
Boundary Scan in XC4000/XC5200 Devices	100 KB	XAPP017	XC4000 XC5200	
Estimating the Performance of XC4000E Adders and Counters	40 KB	XAPP018	XC4000	
Adders, Subtracters and Accumulators in XC3000	60 KB	XAPP022	XC3000	VIEW*logic* OrCAD
Accelerating Loadable Counters in XC4000	30 KB	XAPP023	XC4000	VIEW*logic* OrCAD
XC3000 Series Technical Information	110 KB	XAPP024	XC3000	
Multiplexers and Barrel Shifters in XC3000 Series	40 KB	XAPP026	XC3000	VIEW*logic* OrCAD
Implementing State Machines in FPGA Devices	30 KB	XAPP027	FPGAs	
Frequency/Phase Comparator for Phase Locked Loops	40 KB	XAPP028	FPGAs	VIEW*logic* OrCAD

Serial Code Conversion between BCD and Binary	20 KB	XAPP029	XC3000	VIEW*logic* OrCAD

Title	Size	Summary	Family	Design
Megabit FIFO in Two Chips: One LCA Device and One DRAM	20 KB	XAPP030	XC3000	
Improving XC4000 Design Performance	160 KB	XAPP043	XC4000	
XC4000 Series Technical Information	30 KB	XAPP045	XC4000	
Synchronous and Asynchronous FIFO Designs	120 KB	XAPP051	XC4000	
Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators	70 KB	XAPP052	XC4000	
Implementing FIFOs in XC4000 Series RAM	220 KB	XAPP053	XC4000	VIEW*logic*
Constant Coefficient Multipliers for the XC4000E	110 KB	XAPP054	XC4000	
Block Adaptive Filter	120 KB	XAPP055	XC4000	
System Design with New XC4000X I/O Features	70 KB	XAPP056	XC4000	
Using SelectRAM Memory in XC4000 Series FPGAs	140 KB	XAPP057	XC4000	
XC9500 In-System Programming Using an 8051 Microcontroller	250 KB	XAPP058	XC9500	PC SunOS Solaris HP
Gate Count Capacity Metrics for FPGAs	80 KB	XAPP059	FPGAs	
Design Migration from XC4000 to XC5200	120 KB	XAPP060	XC4000 XC5200	
Design Migration from XC2000/XC3000 to XC5200	70 KB	XAPP061	XC2000 XC3000 XC5200	
Design Migration from XC4000 to XC4000E	60 KB	XAPP062	XC4000	
Interfacing the XC6200 to a uP - Motorola MC68020 Example	70 KB	XAPP063	XC6200	
Interfacing the XC6200 to uP - TMS320C50 Example	80 KB	XAPP064	XC6200	
XC4000 Series Edge-Triggered and Dual-Port RAM Capability	50 KB	XAPP065	XC4000	
Using Serial Vector Format Files to Program XC9500 Devices In-System on Automatic Test Equipment and Third Party Tools	40 KB	XAPP067	XC9500	
In-System Programming Times	10 KB	XAPP068	XC9500	
Using the XC9500 JTAG Boundary Scan Interface	120 KB	XAPP069	XC9500	

Title	Size	Summary	Family	Design
Using In-System Programmability in Boundary Scan Systems	40 KB	XAPP070	XC9500	
Using the XC9500 Timing Model	60 KB	XAPP071	XC9500	
XC9500 Design Optimization	70 KB	XAPP072	XC9500	

Designing with XC9500 CPLDs	100 KB	XAPP073	XC9500	
Pin Preassigning with XC9500 CPLDs	50 KB	XAPP074	XC9500	
Using ABEL with Xilinx CPLDs	120 KB	XAPP075	XC9500	
Embedded Instrumentation Using XC9500 CPLDs	50 KB	XAPP076	XC9500	
Metastability Considerations	30 KB	XAPP077	XC9500	
XC9536 ISP Demo Board	50 KB	XAPP078	XC9500	ABEL VHDL
4Mbit Virtual SPROM	50 KB	XAPP079	XC9500	ABEL
Supply Voltage Migration, 5 V to 3.3 V	30 KB	XAPP080	XC4000	
High-Performance, Low-Area Interpolator Design for the XC6200	120 KB	XAPP081	XC6200	
A Fast Constant Coefficient Multiplier for the XC6200	110 KB	XAPP082	XC6200	
A 32x16 Reconfigurable Correlator for the XC6200	500 KB	XAPP084	XC6200	
A Fax Decoder on the XC6200	160 KB	XAPP085	XC6200	
XC6200 Fax Decoder Co-design	160 KB	XAPP086	XC6200	
Co-Simulation of Hardware and Software	90 KB	XAPP087	XC6200	
I/O Characteristics of the 'XL FPGAs	30 KB	XAPP088	Spartan XC4000	
FPGA Configuration Guidelines	60 KB	XAPP090	FPGAs	
Configuring Mixed FPGA Daisy Chains	20 KB	XAPP091	FPGAs	
Configuration Issues: Power-up, Volatility, Security, Battery Back-up	30 KB	XAPP092	FPGAs	
Dynamic Reconfiguration	20 KB	XAPP093	FPGAs	
Metastable Recovery	20 KB	XAPP094	FPGAs	
Set-up and Hold Times	10 KB	XAPP095	FPGAs	
Overshoot and Undershoot	10 KB	XAPP096	FPGAs	
Xilinx FPGAs: A Technical Overview for the First Time User	20 KB	XAPP097	FPGAs	
The Low-Cost, Efficient Serial Configuration of Spartan FPGAs	100 KB	XAPP098	Spartan	
How to Design Today for the Upcoming SpartanXL FPGA Family	40 KB	XAPP099	Spartan	

Title	Size	Summary	Family	Design
Choosing a Xilinx Product Family	30 KB	XAPP100	all	
XC9500 Remote Field Upgrade	80 KB	XAPP102	XC9500	PC UNIX
The Tagalyzer - A JTAG Boundary Scan Debug Tool	130 KB	XAPP103	XC9500	
A Quick JTAG ISP Checklist	10 KB	XAPP104	XC9500	
A CPLD VHDL Introduction	60 KB	XAPP105	XC9500	
DES Encryption and Decryption on the XC6216	210 KB	XAPP106	XC6200	

Synopsys/Xilinx High Density Design Methodology Using FPGA Compiler	240 KB	XAPP107	XC4000X	
Chip-Level HDL Simulation Using the Xilinx Alliance Series	200 KB	XAPP108	FPGAs	
Hints, Tips and Tricks for using XABEL with Xilinx M1.5 Design and Implementation Tools	80 KB	XAPP109	all	
XC9500 CPLD Power Sequencing	30 KB	XAPP110	XC9500	
Using the XC9500XL Timing Model	80 KB	XAPP111	XC9500XL	
Designing With XC9500XL CPLDs	150 KB	XAPP112	XC9500XL	
Faster Erase Times for XC95216 and XC95108 Devices on HP 3070 Series Testers	30 KB	XAPP113	XC9500	
Understanding XC9500XL CPLD Power	70 KB	XAPP114	XC9500XL	
Planning for High Speed XC9500XL Designs	100 KB	XAPP115	XC9500XL	
Adapting ASIC Designs for Use with Spartan FPGAs	50 KB	XAPP119	Spartan	
How Spartan Series FPGAs Compete for Gate Array Production NEW!	50 KB	XAPP120	Spartan	
The Express Configuration of SpartanXL FPGAs	90 KB	XAPP122	SpartanXL	
Using Three-State Enable Registers in XLA, XV, and SpartanXL FPGAs NEW!	40 KB	XAPP123	XC4000XLA XC4000XV SpartanXL	PC UNIX
Using the Virtex Block SelectRAM+	100 KB	XAPP130	Virtex	
170 MHz FIFOs Using the Virtex Block SelectRAM+ NEW!	60 KB	XAPP131	Virtex	PC UNIX
Using the Virtex Delay-Locked Loop	90 KB	XAPP132	Virtex	
Using the Virtex SelectIO	120 KB	XAPP133	Virtex	

XAPP Note Summaries

XAPP004 Loadable Binary Counters

The design strategies for loadable and non-loadable binary counters are significantly different. This application note discusses the differences, and describes the design of a loadable binary counter. Up, down and up/down counters are described, with lengths of 16 and 32 bits. Design files are available for all six versions.

XAPP005 Register-Based FIFO

While XC3000 series FPGA devices do not provide RAM, it is possible to construct small register-based FIFOs. A basic synchronous FIFO requires one CLB for each two bits of FIFO capacity, plus one CLB for each word in the FIFO. Optional asynchronous input and output circuits are provided. Design files are available for two implementations of this design. The fastest of the two implementations uses a constraints file to achieve better placement.

XAPP007 Boundary Scan Emulator for XC3000

CLBs are used to emulate IEEE 1149.1 Boundary Scan. The FPGA device is configured to test the board interconnect, and then reconfigured for operation.

XAPP008 Complex Digital Waveform Generator

Complex digital waveforms are generated without the need for complex decoding. Instead, fast loadable counters are used to time individual High and Low periods.

XAPP009 Harmonic Frequency Synthesizer and FSK Modulator

Harmonic Frequency Synthesizer:
Uses an accumulator technique to generate frequencies that are evenly spaced harmonics of some minimum frequency. Extensive pipelining is employed to permit high clock rates.

FSK Modulator:
A modification of the Harmonic Frequency Synthesizer that automatically switches between two frequencies in accordance with an NRZ input.

XAPP010 Bus Structured Serial Input/Output Device

Simple shift registers are used to illustrate how 3-state busses may be used within an FPGA device. Dedicated wide decoders are used to decode an I/O address range and enable the internal registers.

XAPP011 LCA Speed Estimation: Asking the Right Question

A simple algorithm is described for determining the depth of logic, in CLBs, that can be supported at a given clock frequency. The algorithm is suitable for XC3000 Series or XC4000 Series FPGA devices.

XAPP012 Quadrature Phase Detector

A simple state machine is used to adapt the output of two photo-cells to control an up/down counter. The state machine provides hysteresis for counting parts correctly, regardless of changes in direction.

XAPP013 Using the Dedicated Carry Logic in XC4000E

This Application Note describes the operation of the XC4000/Spartan dedicated carry logic, the standard configurations provided for its use, and how these are combined into arithmetic functions and counters.

XAPP014 Ultra-Fast Synchronous Counters

This fully synchronous, non-loadable, binary counter uses a traditional prescaler technique to achieve high performance. Typically, the speed of a synchronous prescaler counter is limited by the delay incurred distributing the parallel Count Enable. This design minimizes that delay by replicating the LSB of the counter. In this way even the small longline delay is eliminated, resulting in the fastest possible synchronous counter.

XAPP015 Using the XC4000 Readback Capability

This Application Note describes the XC4000/Spartan Readback capability and its use.

Topics include: initialization of the Readback feature, format of the configuration and Readback bitstreams, timing considerations, software support for reading back FPGA devices, and Cyclic Redundancy Check (CRC).

XAPP017 Boundary Scan in XC4000 and XC5200 Series Devices

XC4000/XC5200/Spartan FPGA devices contain boundary scan facilities that are compatible with IEEE Standard 1149.1. This Application Note describes those facilities in detail, and explains how boundary scan is incorporated into an FPGA design.

XAPP018 Estimating the Performance of XC4000E Adders and Counters

Using the XC4000/Spartan dedicated carry logic, the performance of adders and counters can easily be predicted. This Application Note provides formulae for estimating the performance of such adders and counters.

XAPP022 Adders, Subtracters and Accumulators in XC3000

This Application Note surveys the different adder techniques that are available for XC3000 designs. Examples are shown, and a speed/size comparison is made.

XAPP023 Accelerating Loadable Counters in XC4000

The XC4000/Spartan dedicated carry logic provides for very compact, high-performance counters. This Application Note describes a technique for increasing the performance of these counters using minimum additional logic. Using this technique, the counters remain loadable.

XAPP024 XC3000 Series Technical Information

This Application Note contains additional information that may be of use when designing with the XC3000 series of FPGA devices. This information supplements the data sheets, and is provided for guidance only.

XAPP026 Multiplexers and Barrel Shifters in XC3000 Series

This Application Note provides guidance for implementing high performance multiplexers and barrel shifters in XC3000 Series FPGA devices.

XAPP027 Implementing State Machines in LCA Devices

This Application Note discusses various approaches that are available for implementing state machines in FPGA devices. In particular, the one-hot-encoding scheme for medium-sized state machines is discussed.

XAPP028 Frequency/Phase Comparator for Phase Locked Loops

The phase comparator described in this Application Note permits phase-locked loops to be constructed using FPGA devices that only require an external voltage-controlled oscillator and integrating amplifier.

XAPP029 Serial Code Conversion Between BCD and Binary

Binary-to-BCD and BCD-to-binary conversions are performed between serial binary values and parallel BCD values.

XAPP030 Megabit FIFO in Two Chips: One LCA Device and One DRAM

This Application Note describes the use of an FPGA device as an address controller that permits a standard DRAM to be used as deep FIFO.

XAPP043 Improving XC4000 Design Performance

This Application Note describes XC4000 architectural features that can be exploited in high-performance designs, and software techniques that improve placement, routing and timing. It also contains information necessary for advanced design techniques, such as floor planning, locking down I/Os, and critical path optimization.

XAPP045 XC4000 Series Technical Information

This Application Note contains additional information that may be of use when designing with XC4000 Series devices. This information supplements the product descriptions and specifications, and is provided for guidance only.

XAPP051 Synchronous and Asynchronous FIFO Designs

This application note describes RAM-based FIFO designs using the dual-port RAM in XC4000 Series devices. Synchronous designs with a common read/write clock are described, as well as asynchronous designs with independent read and write clocks. Emphasis is on the fast, efficient and reliable generation of the handshake signals FULL and EMPTY, which determine design performance.

XAPP052 Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators

Shift registers longer than eight bits can be implemented most efficiently in XC4000 or Spartan Series SelectRAM memory. Using Linear Feedback Shift Register (LFSR) counters to address the RAM makes the design even simpler. This application note describes 4- and 5-bit universal LFSR counters, very efficient RAM-based 32-bit and 100-bit shift registers, and pseudo-random sequence generators with repetition rates of thousands and even trillions of years, useful for testing and encryption purposes. The appropriate taps for maximum-length LFSR counters of up to 168 bits are listed.

XAPP053 Implementing FIFOs in XC4000 Series RAM

This Application Note demonstrates how to use the various RAM modes in XC4000 and Spartan Series logic blocks. A simple FIFO is implemented in several different ways, using combinations of level-sensitive (asynchronous) and edge-triggered (synchronous), single-port and dual-port RAM.

XAPP054 Constant Coefficient Multipliers for the XC4000E

This paper identifies two points at which constant coefficient multipliers become the optimum choice in DSP, and implements constant (k) coefficient multipliers (KCMs) in the XC4000E. It also reveals the solution to an interesting design problem which emerges.

XAPP055 Block Adaptive Filter

This application note describes a specific design for implementing a high-speed, full-precision, adaptive filter in the XC4000E/X family of FPGAs. The design may be easily modified, and demonstrates the suitability of using FPGAs in digital signal processing applications. This application note is based on a 12-bit data, 12-bit coefficient, full-precision, block adaptive filter design. This design can be modified to accommodate different data and coefficient sizes, as well as lesser precision. The application note covers how to modify the design including the trade-offs involved. The filter is engineered for use in the XC4000 Series.

XAPP056 System Design with New XC4000X I/O Features

The XC4000X FPGA family (XC4000EX, XC4000XL, XC4000XLA, XC4000XV) provides several new I/O features, including an additional latch on each input and an output multiplexer on each output. The output multiplexer can also be configured as a two-input function generator. Two different types of clock buffers allow system timing flexibility. These features are discussed, and examples show how to use them.

XAPP057 Using SelectRAM Memory in XC4000 Series FPGAs

XC4000 and Spartan Series FPGAs include SelectRAM memory, which can be configured as ROM or as single- or dual-port RAM, with edge-triggered or level-sensitive timing. This application note describes how to implement SelectRAM memory in a design: in schematic entry, using the memory block generator, X-BLOX or LogiBLOX synthesis, and HDL synthesis environments. Specifying timing requirements, evaluating performance, and floorplanning are also described.

XAPP058 XC9500 In-System Programming Using an 8051 Microcontroller

The XC9500 high performance CPLD family provides in-system programmability, reliable pin locking, and JTAG boundary scan test capability. This powerful combination of features allows designers to make significant changes and yet keep the original device pinouts, eliminating the need to re-tool PC boards. By using an embedded controller to program these CPLDs from an on-board RAM or EPROM, designers can easily upgrade, modify, and test designs, even in the field.

XAPP059 Gate Count Capacity Metrics for FPGAs

Three metrics are defined to describe FPGA device capacity: Maximum Logic Gates, Maximum Memory Bits, and Typical Gate Range. The methodology used to determine these values is described.

XAPP060 Design Migration from XC4000 to XC5200

This Application Note reviews the differences between the XC5200 and XC4000 families, recommends approaches for converting XC4000 designs to the XC5200 architecture, and provides a methodology to migrate designs easily in multiple CAE environments.

XAPP061 Design Migration from XC2000/XC3000 to XC5200

This Application Note reviews the differences between the XC5200 and XC2000/XC3000 families, recommends approaches for converting XC2000/XC3000 designs to the XC5200 architecture, and provides a methodology to migrate designs easily in multiple CAE environments.

XAPP062 Design Migration from XC4000 to XC4000E

The XC4000E is an enhanced architecture based on the XC4000 family, but offers many new features, particularly SelectRAM memory. When converting XC4000, XC4000A, XC4000D, and XC4000H designs, the XC4000E is an excellent choice. The conversion process may be as simple as downloading the same bitstream into the

XC4000E device (XC4000 and XC4000D bitstreams only), or it may involve changes to the schematic or HDL code. This Application Note describes techniques that should be employed to convert from any of the XC4000, XC4000A, XC4000D, or XC4000H families to the XC4000E family.

XAPP063 **Interfacing XC6200 To Microprocessors (MC68020 Example)**

The issues involved in interfacing XC6200 family members to microprocessors are discussed. An example using the Motorola 68020 processor is described.

XAPP064 **Interfacing XC6200 To Microprocessors (TMS320C50 Example)**

The issues involved in interfacing XC6200 family members to microprocessors are discussed. An example using the TMS320C50 processor is described.

XAPP065 **XC4000 Series Edge-Triggered and Dual-Port RAM Capability**

The XC4000E/X and Spartan FPGA families provide distributed on-chip RAM. SelectRAM memory can be configured as level-sensitive or edge-triggered, single-port or dual-port RAM. The edge-triggered capability simplifies system timing and provides better performance for RAM-based designs. The dual-port mode offers new capabilities and simplifies FIFO designs.

XAPP067 **Using Automatic Test Equipment to Program XC9500 Devices In-System**

This application note describes how to program XC9500 devices in-system, using standard Serial Vector Format (SVF) stimulus files.

XAPP068 **In-System Programming Times**

This application note discusses the in-system programming speed of the XC9500 devices.

XAPP069 **Using the XC9500 JTAG Boundary Scan Interface**

This application note explains the XC9500 boundary scan interface and demonstrates the software available for programming and testing XC9500 CPLDs. An appendix summarizes the JTAG programmer operations and overviews the additional operations supported by XC9500 CPLDs for in-system programming.

XAPP070 **Using In-System Programmability in Boundary Scan Systems**

This application note discusses basic design considerations for in-system programming of multiple XC9500 devices in a boundary scan chain, and shows how to design systems that contain multiple XC9500 devices as well as other IEEE 1149.1-compatible devices.

XAPP071 **Using the XC9500 Timing Model**

This application note describes how to use the XC9500 timing model. All XC9500 CPLDs have a uniform architecture and an identical timing model, making them very easy to use and understand. To determine specific timing details, users need only compare their paths of interest to the architectural diagrams and, using the timing model presented here, perform a simple addition of incremental time delays.

XAPP072 **XC9500 Design Optimization**

This application note shows the tradeoffs that can be made to gain the greatest possible densities and speeds for schematic, behavioral, and VHDL implementations.

XAPP073 Designing with XC9500 CPLDs

This application note will help designers understand the XC9500 architecture and how to get the best performance from these devices.

XAPP074 Pin Preassigning with XC9500 CPLDs

This application note describes the planning required for successful pin preassigning and gives a detailed example.

XAPP075 Using ABEL with Xilinx CPLDs

This application note provides a basic overview of the ABEL language and gives examples showing how to use ABEL to fully utilize the specific features of Xilinx CPLDs.

XAPP076 Embedded Instrumentation Using XC9500 CPLDs

This application note shows how to build embedded test instruments into XC9500 CPLDs.

XAPP077 Metastability Considerations

Metastability is unavoidable in asynchronous systems. However, using the formulas and test measurements supplied here for the XC9500 CPLDs, designers can calculate the probability of failure. Design techniques for minimizing metastability are also provided.

XAPP078 XC9536 ISP Demo Board

The demo board described in this application note is a tool for demonstrating the In-System Programming (ISP) capabilities of the XC9500 CPLD family.

XAPP079 4Mbit Virtual SPROM

This application note describes the design of a very low cost, CPLD-based virtual SPROM downloader for programming the Xilinx high-density XC4000-Series FPGAs in embedded applications.

XAPP080 Supply Voltage Migration, 5 V to 3.3 V

Mixed voltage environments could create a variety of design challenges. The new 3.3-V XC4000XL, XC4000XLA, and SpartanXL FPGA families are immune to all power sequencing problems and can be interfaced directly with older technology 5-V devices, making them an ideal solution for many mixed voltage systems.

XAPP081 High-Performance, Low-Area Interpolator Design for the XC6200

An interpolator FIR filter design for the XC6200 is discussed. Demonstrates the suitability of the XC6200 for CIC Filters and general DSP. Demonstrates the hardware/software co-design process with the XC6200 demo board.

XAPP082 A Fast Constant Coefficient Multiplier for the XC6200

This application note presents a high performance constant coefficient multiplier for the Xilinx XC6200 FPGA. The design provides performance and density by using dynamic reconfiguration, allowing changes to coefficients without the need for complete reconfiguration.

XAPP084 A 32x16 Reconfigurable Correlator for the XC6200

A correlator design for the XC6200 is discussed. Dynamic reconfiguration is exploited to rapidly reconfigure the hardwired match image template into the design.

XAPP085 A Fax Decoder on the XC6200

Part of a fax decoder circuit is designed in VHDL which, with the aid of some simple software, can decode fax format data. The circuit is mapped onto an XC6216 FPGA within the XC6000DS development system PCI board to accelerate the most cycle intensive parts of the decoding algorithm. This note describes the design of the accelerator circuit for the XC6216 and demonstrates simple and effective codesign.

XAPP086 XC6200 Fax Decoder Co-design

This application note describes the development of co-designs in software and hardware for a code decompression application. The target platform for the application is the XC6200 part within the XC6200DS development system - a PCI-interfaced, reconfigurable processing platform.

XAPP087 Co-Simulation of Hardware and Software

It is possible to implement an entire hardware-software co-design based around the XC6000DS development system. This application note describes a method to allow simulation of the hardware part of the design using the application code as the test bench. This allows the application to be functionally debugged with the minimum of effort and the maximum of confidence, before proceeding with placement and routing of the hardware part on an XC6200 FPGA.

XAPP088 I/O Characteristics of the 'XL FPGAs

Data sheets describe I/O parameters in digital terms, providing tested and guaranteed worst case values. This application note describes XC4000XL/XLA and SpartanXL I/O parameters in analog terms, giving the designer a better understanding of the circuit behavior. Such parameters are, however, not production tested and are, therefore, not guaranteed.

XAPP090 FPGA Configuration Guidelines

These guidelines describe the configuration process for all members of the XC3000, XC4000, XC5200, and Spartan FPGA devices and their derivatives. The average user need not understand or remember all these details, but should refer to the debugging hints when problems occur.

XAPP091 Configuring Mixed FPGA Daisy Chains

Xilinx FPGAs can be configured in a common daisy chain structure, where the lead device generates CCLK pulses and feeds serial configuration information into the next downstream device, which in turn feeds data into the next downstream device, etc. There is no limit to the number of devices in a daisy chain, and XC3000, XC4000, Spartan, and XC5200 series devices can be mixed freely with only one constraint: the lead device must be a member of the highest order family used in the chain.

XAPP092 Configuration Issues: Power-up, Volatility, Security, Battery Back-up

This application note covers several related subjects: How does a Xilinx FPGA power up, and how does it react to power supply glitches? Is there any danger of picking up erroneous data and configuration? What can be done to maintain configuration during loss of primary power? What can be done to secure a design against illegal reverse engineering?

XAPP093 Dynamic Reconfiguration

All Xilinx SRAM-based FPGAs can be in-system configured and re-configured an unlimited number of times. This application note describes the procedures for reconfiguring
the more traditional Xilinx FPGAs.

XAPP094 Metastable Recovery

Whenever a clocked flip-flop synchronizes an asynchronous input, there is a small probability that the flip-flop output will exhibit an unpredictable delay. The flip-flop can enter a symmetrically balanced transitory state, called metastable (meta = between). Xilinx evaluated the XC4000 and XC3000 series flip-flops. The result of this evaluation shows the Xilinx flip-flop to be superior in metastable performance to many popular MSI and PLD devices.

XAPP095 Set-up and Hold Times

Beware of hold time problems, because they can lead to unreliable, temperature-sensitive designs that can fail even at low clock rates.

XAPP096 Overshoot and Undershoot

When users put modern CMOS devices on PC boards, and interconnect them with unterminated lines, there are reflections, commonly called "ringing", that cause overshoots and undershoots of substantial amplitude.

XAPP097 Xilinx FPGAs: A Technical Overview for the First Time User

In the Spartan, XC3000, XC4000, and XC5200 device families, Xilinx offers several evolutionary and compatible generations of Field Programmable Gate Arrays (FPGAs). Here is a short description of their common features. This overview describes two aspects of Xilinx FPGAs:

- What logic resources are available to the user
- How the devices are programmed

XAPP098 The Low-Cost, Efficient Serial Configuration of Spartan FPGAs

This application note shows how to achieve low-cost, efficient serial configuration for Spartan FPGA designs. The approach takes advantage of unused resources in a design, thereby reducing the cost, part count, memory size, and board space associated with the serial configuration circuitry. As a result, neither processor nor PROM needs to be fully dedicated to performing configuration. Information is provided on how the idle processing time of an on-board controller can be used to load configuration data from an off-board source. As a result, it is possible to upgrade a Spartan design in the field by sending the bitstream over a network. A brief summary of Spartan slave serial configuration, its protocol and signals, lays the groundwork for a discussion on ways to reduce bitstream storage and processing requirements. A detailed example illustrates how these techniques can be put into practice. Finally, different formats for configuration data are described along with instructions for their use.

XAPP099 How to Design Today for the SpartanXL FPGA Family

This application note describes how to design a prototype for a SpartanXL FPGA today. By following the design guidelines presented in this note, such a prototype can easily be converted to using a SpartanXL device, once the new family becomes available.

XAPP100 Choosing a Xilinx Product Family

This Application Note describes the various Xilinx product families. Differences between the families are highlighted. The focus of the discussion is how to choose the appropriate family for a particular application. Covers the Spartan, XC3000, XC4000, XC5200, and XC9500 families.

XAPP102 XC9500 Remote Field Upgrade

This application note describes the concept and design of a remote field upgrade subsystem for an in-system programmable XC9500 CPLD. The description of the subsystem is given along with guidelines that should help with variations on it. Additional VHDL files are available for direct use of this design. Specifically, the VHDL files include a complete IRDA receiver design fitting into an XC95108 CPLD.

XAPP103 The Tagalyzer - A JTAG Boundary Scan Debug Tool

The Tagalyzer is a diagnostic tool that helps debug long JTAG boundary scan chains. It can be modified to adapt to a wide variety of different testing situations, and is made from a single XC9536 CPLD. It can be used to debug JTAG chains made up of any manufacturer's parts. The Tagalyzer can be expanded to support arbitrarily long boundary scan chains and adapted to change its functionality, as needed.

XAPP104 A Quick JTAG ISP Checklist

ISP circuitry is beneficial for fast prototype development. However, even the most robust circuitry needs minimal consideration to deliver the best in system programming results. This application brief describes a short list of considerations needed to get the best performance from your ISP designs.

XAPP105 A CPLD VHDL Introduction

This introduction covers the basics of VHDL as applied to CPLDs. Specifically included are those design practices that translate well to CPLDs, permitting designers to use the best features of this powerful language to extract the best performance from CPLD designs.

XAPP106 DES Encryption and Decryption on the XC6216

This Application Note describes the design and implementation of DES (Data Encryption Standard) encryption/decryption using the XC6216.

XAPP107 Synopsys/Xilinx High Density Design Methodology Using FPGA

Compiler

This paper describes design practices to synthesize high density designs (i.e. over 100,000 gates), composed of large functional blocks, for today's larger Xilinx FPGA devices using the Synopsys FPGA Compiler. The Synopsys FPGA Compiler version 1998.02, Alliance Series 1.5, and the XC4000X family were used in preparing the material for this
application note.

XAPP108 Chip-Level HDL Simulation Using the Xilinx Alliance Series

This application note describes the basic flow and some of the issues to be aware of for HDL simulation with Alliance Series software. The goal of this document is to familiarize the user with some of the concepts but should not be considered a replacement for the Xilinx or HDL simulator's documentation.

XAPP109 Hints, Tips and Tricks for using XABEL with Xilinx M1.5 Design and Implementation Tools

This application note summarizes the issues and design techniques specific to the Xilinx ABEL Interface, version M1.5.

XAPP110 XC9500 CPLD Power Sequencing

Mixed signal systems require logic parts that can operate with two power supplies. XC9500 CPLDs are designed to operate in either mixed 5V/3.3V systems or 5V only systems. To handle both conditions, care has been taken to ensure that designers need not introduce elaborate circuitry to guarantee that 5V and 3.3V power supplies rise or fall in any particular sequence. This application note describes the underlying XC9500 circuitry to give designers the understanding they need to best use these powerful CPLDs.

XAPP111 Using the XC9500XL Timing Model

This application note describes how to use the XC9500XL timing model.

XAPP112 Designing With XC9500XL CPLDs

This application note will help designers get the best results from XC9500XL CPLDs. Included are practical details on such topics as pin migration, timing, mixed voltage interfacing, power management, PCB layout, high speed considerations and JTAG best practices.

XAPP113 Faster Erase Times for XC95216 and XC95108 Devices on HP 3070 Series Testers

This application note describes an enhanced procedure for utilizing the new faster bulk erase capability of the XC95216 and XC95108 devices on the HP 3070 tester.

XAPP114 Understanding XC9500XL CPLD Power

The goal of this application note is to discuss XC9500XL CPLD power estimation and optimization and provide the reader with an understanding of sense-amplifier based CPLD power dissipation. A brief discussion of the process for estimation is given. With this information, you can accurately assess the power dissipation for a design. You will also be given guidelines permitting you to make key choices to manage the power dissipation of your design and understand the package thermal limits.

XAPP115 Planning for High Speed XC9500XL Designs

Discovering electrical problems at debug is too late. The printed circuit board has been built and may have to be significantly changed to debug. The best approach is to avoid the problem. By anticipating common problems, designs can be substantially “bullet-proofed” before debug. This means planning for options at the outset is the best solution. A thorough but practical checklist is one aspect of planning for success. This application note provides a framework for checklisting a design early to eliminate problems.

XAPP119 Adapting ASIC Designs for Use with Spartan FPGAs

Spartan FPGAs are an exciting, new alternative for implementing digital designs that, previously, would have employed ASIC technology. Pre-existing ASIC intellectual property can be adapted for use with Spartan devices by following a straightforward procedure. Each step of the procedure is explained in detail. Guidelines show how an ASIC design, in the form of an RTL-level HDL file, can be revised to take full advantage of the Spartan series’ capabilities, thereby achieving efficient, high-performance implementations.

XAPP120 How Spartan Series FPGAs Compete for Gate Array Production NEW!

This application note discusses the enormous progress made by FPGAs in the areas of technology, low-price and performance. It discusses the major advantages of using FPGAs over traditional gate arrays, which makes FPGAs the best high-volume production solution available today.

XAPP122 The Express Configuration of SpartanXL FPGAs

Express Mode uses an eight-bit-wide bus path for fast configuration of Xilinx FPGAs. This application note provides information on how to perform Express configuration specifically for the SpartanXL family. The Express mode signals and their associated timing are defined. The steps of Express configuration are described in detail, followed by detailed instructions that show how to implement the configuration circuit.

XAPP123 Using Three-State Enable Registers in XLA, XV, and SpartanXL FPGAs NEW!

The use of the internal IOB three-state control register can significantly improve output enable and disable time. This application note shows you how to use hard macros to implement this register in both HDL and schematic based designs.

XAPP130 Using the Virtex Block SelectRAM+

The Virtex FPGA Series provides dedicated blocks of on-chip 4096 bit dual-port synchronous RAM. You can use each port of the block SelectRAM+ memory independently as a read/write, read or write port, and configure each port to a specific data width. The Block SelectRAM+ offers new capabilities for the FPGA designer, allowing you to simplify designs.

XAPP131 170 MHz FIFOs Using the Virtex Block SelectRAM+ NEW!

The Virtex FPGA Series provides dedicated on-chip blocks of 4096 bit dual-port synchronous RAM, which are ideal for use in FIFO applications. This application note describes a way to create a common clock (synchronous) version and an independent clock (asynchronous) version of a 512 x 8 FIFO, with the depth and width being adjustable within the Verilog code. A hand-placed version of the design runs at 170 MHz in the -6 speed grade.

XAPP132 Using the Virtex Delay-Locked Loop

The Virtex FPGA series provides four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, zero clock skew between output clock signals distributed throughout the device, and advanced clock domain control. You can use these dedicated DLLs to implement several circuits which improve and simplify system level design.

XAPP133 Using the Virtex SelectIO

The Virtex FPGA series provides highly configurable, high-performance I/O resources called SelectIO which provide support for a wide variety of I/O standards. SelectIO includes a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and features of SelectIO and the design considerations described in this document can improve and simplify system level design.

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