16 Bit Constant Current LED Driver

Product Description

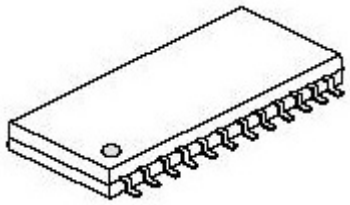
FD9802 is a 16-bit constant current driver for LED displays. This product is designed by Shanghai Fengxin Microelectronics Co., Ltd. The constant current can be set between 5mA to 90mA by an external resistor.

FD9802C has the same function with MBI5026GF and FD9802D has the same function with MBI5026GP. FD9802 can be directly used on the existing PCB, no need to design new PCB. FD9802's performance price ratio is higher; the manufacturers of LED display can save cost by using FD9802.

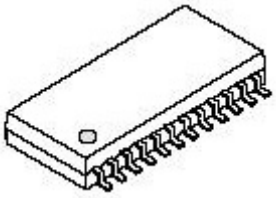
Model

FD9802C (Package SSOP24-1.0)

FD9802D (Package SSOP24-0.635)



FD9802C:SSOP24-300-1.0



FD9802D:SSOP24-150-0.635

Features

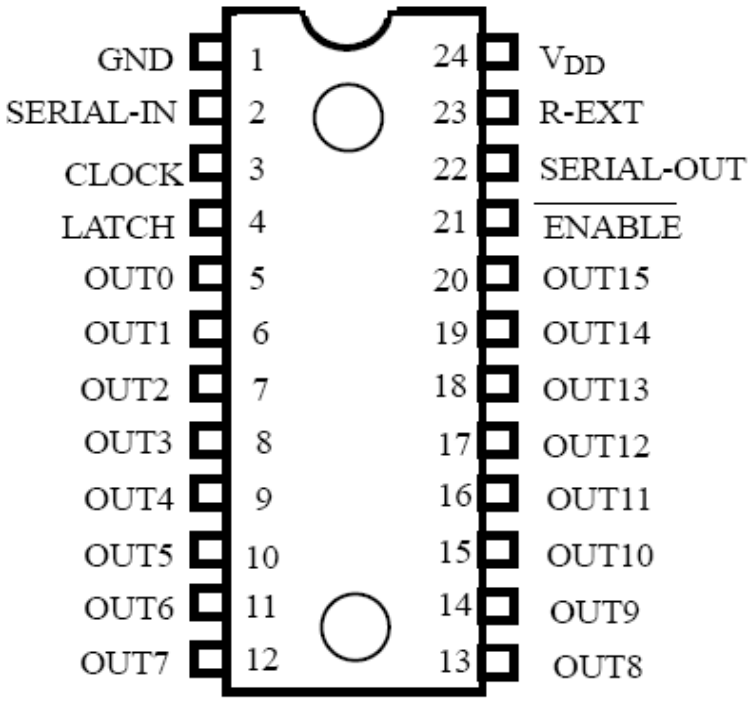
16 constant-current output channels
Constant output current invariant to load voltage change
Output current adjusted through an external resistor
Constant output current range: 5-90mA
Excellent output current accuracy:
- Between channels：<±3%
- Between ICs：<±4%

25MHZ clock frequency
Input compatible 5V CMOS
5V supply voltage

"Bb-free & Green" Package

Compatible with TI's TLC5926/7, TOSHIBA's TB62726 and Macroblock's MBI5026/4/0.

Pin Assignment

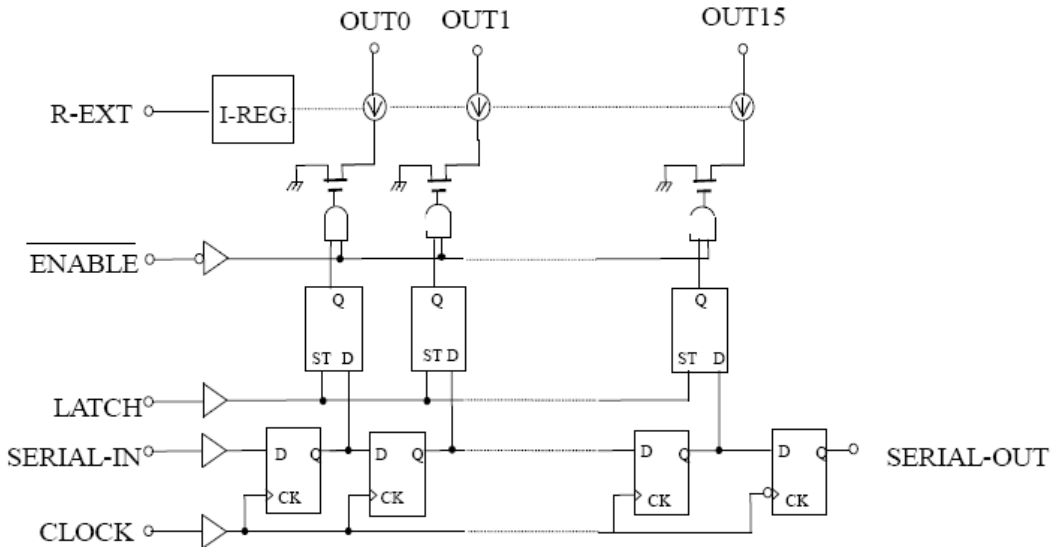


Pin Description

Pin Number	Pin Name	Function
1	GND	Ground terminal.
2	SERIAL-IN	Terminal of serial-data input to the shift register.
3	CLOCK	Clock input terminal for data shift on rising edge.
4	LATCH	Data strobe input terminal. Serial data is transferred to the output latch when LATCH is high. The data is latched when LATCH goes low.
5~20	OUT 0~15	Constant current output terminals.
21	ENABLE	Output enable terminal. All the output terminals are turned off when ENABLE is high; all the output terminals are turned on when ENABLE is low.

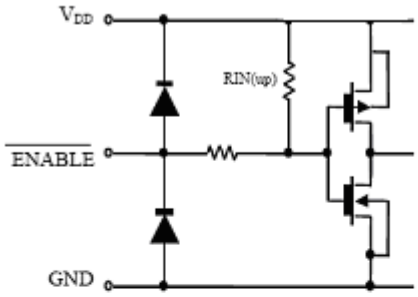
22	SERIAL-OUT	Serial-data output terminal, to the next SERIAL-IN.
23	R-EXT	Current setting terminal. Connected with an external resistor to adjust output current.
24	V_{DD}	Supply voltage terminal.

Block Diagram

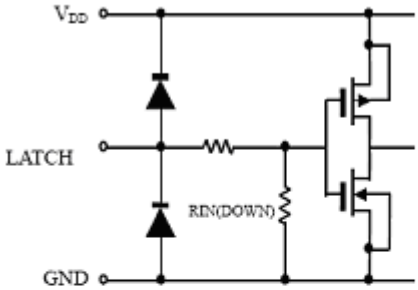


Equivalent Circuit of Inputs and Outputs

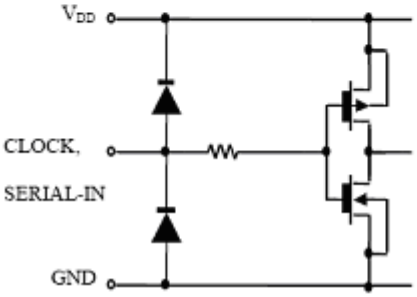
1. $\overline{\text{ENABLE}}$



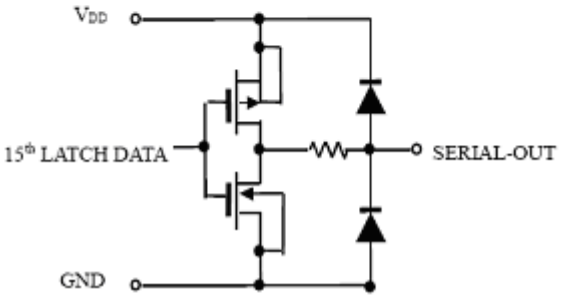
2. LATCH



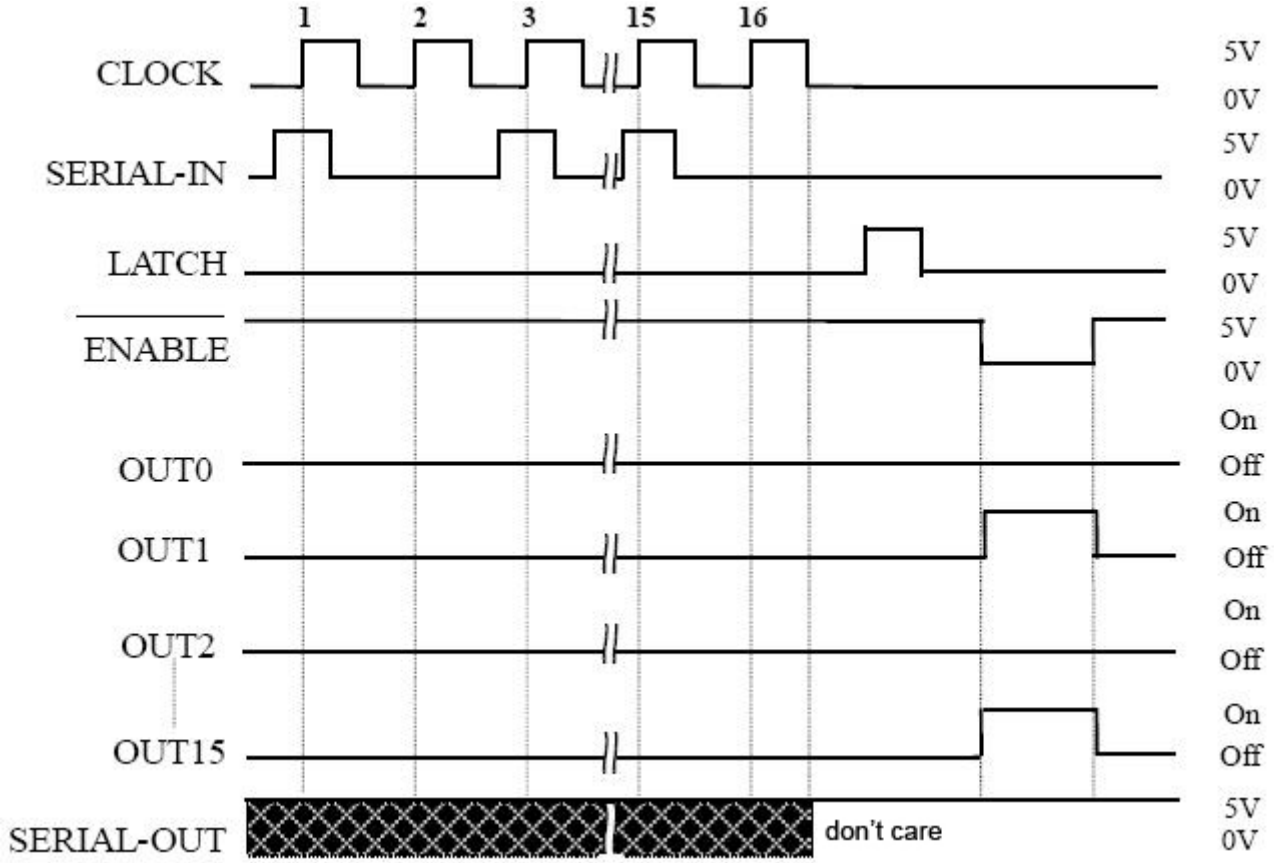
3. CLOCK, SERIAL-IN



4. SERIAL-OUT



Timing Diagram



Note: The latches circuit holds data when the LATCH terminal is Low. When the LATCH terminal is at High level, latch circuit doesn't hold the data, it passes from the input to the output. When the ENABLE terminal is at Low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF. When the ENABLE terminal is at High level, it switches off all the data on the output terminal.

Truth Table

CLOCK	LATCH	$\overline{\text{ENABLE}}$	SERIAL-IN	$\overline{\text{OUT0}}$ ... $\overline{\text{OUT7}}$ ... $\overline{\text{OUT15}}$	SERIAL-OUT
↑	H	L	D_n	$\overline{D_n}$ ..... $\overline{D_{n-7}}$ ..... $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ ..... $\overline{D_{n-5}}$ .... $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ .... $\overline{D_{n-5}}$ .... $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

Note: OUT0 to OUT15 = ON when Dn = H; OUT0 to OUT15 = OFF when Dn = L.

Maximum Rating

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD}	0~7.0	V
Input voltage	V_{IN}	-0.4~VDD+0.4	V
Output voltage on OUTn	V_{OUT}	-0.5~+17.0	V
Output current on OUTn	I_{OUT}	+90	mA
Clock frequency	f_{CLK}	25	MHz
GND terminal current	I_{GND}	1440	mA
Power Dissipation	P_D	1.00(ON PCB, Ta=25℃)	W
Thermal Resistance	$R_{th(j-a)}$	120(ON PCB)	℃/W
Storage temperature range	T_{stg}	-55~+150	℃
Operating temperature range	Topr	-40~+85	℃

Recommended Operating Conditions

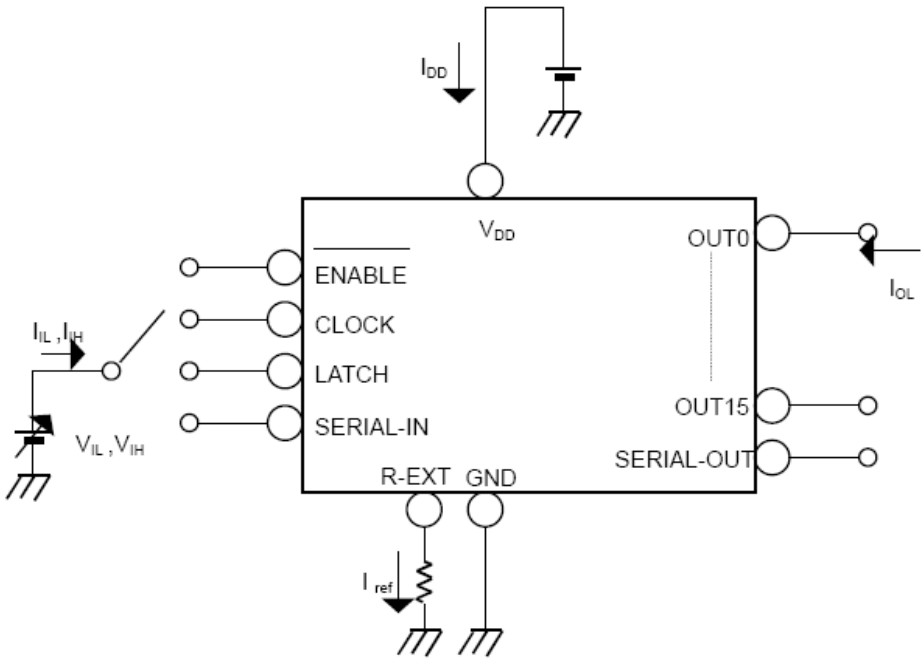
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	4.5	5.0	5.5	V
Input voltage	V_{IH}	-	0.7VDD	-	VDD+0.3	V
	V_{IL}	-	-0.3	-	0.3VDD	
Output voltage on OUTn	V_{OUT}	-	-	-	15.0	V
Output current	I_{OUT}	OUTn	5	-	45	mA
	I_{OH}	SERLAL-OUT	-	-3.7	-	
	I_{OL}	SERLAL-OUT	-	-4.0	-	
LATCH pulse width	$T_{w\,LAT}$	VDD=4.5~5V	100	-	-	ns
CLOCK pulse width	$T_{w\,CLK}$		50	-	-	ns
Setup time for DATA	$T_{setup(D)}$		60	-	-	ns
Holdtime for DATA	$T_{hold(D)}$		20	-	-	ns
Hold time for LATCH	$T_{setup(L)}$		100	-	-	ns
Clock frequency	f_{CLK}	Cascade Operation	-	15	20	MHz
Power Dissipation	P_D	Ta=85 ^{o}C	-	-	0.5	W

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	-	0.7VDD	-	VDD	V
Low level input voltage	V_{IL}	-	GND	-	0.3VDD	
Output leakage current	I_{OH}	V_{OH}=9.5V	-	-	1.0	uA
Output Voltage (S-OUT)	V_{OL}	I_{OL}=1.0mA	-	-	0.4	V
	V_{OH}	I_{OH}= -1.0mA	4.6	-	-	
Output Current (Between channels)	I_{OL1}	V_{OUT}=0.7±0.25V REXT=910Ω	-	-	±3	%
	I_{OL2}	V_{OUT}=0.7±0.25V REXT=360Ω	-	-	±3	
Output Current (Between Ics)	I_{OL3}	V_{OUT}=0.7V REXT=910Ω	-	-	±4	
	I_{OL4}	V_{OUT}=0.7V REXT=360Ω	-	-	±4	
Output Current vs. Output Voltage Regulation	%/VDD	REXT=360Ω, Ta=-40~85 ^{o}C	-	1.5	5.0	%/V
Pull-up Resistor	$R_{IN(pull\ up)}$	-	150	300	600	kΩ
Pull-down Resistor	$R_{IN(pull\ down)}$	-	100	200	400	kΩ
Supply Current (OFF)	$I_{DD(off)1}$	REXT=OPEN,OUT0~7=off	-	0.3	0.6	mA
	$I_{DD(off)2}$	REXT=470Ω,OUT0~7=off	3.9	5.5	7.7	
	$I_{DD(off)3}$	REXT=250Ω,OUT0~7=off	7.2	10.1	14.1	
	$I_{DD(on)1}$	REXT=470Ω,OUT0~7=on	3.9	5.5	7.7	

Supply Current (ON)	$I_{DD(on)2}$	REXT=250Ω,OUT0~7=on	7.2	10.1	14.1	

Test Circuit for Electrical Characteristics

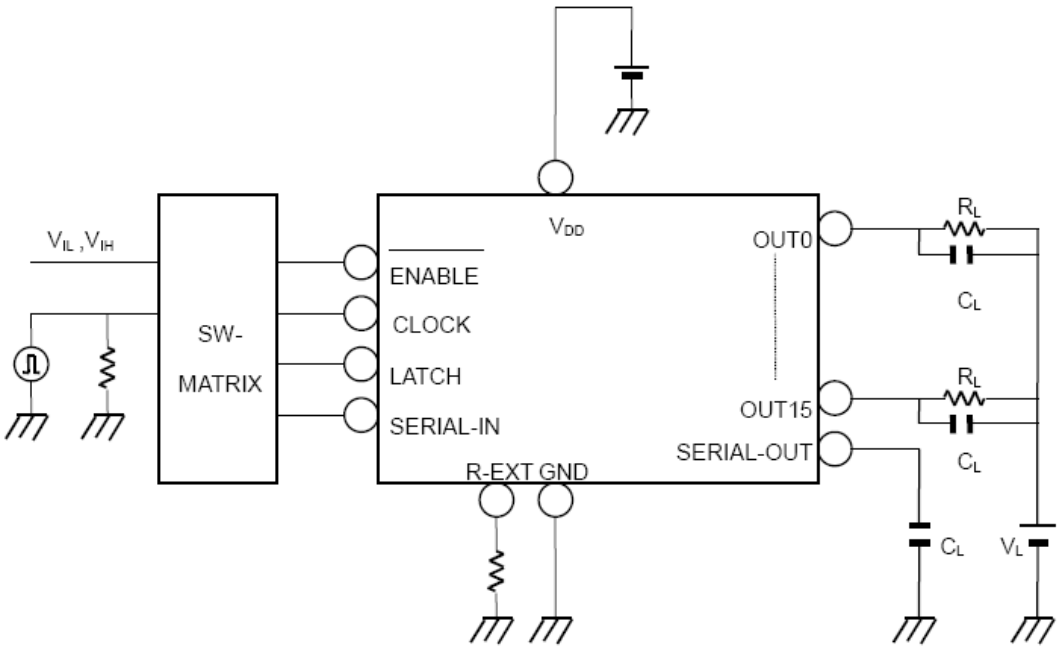


Switching Characteristics

Parameter		Symbol	Test Condition	Min.	Typ.	Max.	Unit
propagation delay time （“L” to “H”）	CLK-$\overline{OUTn}$	tpLH	VDD=5.0V VCE=0.4V VIH= VDD VIL=GND REXT=470Ω VL=3.0V RL=1.0K CL=10.5pF	-	120	150	ns
	$\overline{LATCH}$ - $\overline{OUTn}$			-	120	150	
	$\overline{ENABLE}$ - $\overline{OUTn}$			-	120	150	
	CLK-S-OUT			-	30	70	
propagation delay time （“H” to “L”）	CLK-$\overline{OUTn}$	tpHL		-	70	100	ns
	$\overline{LATCH}$ - $\overline{OUTn}$			-	70	100	
	$\overline{ENABLE}$ - $\overline{OUTn}$			-	70	100	
	CLK-S-OUT			-	30	70	

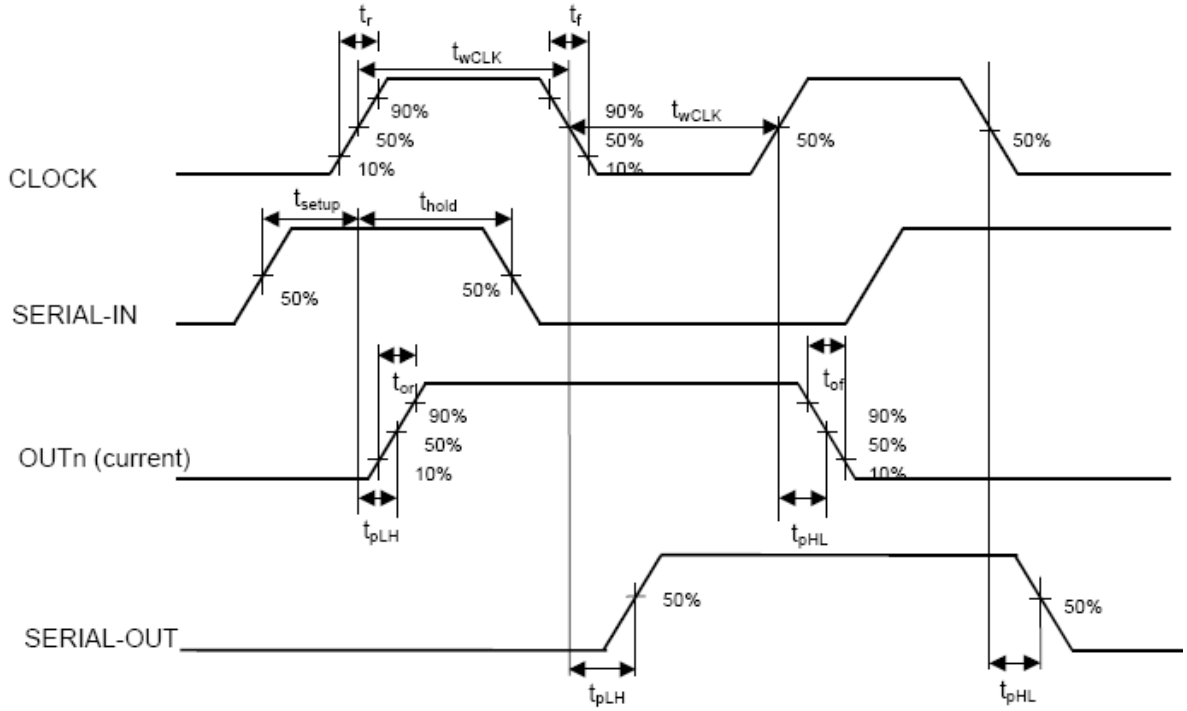
Output current rise time	tor		-	100	200	ns
Output current fall time	tof		-	60	120	ns

Test Circuit for Switching Characteristics

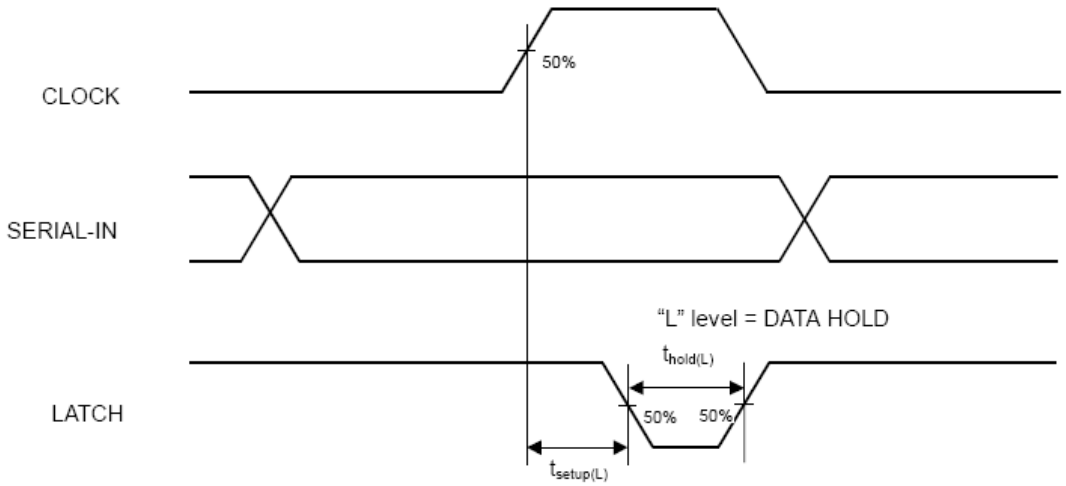


Timing Waveform

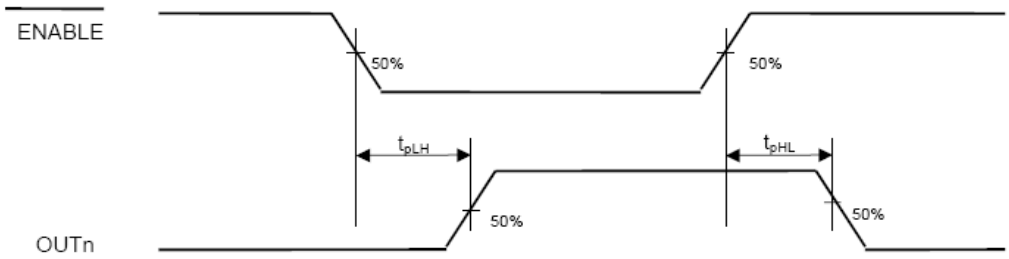
1. CLOCK; OUTn ; SERIAL-IN; SERIAL-OUT



2. CLOCK; SERIAL-IN; LATCH



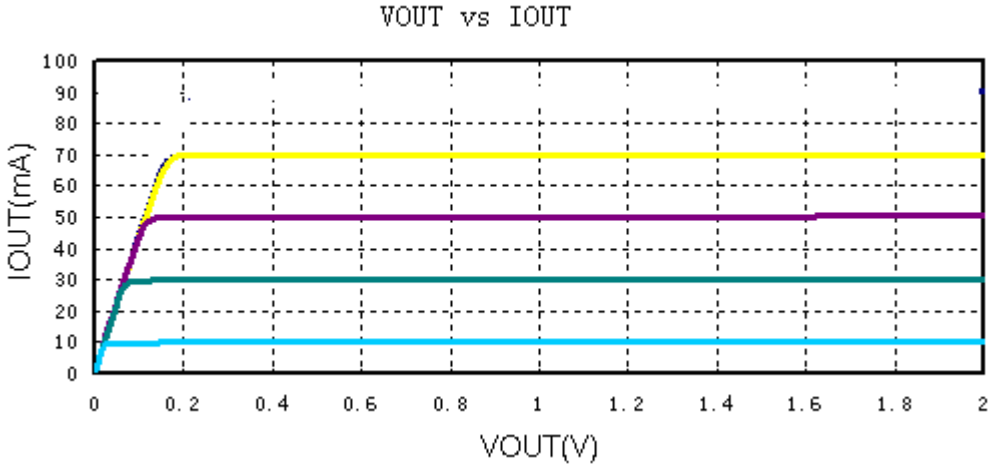
3. ENABLE;OUTn



Constant Current

In LED display application, FD9802 Provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

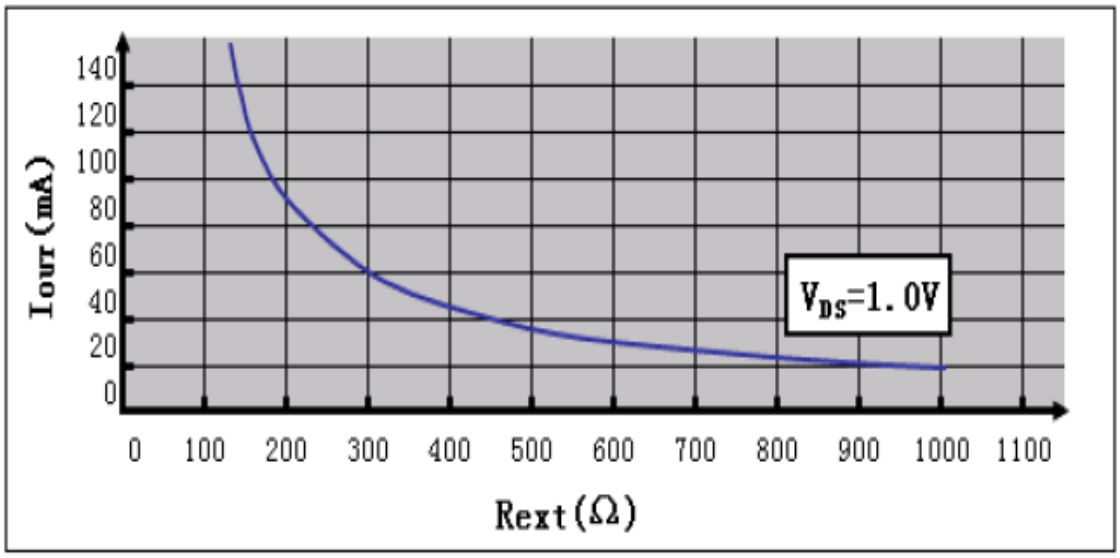
1) The maximum current variation between channels is less than ±3%,and that between Ics is less than ±4%.
2) The output current can be kept constant regardless of the variations of LED forward voltages(Vf). This performs as a perfection of load regulation.



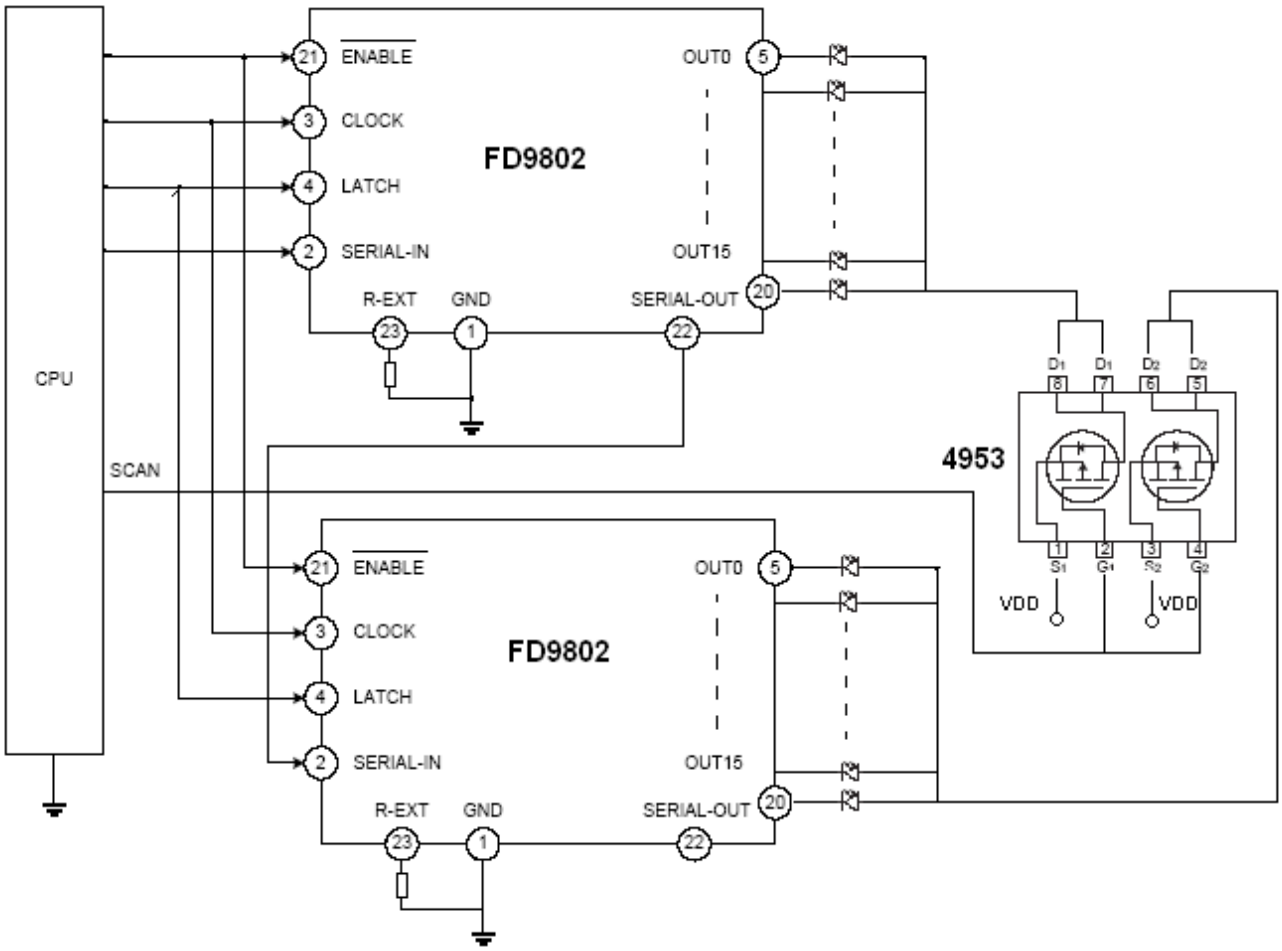
Output Current Setting（IOUT-R-EXT ）

The output current is set by the external resistor RSET. The output current is:

Iout = (1.23/Rext)×15.3



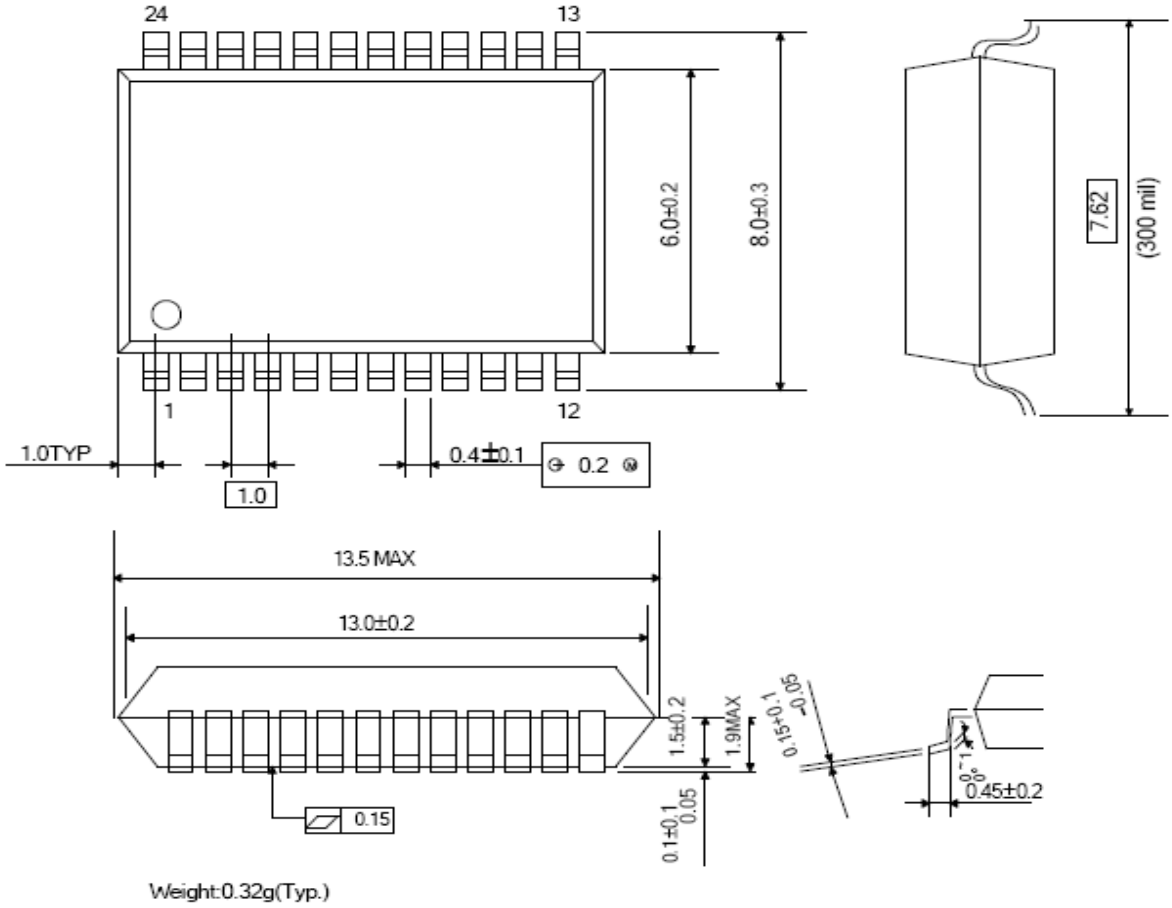
Application circuitry



Package Information

Part Number	Package Type
FD9802C	SSOP24-300-1.00
FD9802D	SSOP24-150-0.635

FD9802C （SSOP24-300-1.00） Unit: mm



Weight:0.32g(Typ.)

FD9802D （SSOP24-150-0.635） Unit: mm