

FPGA XLink Application Note

(VERSION 1.0)



2009-01-06

Authors:

Ali Dixon

Copyright © XMOS Ltd.
All Rights Reserved

Document History

Date	Author	Details
2009.01.06	Ali Dixon	First release – Version 1.0

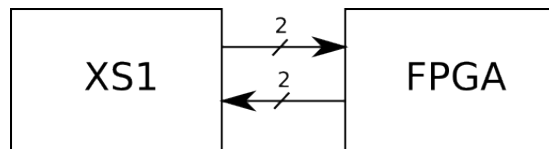
Introduction

Implementing an XLink on an FPGA is extremely useful, as it allows direct connectivity into the XS1 architecture. Channels can be established between software executing on the XC1 and hardware on the FPGA, allowing high level software to communicate directly with external devices.

The full specification of XLink is available at:

<https://www.xmos.com/system/files/xsystem.pdf>

In this simple example, the FPGA receives packets over a 2-bit XLink from a thread executing on the XS1 device, performs some simple processing and sends back response packets. The thread inputs the response messages and validates the data.



Assembly functions are used to enable the XLink and provide a channel end to the XC test program.

The example has been built and tested on an XDK, using an expansion port to connect the XLink to the FPGA board.

Performance and Logic Utilisation

Synthesis for a Xilinx Spartan 3 (xc3s1000-4ft256) device gives the following results:

Max Frequency	110 MHz
4 input LUTs	608
Flops	300

Note the flop count includes the 8 token buffers for both transmit and receive.

Testing

To build the XDK application, in the `test` directory build the test program using the Makefile.

Use `xrun` to execute the program on the `xdk`. The `-io` flag is needed to output the test results over `jtag`.

```
xrun -io test.xe
```

The program outputs the values successfully transmitted and received.

Verilog Source Listing

Fifo.v	Fifo used for buffering incoming/outgoing tokens
SwitchCommonDef.v	Switch definitions
SwitchTokenDef.v	Token definitions
XLinkController.v	Controls sending and receiving of credit and reset tokens
XLinkDataProc.v	User code – data processor. This receives messages and sends replies back.
XLinkTb.v	Testbench – performs reset and sends packets.
XLinkTxCtrl	Manages the tx fifo, giving data to TxPhy when it requests it.
XLinkTop.v	Top level module. Instantiates the fifos, tx and rx phys, xlink_controller and data processor.
XLinkDefines.v	Link layer definitions
XLinkRxPhy2B.v	2-bit Xlink receive state machine
XLinkRxPhy.v	Wrapper for 2-bit Xlink receive
XLinkTxPhy2B.v	2-bit Xlink transmit state machine
XLinkTxPhy.x	Wrapper for 2-bit Xlink transmit

XS1 Source Listing

test/main.xc	Test program which enables the XLink and sends and receives messages.
test/data.S	Assembly functions for creating the connection and sending messages
common/xlinks.xc	Functions for controlling Xlinks
Common/ssctrl.S	Assembly functions for reading and writing SSCTL control registers.

XMOS Ltd is the owner or licensee of this design, code, or Information (collectively, the “Information”) and is providing it to you “AS IS” with no warranty of any kind, express or implied and shall have no liability in relation to its use. XMOS Ltd makes no representation that the Information, or any particular implementation thereof, is or will be free from any claims of infringement and again, shall have no liability in relation to any such claims.

(c) 2008 XMOS Limited - All Rights Reserved