Three-channel constant current LED driver TM1829

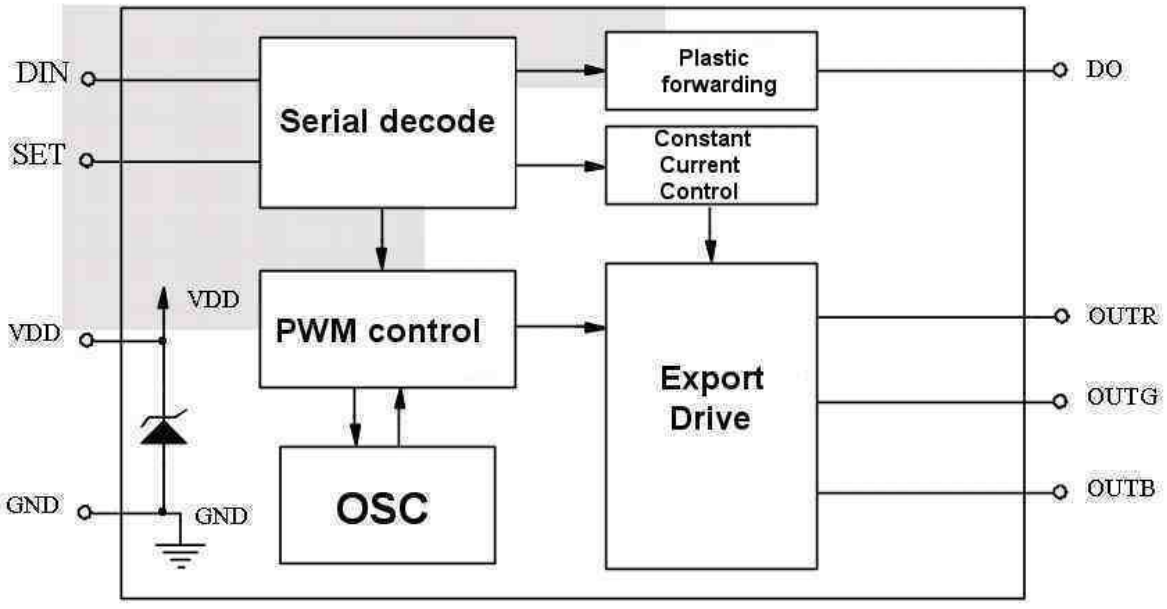
Characterization

TM1829 is a three-channel LED (light emitting diode) constant current drive control of a dedicated circuit, the internal MCU integrated single-wire digital interface, data latches Devices, LED constant current driver circuit, PWM brightness control circuit. Through the single-wire digital interface chip (DI, DO) cascade, the external controller only Single line can control the chip and its subsequent cascade chips. Constant luminance value and the PWM output port can be individually TM1829 by peripheral controller Setting. VDD pin internal 5V regulator integrated, less peripheral devices. This product is excellent performance, reliable quality.

Features

Using power CMOS process
OUT 24V output port pressure
Built-in 5V VDD regulator, the series resistor voltage support 6 ~ 24V
Brightness adjustment circuit 256 adjustable brightness
Wire serial cascade interface
Oscillation mode: Built-in RC oscillator and clock synchronization based on the data line signal, after completion of this unit can receive data automatically after
After regeneration to continue sending data through the data output lower, the signal does not change with the cascade far and distortion or attenuation
Built-in power-on reset circuit
PWM control side can achieve 256 adjustable scan frequency 7kHz
Constant current regulator can achieve 32 (10mA-41mA)
By receiving and decoding a data signal line is completed
When the refresh rate of 30 frames / s, the number of low-speed mode cascade of not less than 1024 points, the high-speed mode is not less than 2048 points
Data transfer rate up to 800Kbps and 1.6Mbps modes
Transmission distance between any two points less than 30 m
Package: SOP8, DIP8

Internal structure diagram



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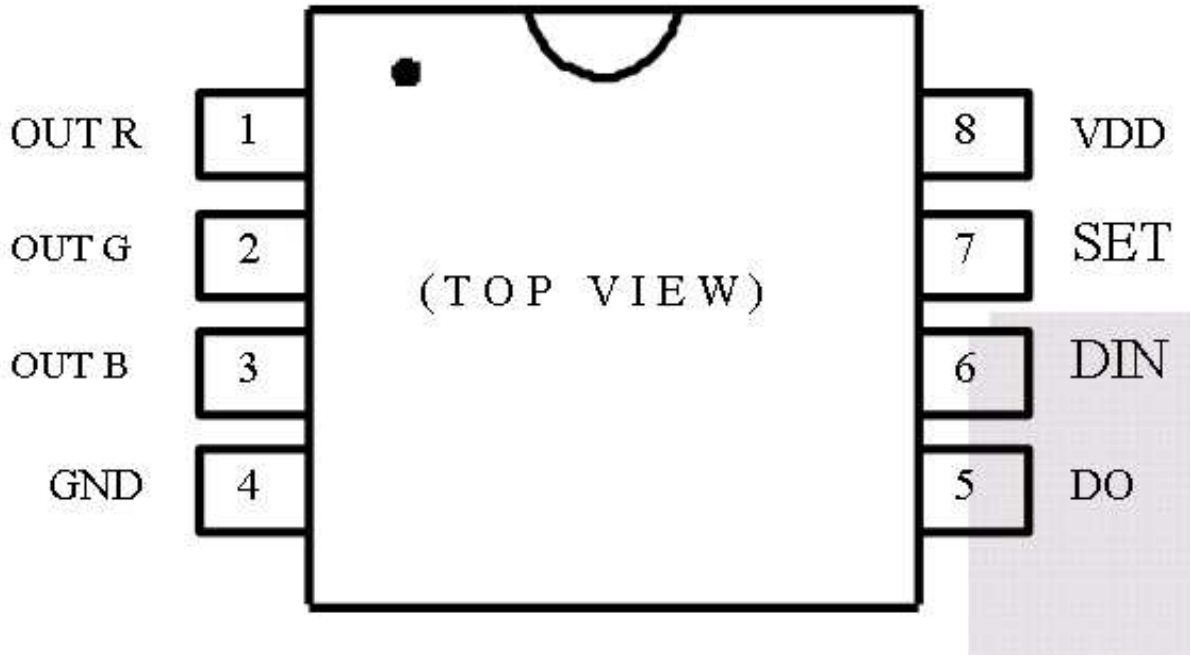
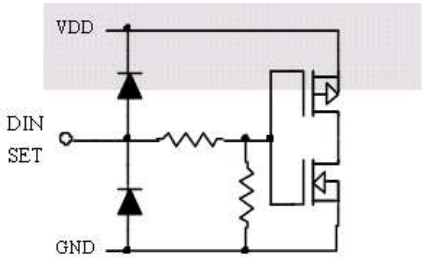
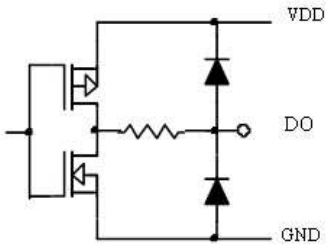
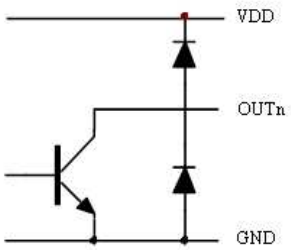


Pin Name	Pin Number	I / O	Description
DIN	6	In	Data input
DO	5	Out	Data Output
SET	7	In	to VDD -> high-speed mode, to GND or floating -> low-speed mode
OutR	1	Out	Red PWM constant current output
OutG	2	Out	Green PWM constant current output
OutB	3	Out	Blue PWM constant current output
VDD	8	-	Logic Supply
GND	4	-	Ground

Input and output equivalent circuit:







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IC system electrostatic sensitive devices, in the dry season or a dry environment prone to a lot of static electricity, electrostatic discharge may damage
Bad integrated circuits, microelectronic day is recommended to take all appropriate measures to integrated preventive treatment, improper handling and welding, may
ESD can cause damage or performance degradation, the chip does not work.

Limiting values:

Parameter name		Parameter Symbol	Limits	Unit
Logic Supply Voltage		VDD	-0,5 - +7,0	V
Input voltage range	DIN, SET	Vin	-0,5 - VDD +0.7	V
Output Current (DC)	OutR, OutG, OutB	Iout	41	mA
output terminal voltage range	OutR, OutG, OutB	Vout	-0,5 - 30,0	V
Clock frequency	DIN	Felk	2.0	MHz
Operating Temperature Range		Topr	-40° - +85	°C
Storage temperature range		Tstg	-55 - +150	°C
Human Body Model (HBM) Machine Model (MM)		ESD	4000 400	V V

(1) chip to work long hours under the above conditions limit parameters may cause permanent damage to the device or reduced reliability, the day is not built Microelectronics
Any of the parameters to meet or exceed these limits when meeting the actual use;
(2) All voltage values are with respect to the system test.

Recommended Operating Conditions:

At -45° - +85° under test, unless otherwise noted			TM1829			
Parameter name	Parameter Symbol	Test Conditions	Min	Typical values	Max	Unit
Supply Voltage	VDD		4.5	5.0	5.5	V
DIN input Voltage range	VDIN	DIN 1k resistor in series	-0,5	--	VDD-07	V
SET input Voltage range	Vset	DIN 1k resistor in series	-0.5	--	VDD+0.7	V
DO output Voltage range	Vdo	DO 1k resistor in series	-0.5	--	VDD-0.7	V
OUT output Voltage range	Vout	OUT = OFF	-0.5	--	24.0	V
Operating Temperature Range	Ta		-40	--	+85	°
Operating junction temperature range	Tj		-40	--	+125	°

Three-channel constant current LED driver TM1829

Electrical Characteristics

(VDD = 5.0V and under -40° - +85° in, and VDD = 5.0V typ. TA = +25°), unless otherwise noted			TM1829			Unit
Parameter name	Parameter Symbol	Test Conditions	Min	Typical values	Max	
High-level output voltage	Voh	Ioh =-6mA: DO	VDD-0.5	VDD	VDD +0.5	V
Low level output voltage	Vol	Iol = 10mA: DO			0.4	V
High input voltage	Vih	VDD = 5.0V	3.5		VDD	V
Low-level input voltage	Vil	VDD = 5.0V	0		1.35	V
High output current	Ioh	VDD = 5.0V, SDO = 5.0V		1		mA
Low-level output current	Iol	VDD = 5.0V, SDO = 1.0V		10		mA
Input Current	Iin	DIN tied to VDD or GND	-1		1	μA
Logic Supply Current (VDD)	Icco	OUTR, OUTG, OUTB, DIN, SET, DO = open	1.2	3.0	4.2	mA
Constant output current range	Iolc	OUTR, OUTG, OUTB = 3.0V	10		41	mA
Output leakage current	Iolck	OUTR, OUTG, OUTB = OFF	0		0.3	μA
OUT port duty cycle	Tpwm	OUT pull-up resistor	135	140	145	μs
Constant error (Channel-to-channel)	ΔIolco	OUTR, OUTG, OUTB = ON , VOUTn = 1V			± 3	%
Constant error (Chip-to-chip)	ΔIolc1	OUTR, OUTG, OUTB = ON , VOUTn = 1V			± 6	%
Linear adjustment	ΔIolc2	OUTR, OUTG, OUTB = ON , VOUTn = 1V		± 0.5	± 1	% / V
Load Regulation	ΔIolc3	OUTR, OUTG, OUTB = ON , VOUTn = 1V3V				
Dynamic current consumption	Idddyn	OUTR, OUTG, OUTB = OFF DO = open			3	mA
Thermal resistance	Rth (ja)		79.2		190	° /W
Power Consumption	PD	(Ta = 25 ° C)			250	mW

Switching Characteristics

(VDD = 5.0V and under -40° to +85°, VDD = 5.0V typ. TA = +25°), unless otherwise noted			TM1829			
Max	Typical values	Min	Test Conditions	Parameter Symbol	Parameter name	Unit
Low-speed mode	fosc1	DIN floating or connected to GND		800		KHz
High-speed mode	fosc2	DIN tied to VDD		1.6		MHz
OUT PWM output frequency	fout	OutR, OutG, OutB	6.5	7	7.5	KHz
Propagation delay time	Tplz	DIN → DOUT			200	ns
	Tplz	CL = 15pF RL = 10K Ω			100	ns
Fall Time	Tthz	CL = 300pF OutR / OutG / OutB			80	μs
Input capacitance	Ci				15	pF

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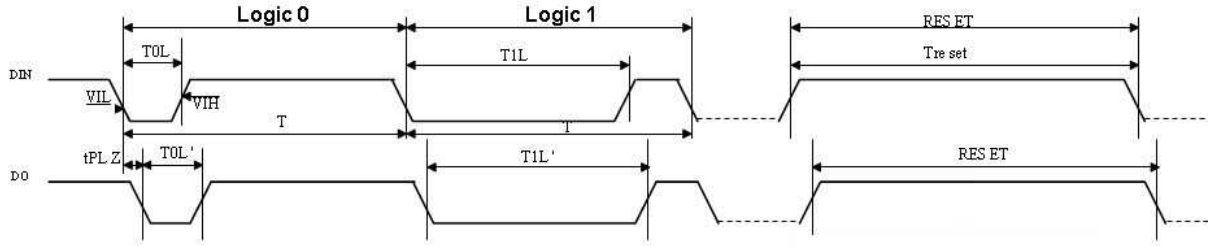
Timing Characteristics



Description

The chip uses single-wire communication, using methods NRZ transmission signal. Chip power-on reset after accepting DIN

End of the data sent, after receiving complete 24bit, DO DIN port starts forwarding client continues to send data to the next chip to mention cascade

For the input data. Before forwarding the data, DO port has been high. If the DIN input RESET Reset signal, the chip will reset after a successful root

According to the received data output corresponding 24bit PWM duty cycle waveform, and the chip re waiting to receive new data, beginning at the receiving end 24bit

After the data, DO port forwarding data through the chip RESET signal is not received before, OutR, OutG, OutB original pin output remains unchanged.

Automatic plastic transponder chip technology, signal attenuation without distortion, making the number of the chip unrestricted cascade signal transmission, only

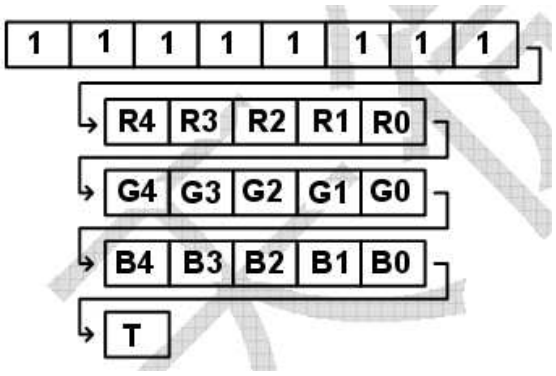
Restricted refresh speed requirements.

A data structure

Constant current mode commands:

After the on-chip power-on reset, the input data for each successive Din 24-bit for a complete packet, starting high, if high 8 [bit23bit16]

As a whole, the data packet is set constant, the following structure:



BIT23 - BIT16 whole is 1:00, which means that the following data set constant parameters

BIT15-BIT11 Set OUTR constant current output

BIT10-BIT6 Set OUTG constant current output

BIT5-BIT1 Set OUTB constant current output

BIT0 Test Mode bit

R [bit15 - bit11]: Set R-channel constant current value, Ir = 10 + R [4:0] mA, ie, minimum 10 +0 = 10mA, maximum 10 +31 = 41mA
G [bit10 - bit6]: Set G-channel constant current value setting mode ditto
B [bit5 - bit1]: Set B-channel constant current value setting mode ditto
T: Test Mode Bit 1: This bit is set, the test mode
0: This bit is cleared, the normal operating mode, OUT output PWM

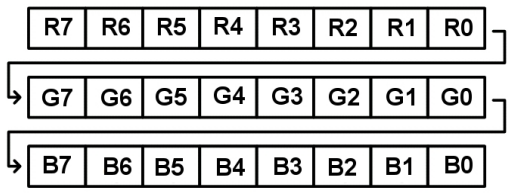
[Bit15bit1] bits are set independently OUTR, OUTG, OUTB pin output current value, the values range from 031, the corresponding constant in the following table Current value.

OutR	R4 Bit 15	R3 Bit 14	R2 Bit 13	R1 Bit 12	R0 Bit 11		
OutG	G4 Bit 10	G3 Bit 9	G2 Bit 8	G1 Bit 7	G0 Bit 6	Value	Current value (mA)
OutB	B4 Bit 5	B3 Bit 4	B2 Bit 3	B1 Bit 2	B0 Bit 1		
	0	0	0	0	0	0	10
	0	0	0	0	1	1	11
	0	0	0	1	0	2	12
	0	0	0	1	1	3	13
	0	0	1	0	0	4	14
	0	0	1	0	1	5	15
	0	0	1	1	0	6	16
	0	0	1	1	1	7	17
	0	1	0	0	0	8	18
	0	1	0	0	1	9	19
	0	1	0	1	0	10	20
	0	1	0	1	1	11	21
	0	1	1	0	0	12	22
	0	1	1	0	1	13	23
	0	1	1	1	0	14	24
	0	1	1	1	1	15	25
	1	0	0	0	0	16	26
	1	0	0	0	1	17	27
	1	0	0	1	0	18	28

1	0	0	1	1	19	29
1	0	1	0	0	20	30
1	0	1	0	1	21	31
1	0	1	1	0	22	32
1	0	1	1	1	23	33
1	1	0	0	0	24	34
1	1	0	0	1	25	35
1	1	0	1	0	26	36
1	1	0	1	1	27	37
1	1	1	0	0	28	38
1	1	1	0	1	29	39
1	1	1	1	0	30	40
1	1	1	1	1	31	41

PWM mode commands:

If 24bit data packets, the high 8 insufficiency 1, the packet is PWM setting data, and its structure is as follows:



BIT23-BIT16	Set OUTR output PWM duty cycle, can not be set to all 1s
BIT15-BIT8	Set the output PWM duty cycle OUTG
BIT7-BIT0	Set the PWM duty cycle output OUTB

Translated from: TM1829_V1.4-chin.pdf - by BNT - Date: 07.12.13 Page 07

Three-channel constant current LED driver TM1829

PWM duty cycle is continuously adjustable from 0-255, failure to pay attention to the high 8 1.

When high starting 24bit data transmission, sending data in the order of RGB. 24 split into three 8-bit data to send, pay attention to byte

High time between bytes RESET signal should not exceed the time, otherwise the chip will reset and reset again after receiving the data, the number can not be achieved

Data transmission.

Low-speed mode time

Symbol	Parameter	Test Conditions	Min	Typical values	Max	Unit
T0l	Enter 0 yards, low time	VDD = 5V GND = 0V	150	300	450	ns
T11	Input 1 yard, low time		600	800	1000	ns
T0l '	Output 0 yards, low time		--	340	--	ns
T1l '	Output 1 yard, low time		--	680	--	ns
T	0 yards or 1 yard cycle time		1200		--	ns
Treset	Reset yards, high time		140	500		μs

Note: Send the low-speed mode 1 yard or 0 yards cycle time is 1200ns (frequency 800KHZ).

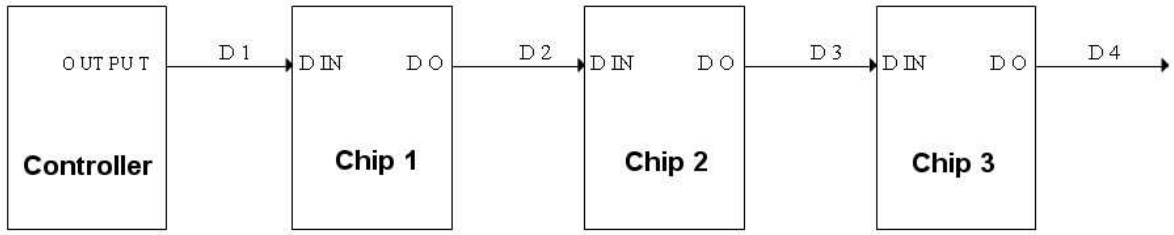
High-speed mode time

Symbol	Parameter	Test Conditions	Min	Typical values	Max	Unit
T0l	Enter 0 yards, low time	VDD = 5V GND = 0V	50	170	250	ns
T11	Input 1 yard, low time		300	450	550	ns
T0l '	Output 0 yards, low time		--	170	--	ns
T1l '	Output 1 yard, low time		--	340	--	ns
T	0 yards or 1 yard cycle time		600		--	ns
Treset	Reset yards, high time		140	500		μs

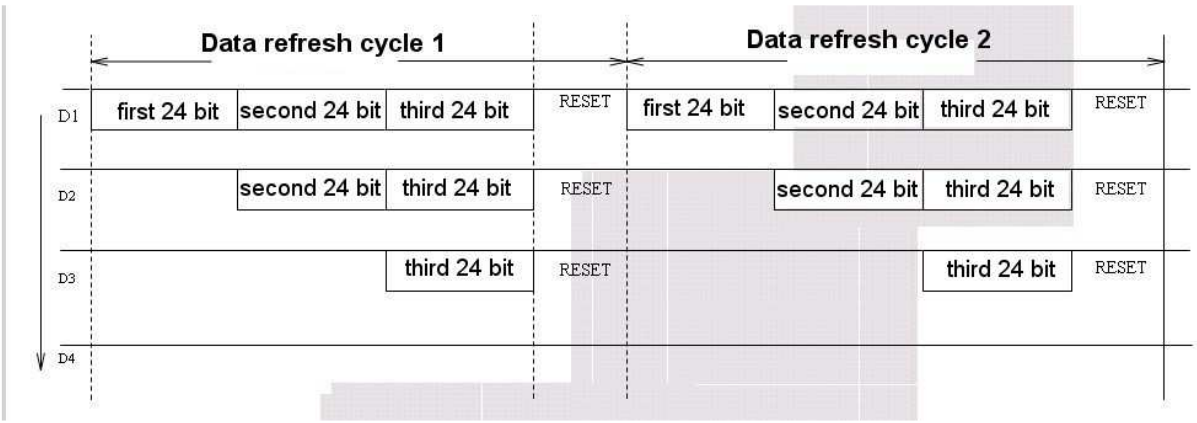
Note: Send one yard or 0 yards cycle time of 600ns high-speed mode (frequency 1.6MHZ). High and low speed mode Treset reset time is Same.

Three-channel constant current LED driver TM1829

data transmission and forwarding



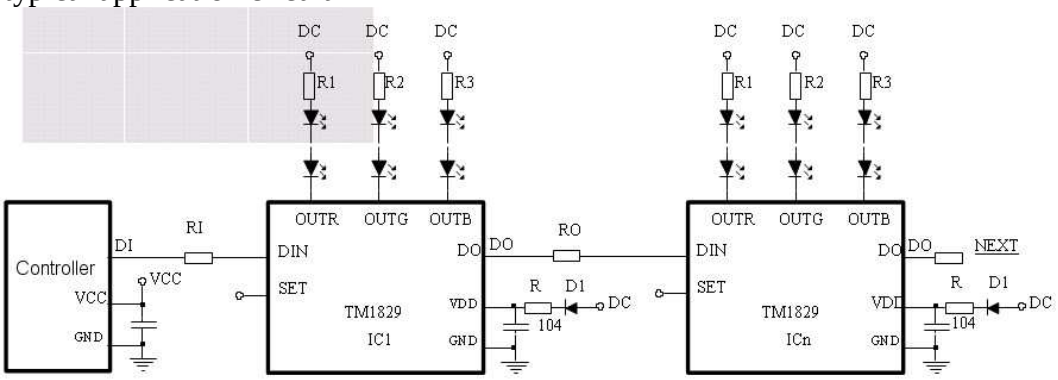
Wherein the data transmission controller D1, D2, D3, D4 concatenated data forwarded TM1829



Chip cascade process and the data transmission and forwards: the controller to send data (D1), when the receiving end of the first chip 1 24bit, chip 1 is not
Forwarding data (D2), then the controller continues to send data, and then receives a second chip 24bit, because there has been a first chip 24bit,
Therefore, the second chip 1 through DO forwarded 24bit chip transponder chip 1 to 2 receives data (D2), at this time, no transponder chip 2
Data (D3); controller continues to send data to the chip 1 is again received is forwarded to a third 24bit chip 2, since the chip 2 has also exists a
24bit, so 24bit transponder chip 2 is again the third (D3), the chip 3 receives the third 24bit, if at this time the controller sends a RESET

High signal, and put all the chips will be reset each received data decoding control 24bit RGB output port, complete a data refresh
Cycle. Chip went back to the reception state of readiness.

Application Information
a typical application circuit



Translated from: TM1829_V1.4-chin.pdf - by BNT - Date: 07.12.13 Page 09

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the power configuration
TM1829 can be configured DC6 ~ 24V voltage supply, but according to the input voltage is different, you should configure different power resistors,
Resistance Calculation: Since in practice, the power supply voltage decreases as the load increases. Therefore, the current flowing through VDD pin set at 4.5mA
Calculation, the series resistor to VDD R = (DC-5.0V) / 4.5mA (DC supply voltage).

List Configuration resistance typically as follows:

Supply voltage **DC**	Recommended **VDD** power interface and connection resistance value between
5V	Without resistor, the internal regulator does not work
6V	100
9V	750
12V	1,5k
24V	3,9k

When SET high termination, should be connected at VDD, prohibit access external power VCC, to prevent chip breakdown. Recommended terminating the anti-reverse power input Diodes to protect the chip.

how to calculate the data refresh rate
Update time is based on a cascade system to calculate the number of pixels, usually a set of RGB pixel requires a
TM1829 chip to control.
Calculated in accordance with the high-speed mode:
A maximum transmission rate of BIT 600ns (frequency 1.6MHZ), a pixel data including red (8BIT), green (8BIT), blue (8BIT)
Total 24BIT bit, the transmission time of 24 × 0.6μS = 14.4μS, if a system total of 2000 pixels, a refresh of all displays
Inter was 14.4 μS × 2000 = 28.8mS (RESET code ignores the time), that a second refresh rate: 1 ÷ 28.8 × 1000 ≈ 34.7Hz.

Low-speed mode refresh rate minus twice the corresponding high-speed mode.
The following is a cascade of dots corresponding to the highest form of data refresh rate:

	High-speed mode		Low-speed mode	
Pixel	Number of fastest refresh According to Time (**mS**)	Maximum refresh rate (**Hz**)	Number of fastest refresh According to Time (**mS**)	Maximum refresh rate (**Hz**)
1500	7.2	138	14.4	69
1800	11.52	87	23.04	44
11000	14.4	69	28.8	35
11500	21.6	46	43.2	23
11800	25.92	38	51.84	19
12000	28.8	35	57.6	17

If the system is less demanding on the data refresh rate, the number of cascaded pixel matrix is not required, as long as the power supply is normal, theoretically available TM1829 Infinite cascade.

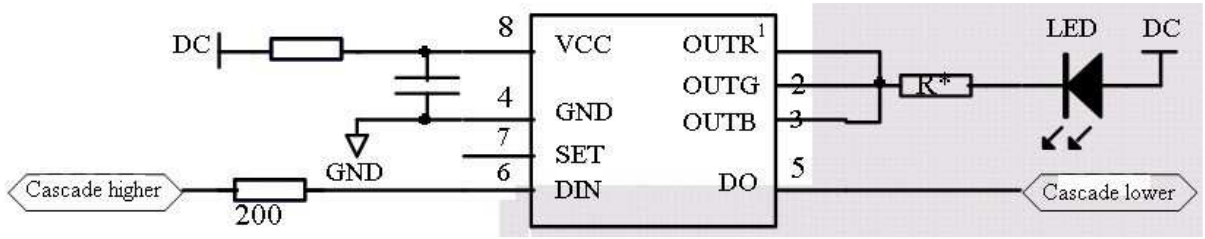
how to work in the best constant state TM1829

TM1829 output constant current drive, based on the constant current output curve shows that at 41mA constant current, constant region into the OUT terminal voltage required for the 1.2V or more, then the chip only constant effect, but not this OUT terminal voltage higher the better, the higher the voltage, the greater the reduction in power consumption of the chip, the chip
Severe fever, reducing overall system reliability, it is recommended that when the turn-on voltage Vout OUT terminal control between 1.23V better, common side series resistor
Type may be used, the following is the choice of resistance theoretical calculations:
System drive voltage: VDD
Single LED voltage drop: Vled
Series LED number: n
Constant Value: Iout

Constant Voltage: 1.5V
Resistance: R
R = (VDD-1.5-n × Vled) / Iout
Example: power supply 24V, single LED forward voltage: 2V, LED series number: 6, 40mA constant current value
Series resistance should be: R = (24-1.5-2 × 6) / 0.04 = 262.5Ω, just about 260Ω resistor in series to the OUT pin

using the TM1829 how expansion flow
TM1829 each OUT terminal maximum output only 41mA constant current, constant value if the user needs to expand the drive, which can be short-circuited end after three OUT
Use every one OUT shorted end, and will increase the maximum current value 41mA, three-way pick up after a short constant around 123mA, but the disadvantage of this method

Software is required in conjunction with control values were written three sets of registers, the advantage is precisely to get the desired current value and the constant current is large.



TM1829

with a process-driven approach LED

5.1 To achieve chip LED brightness control, first make sure that RGB port voltage, enabling the chip to enter the constant work (specific reference to "constant Curve ");

5.2-chip power-on reset initializes the first set of constant values and the test mode bit T is 0 (allow PWM outputs), such as setting the output through
RGB channel constant current of 20mA, then the maximum current is allowed to flow through to 20mA. Current value should be set according to LED;

5.3 pairs of PWM register is written, set the PWM output, as set PWM output channel RGB luminance level is 100, then flows through the LED
Current is 100 ÷ 256 × 20mA = 7.8mA;

5.4 PWM values constantly changing, we can arbitrarily adjust the brightness of the LED. Set PWM value is 0, the output full-height, LED off. Set PWM
Value FFH (Note 24BIT not all high 8 1), the largest low duty cycle of the output waveform, LED brightest.

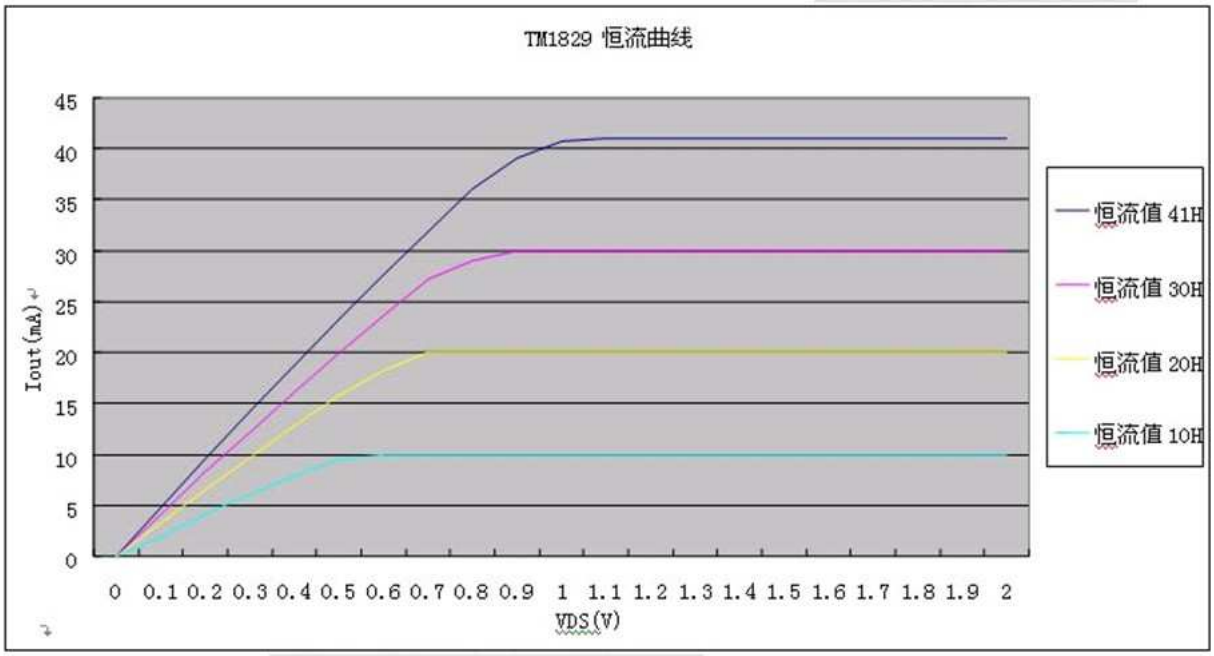
5.5 If the current value is set and the test mode bit T is 1, then enter the test mode.
Note: To avoid the chip after powering off the controller does not cause initialization set register values lost constant, constant current
Changes suggested in the course of the PWM register refresh refresh timer constant register or re-register constant refresh refresh PWM register.

Translated from: TM1829_V1.4-chin.pdf - by BNT - Date: 07.12.13 Page 11

Three-channel constant current LED driver TM1829

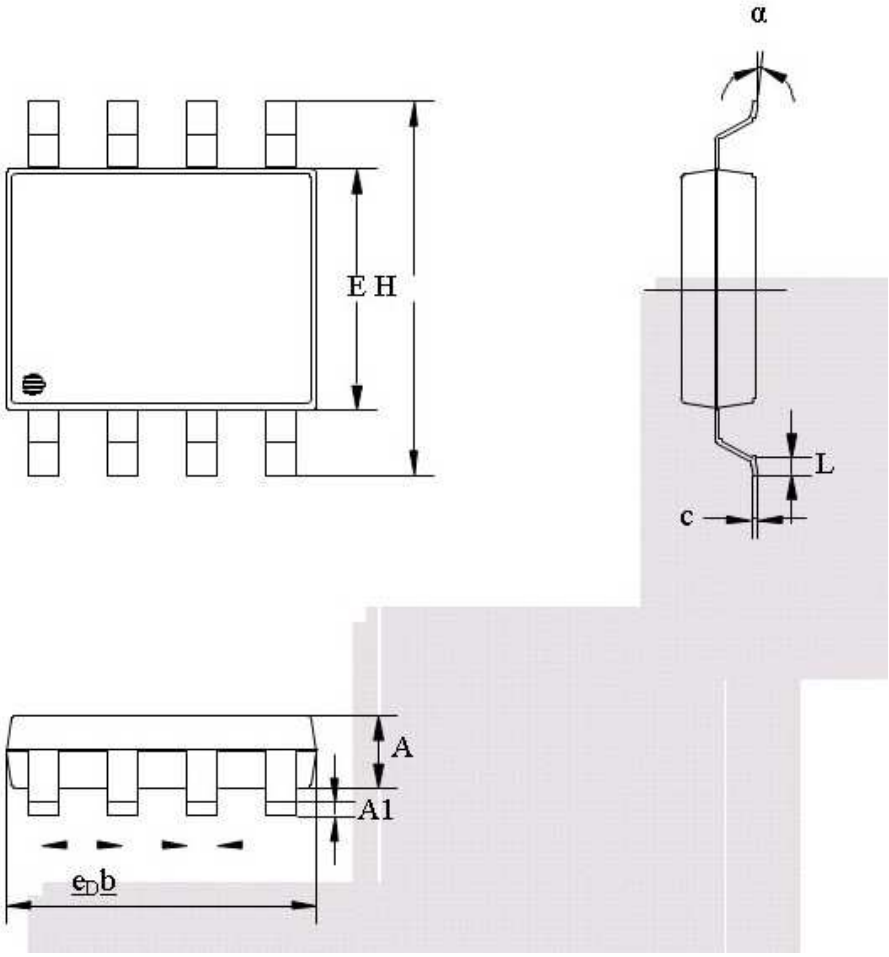
Constant Curve
The TM1829 is applied to the LED panel design on time, even between ICs minimal between channels. This stems from the excellent characteristics TM1829
Sex:
When the load terminal voltage changes, the output current is not affected its stability, as shown below
As shown in Figure, the current Iout voltage Vds output port to the port and the relationship shows that, when working in a constant state, the port

The output of the constant current value Iout, Iout constant current is smaller, Vds need the smaller the minimum can not be less than 0.8V.



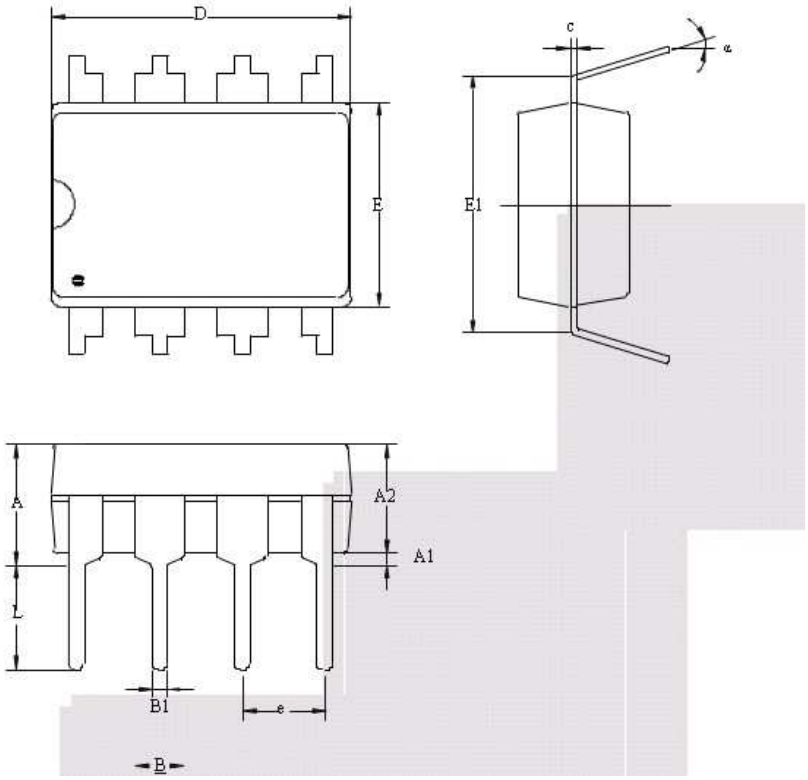
Three-channel constant current LED driver TM1829

Package Drawing (SOP8)



	Inch			Millimeter		
Grade	Least	Standard	Maximum	Least	Standard	Maximum
A	0.051	0.059	0.067	1.30	1.50	1.70
A1	0.002	0.006	0.010	0.06	0.16	0.26
b	0.012	0.016	0.022	0.30	0.40	0.55
c	0.006	0.010	0.014	0.15	0.25	0.35
D	0.186	0.194	0.202	4.72	4.92	5.12
E	0.148	0.156	0.163	3.75	3.95	4.15
e		0.050			1.27	
H	0.224	0.236	0.248	5.70	6.00	6.30
L	0.018	0.026	0.033	0.45	0.65	0.85
α	0°		8°	0°		8°

Package Drawing (DIP8)



	Inch			Millimeter		
Grade	Least	Standard	Maximum	Least	Standard	Maximum
A			170			4.31
A1	0.015			0.38		
A2	0.124	0.134	0.144	3.15	3.4	3.65
B	0.015	0.018	0.020	0.38	0.46	0.51
B1	0.050	0.060	0.070	1.27	1.52	1.77
C	0.008	0.010	0.012	0.20	0.25	0.30
D	0.352	0.362	0.372	8.95	9.20	9.45
E	0.242	.0252	0.262	6.15	6.40	6.65
E1		0.300			7.62	
e		0.100			2.54	
L	0.118	0.130	0.142	3.00	3.30	3.60
α	0°		15°	0°		15°

All specs and applications shown above subject to change without prior notice.
(The above specifications are for reference circuit and, if the Company be amended without further notice)

Translated from: TM1829_V1.4-chin.pdf - by BNT - Date: 07.12.13 Page 14

Three-channel constant current LED driver TM1829

Revision History

Version	Date of issue	Amendments Introduction
V1.0	2011-12-21	The official version
V1.1	2012-02-22	Revision
V1.2	2012-05-08	Revision issue
V1.3	2012-06-21	Revision issue
V1.4	2013-01-04	Revision issue