Entertainment Services and Technology Association

United States Institute for Theatre Technology, Inc.

DRAFT

BSR E1.11, Entertainment Technology - USITT DMX512 Asynchronous Serial Digital Data Transmission Standard for Controlling Lighting Equipment and Accessories

Revision 1.1a

Inside Cover

The **United States Institute for Theatre Technology, Inc**. (USITT) is the Association of Design, Production, and Technology Professionals in the Performing Arts and Entertainment Industry. Founded in 1960, the mission of the Institute is to advance the professions of design and technology in the performing arts by disseminating information, actively promoting the advancement of knowledge and skills and facilitating national and international communication among its members. USITT is the United States Center of OISTAT, the International Organization of Scenographers, Theatre Architects and Technicians.

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The **Entertainment Services and Technology Association** (ESTA) is a non-profit trade association representing the North American entertainment technology industry. Its members include dealers, manufacturers, manufacturer representatives, service and production companies, scenic houses, designers and consultants. The Association addresses areas of common concern such as technical standards, customer service, equipment quality, business practices, insurance, and credit reporting, and provides a wide variety of services to Members.

ESTA's Technical Standards Committee (TSC) is accredited by the American National Standards Institute (ANSI) as Accredited Standards Committee *E1, Safety and Compatibility of Entertainment Technical Equipment and Practices* with ESTA as its Secretariat. This accreditation means that the ESTA Technical Standards Program for standards-making has passed a detailed scrutiny by ANSI to insure that it meets the most stringent requirements for fairness and proper public review of proposed ESTA standards. The accreditation allows ESTA to submit standards for the ANSI public review and comment process, and then publish them as ANSI standards. The ESTA Technical Standards Program is now the only ANSI-accredited standards-making program dedicated to the needs of entertainment technology.

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Foreword

The original version of the DMX512 Standard was developed in 1986 by the Engineering Commission of the United States Institute for Theatre Technology, Inc. (USITT). Minor revisions were made in 1990. DMX512 has gained international acceptance throughout the entertainment industry, even though USITT is not formally accredited as a standards making body. The earlier versions of this Standard covered only data used by dimmers. In practice this Standard has been used by a wide variety of devices; this version recognizes this fact.

In 1998, it became evident that additional updates to the Standard were necessary and formal recognition through an internationally recognized standards organization was required. The USITT DMX512 Subcommittee issued a Call for Comments in order to solicit recommendations for changes to the Standard. At the same time, USITT transferred maintenance of DMX512 to the Entertainment Services and Technology Association (ESTA), which is the secretariat for the ANSI Accredited Standards Committee *E1, Safety and Compatibility of Entertainment Technical Equipment and Practices* (more commonly known as the ESTA Technical Standards Program - TSP).

A Task Group established under the ESTA TSP's Control Protocols Working Group acted on the proposals received in response to the Call for Comments. The primary goal was to make editorial updates to DMX512 appropriate for current times, including the addition of technical features while maintaining a balance with backward compatibility. Many proposals, while technically innovative, could not be accepted because their implementation would not have been backward compatible and would have immediately rendered obsolete most of the installed base of equipment.

This document is a result of the actions taken on those proposals and subsequent development under the *Policies and Procedures* of the ESTA Technical Standards Program.

1 General

1.1 Scope

This Standard describes a method of digital data transmission between controllers and lighting equipment and accessories, including dimmers. It covers electrical characteristics, data format, data protocol, connector type, and recommended cable types.

1.2 Definitions

1.2.1 Accessory Power: A 24 VDC supply used to power the electronics and control/drive functions of a product which does not then require connection to mains voltages. Frequently known as scroller power but not in fact restricted to use with scrollers.

1.2.2 Asynchronous: Signals that start at any time and are not locked or synchronized to the receiving device by a separate clock line.

1.2.3 Balanced Line: a data communications line where two wires are present, the signal and its opposite (complement), the actual signal being the difference between the voltages on the two wires. Balanced lines have excellent noise and interference rejection properties.

1.2.4 Baud Rate: the rate in bits per second at which serial information is sent.

1.2.5 Bit: smallest unit of data processing information. A bit assumes the value of either 1 or 0.

1.2.6 Break: a high to low transition (space) followed by a low of at least 88 microseconds.

1.2.7 Byte: a data unit of 8 bits.

1.2.8 Common: see Data Link and Signal Common.

1.2.9 Common-Mode Voltage: a voltage appearing equally on the data + (plus) and data - (minus) lines relative to signal common. $Vcm = (Va + Vb)/2$ where:

Vcm is the Common Mode Voltage
Va is the voltage on DMX512 Pin 2 with respect to Pin 1
Vb is the voltage on DMX512 Pin 3 with respect to Pin 1

1.2.10 Controller: a transmitting device that originates DMX512 data.

1.2.11 Data +: true signal.

1.2.12 Data -: complimentary signal.

1.2.10 Data Link: physical connection between transmitting and receiving devices.

1.2.11 Data Link Common: The connection to signal common at the point of interconnection (DMX512 Port) of the product.

1.2.12 Dimmer: a Receiving Device which controls the intensity of light.

1.2.13 DMX512 Port: see Port.

1.2.14 DMX512 Processing Device: A piece of equipment that regenerates the timing of any DMX512 packet or has provision for other signal inputs from which the outgoing DMX512 packet is generated. In the absence of any DMX512 transmitting capability, the device has provision for other signal outputs which are controlled in some manner by the incoming DMX512 packet. Basic buffer products are not normally considered processing devices.

1.2.14 Driver: the circuit which drives the transmit signal and is directly connected to the DMX512 line. See Line Driver.

1.2.15 Earth Ground: a conducting connection, whether intentional or accidental, between an electrical circuit or equipment and the Earth, or to some conducting body that serves in place of the Earth.

1.2.16 EMC: Electromagnetic Compatibility. Electrical and electronic equipment may have a requirement to meet various regulatory standards for EMC. Usually specified in terms of emission and immunity performance standards.

1.2.17 EMI: Electromagnetic Immunity; see EMC.

1.2.18 Frame: a Start Bit, followed by a Byte and 2- Stop Bits.

1.2.19 Galvanic Isolation: circuit topology in which the output is completely electrically disconnected from the input.

1.2.20 Idle: the time that the DMX512 line is idle (high) and not sending any information (also known as the 'Mark' condition).

1.2.21 In-Line Device: any component that receives and re-transmits DMX512.

1.2.22 Isolation: see Galvanic Isolation.

1.2.23 Isolation voltage: voltage specification between input and output stages of a galvanically isolated system at or below which damage or breakdown of circuit components will not occur.

1.2.24 Legacy Equipment: DMX512 transmitting and receiving devices claiming compliance with DMX512 or DMX512/1990.

1.2.25 LEN: (Load Equivalent Number) the number or fractions of Unit Loads as defined by EIA-485.

1.2.26 Line Driver: electrical circuit providing differential voltage excursions on a data link, operating within a defined Common Mode voltage range and with a specified response to overload and overvoltage conditions.

1.2.27 Line Receiver: electrical circuit allowing detection of differential voltage excursions on a data link, operating within a defined Common Mode voltage range and with a specified response to overload and overvoltage conditions.

1.2.28 Loop-Through Connection: A connector or terminal port which connects the signals present on at least Pins 1, 2 and 3 of one port to another port. Frequently abbreviated to Loop or Thru.

1.2.29 NULL START Code: START Code with a value of 00h.

1.2.30 Manufacturer ID: 2 byte value assigned to a Manufacturer/Organization by the E1 Accredited Standards Committee for use with Alternate START Codes 91h and CFh. This ID serves as an identifier that the data following in that packet is proprietary to that entity and should be ignored by all others.

1.2.31 Mark: a line condition where Signal True is high with respect to Signal Complement.

1.2.32 MAB (MaB): Mark After Break – the period of time between the low to high transition which signifies the end of Break and the high to low transition which is the start bit of the START Code.

1.2.33 MBB (MbB): Mark Before Break – the period of time between the end of the last stop bit of the last Slot and the high to low transition which signifies the start of Break.

1.2.34 Merge Unit: Product comprising one or more receiving devices and one or more transmitting devices that generate a DMX512 packet derived from the manufacturers declared logical combination of the DMX512 input packets.

1.2.35 Packet: Reset Sequence followed by all slots up to a Mark Before Break and the start of next Reset Sequence.

1.2.36 Port: a DMX512 signal connection point (connector or terminal strip).

1.2.37 Reset: see Break.

1.2.38 Reset Sequence: a sequence of a Break, Mark After Break, and properly framed START Code.

1.2.39 Receiver: see Line Receiver.

1.2.40 Receiving Device: a piece of equipment which accepts a DMX512 signal.

1.2.41 Signal Common: the common reference (zero volt supply) of the EIA-485 driver or receiver circuitry.

1.2.42 Slot: a sequentially numbered data Frame in a DMX512 packet. A single Universe contains a maximum of 512 Slots, starting at Frame 1. Frame 0 is the START Code.

1.2.43 Slot Footprint: The number of consecutive slots of data used by a product in its operation.

FPN: A 24 way dimmer rack may have a footprint of 24, it may be more if some slots are used to provide additional control functions using NULL START Code packets. Automated fixtures are renowned for having many and various slot footprints.

1.2.44 Space: a line condition where Signal True is low with respect to Signal Complement.

1.2.45 Start Bit: the extra bit attached to the beginning of a byte to indicate to the receiver that a new byte is being sent. The start bit is always low, i.e., Space.

1.2.46 START Code: the first byte send after Break, indicating the type of information to follow.

1.2.47 Stop Bit: the extra bit(s) attached to a byte to indicate the end of the byte – DMX512 has 2 stop bits. The stop bit is always high, i.e., Mark.
1.2.48 Terminator: device or circuit topology which is designed to minimize unwanted signal reflections on a data link.
1.2.49 Transmitting Device: a piece of equipment which produces a DMX512 signal.
1.2.50 Universe: a DMX512 data link originating from a single DMX512 source. Control of up to 512 DMX512 slots comprises a single universe.
1.2.51 Update (Refresh) Rate: the number of DMX512 packets sent per second.

1.3 Applicability

This Standard is intended as a guide for:

1. Equipment manufacturers and system specifiers who wish to integrate systems of lighting equipment and accessories, including dimmers, with controllers made by different manufacturers.
2. Equipment manufacturers seeking to adopt a standard controller-lighting equipment digital transmission protocol.
3. System specifiers and consultants to gain detailed information about recommended cable types and allowed connectors.
4. End users to identify possible problems with the interconnection and communication of DMX512 equipment.

Use of this Standard is strictly voluntary. Furthermore, it is not intended as a replacement for existing protocols already manufactured, but rather as an addition to existing protocols which will broaden the installed base of controllers and lighting equipment that can communicate with each other.

1.4 Appropriate uses of this Standard

Equipment designers and general users of this Standard must recognize that this Standard is intended to fill only a limited range of uses. Other standards will be more appropriate for different uses. This is not intended to be a venue wide network that can carry data for lighting, sound, and scenery mechanization, for example, all on the same wire. The basic protocol is made up packets that are blocks of un-typed data. Receivers must know what to do with the data simply by knowing the data's position in the block.

This Standard performs no error checking of NULL START Code packets. There is no assurance that all DMX512 packets will be delivered. It is common practice for merge units and protocol convertors to drop packets that they cannot process in a timely manner. The 1986 and 1990 versions of the Standard specifically allow dimmers to ignore packets that they cannot process in a timely manner, and this concept survives in this version of the Standard with respect to NULL START Code packets.

1.5 Classes of data appropriate for transmission over links designed to this Standard

DMX512 is designed to carry repetitive control data from a single controller to one or more receivers. The control data should be used to control dimmers, other lighting control devices and related non hazardous effects equipment.

1.6 Classes of data appropriate for transmission using Non-NULL START Codes

It is recommended that most data be sent in NULL START Code packets since they are universally supported. Nevertheless, where configuration data, data requiring a structured format, or data requiring checksum or other error checks are sent, the use of registered Non-NULL (Alternate) START Codes is appropriate.

1.7 Classes of data not allowed on this Standard

DMX512 is not an appropriate control protocol for hazardous applications, including but not limited to Pyrotechnic Control and Scenery Mechanization.

Data that controls any device that has a reasonable potential to cause serious physical injury shall not be transmitted over data links built to this Standard. No one shall make, market, or sell such a system while claiming to be DMX512 or DMX512 compatible or any similar such wording.

1.8 Limitations

This Standard makes specific but limited reference to the provision of two classes of DC power for use with accessories and limited current remote control devices. The detailed topology and recommended cable types for the distribution of voltage and current for use with accessories is beyond the scope of this Standard.

1.9 Compliance

Compliance with this Standard is the responsibility of the manufacturer, and such markings and identification or other claims of compliance do not constitute certification or approval by the E1 Accredited Standards Committee. See clause 12 for Marking and Disclosure requirements and Annex E for Protocol Implementation Compliance Statement (PICS).

1.10 Cross Reference

See standard *TIA/EIA-485 Electrical Characteristics of Generators & Receivers for Use in Balanced Digital Multipoint Systems (ANSI/EIA-485-A-98)* issued by:

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Arlington , VA 22201-3834 USA
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Telecommunications Industry Association
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and available from: Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112 USA
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This standard will be referred to as EIA-485 in this document.

2 Electrical Specifications and Physical Layer

2.1 General

Except where specifically called out in this document the electrical specifications of this Standard are those of EIA-485. Where a conflict between EIA-485 and this document exists, this document is controlling as far as this Standard is concerned.

The physical layer of a DMX512 data link is constrained by earth grounding practices, termination methods, signal levels, EMC, EMI, protection against ESD, and accidental damage by connection to other devices.

Equipment designers shall pay particular attention to EIA-485 requirements for line drivers, line receiver design, line voltage levels, line loading, and the Common Mode requirements of EIA-485. Further, equipment designers must comply with the non EIA-485 requirements of clauses 3 and 4.

2.2 Electrical isolation

EIA-485 makes no general provisions for electrical isolation. However, this Standard does, and suitable optical isolation, transformer isolation, or other means may be employed to prevent the undesirable propagation of voltages which exceed the Common Mode limits of EIA-485 (see clauses 3 and 4). The inclusion of such isolation does not, however, alter the requirement that a transmitter or receiver conform to EIA-485.

2.3 EMC compliance

This Standard and EIA-485 make no general provisions for Electro Magnetic Compatibility (EMC) emissions or immunity or other regulations to which manufacturers may be obligated to conform.

2.4 Topology

A data link shall consist of a single differential line driver, a terminated transmission line and one or more differential line receivers. The transmission line shall be a data cable with a nominal characteristic impedance of between 100 to 150 ohms as specified in clause 11. The differential drivers and receivers shall meet the requirements of EIA-485 and all additional requirements of this Standard.

At any time only one driver shall connect to the data link. There are no general provisions in the software protocol for controlling switching between multiple data link drivers.

This version of the Standard provides for a defined means of returning data from dimmers and other devices to a console, status monitor or other device, using a secondary EIA-485 data link. The particular requirements relating to topology and termination of the secondary data link used for this facility are described in detail in Annex B.

2.5 Data link common and grounding topologies

Various paragraphs of clause 3 deal with shield earth grounding topologies. In all cases there shall be a low impedance connection between Pin 1 of the DMX512 port and signal common of the EIA-485 driver or receiver circuitry. The impedance of this path shall not be greater than 100 ohms. Note that in some cases, this impedance is limited to 0.2 ohms, and is often zero ohms.

2.6 Preferred method of earth grounding data link common

Where possible, DMX512 systems should make use of ground referenced transmitting devices and isolated receiving devices. This approach provides for a single point solid ground/chassis connection at the source, and allows for variations in building ground potentials between transmitting and receiving devices. This is to ensure that interoperability of equipment is achieved in situations that do not in their own right constitute a safety hazard, but might otherwise exceed the Common Mode limitations of EIA-485. See EIA-485 clause 4.5.2.

2.7 Data termination procedures

DMX512 data links should be terminated to eliminate ringing and signal reflection which can cause mis-operation of an otherwise properly designed system.

In most systems utilizing equipment claiming compliance with this Standard, the driver will be placed at one extremity of the data link used (cable). However, this is not mandatory. If the driver is placed at one extremity of the data link, the driver end of the data link need not be terminated. If the driver is placed at any point other than at the extremity, then the driver shall not be terminated and both extremities of the transmission line shall be terminated with networks matching the characteristic impedance of the line.

Manufacturers of receiving devices may provide internal termination of the data link. Where such termination is provided, it shall comply with the electrical and marking requirements of this Standard.

The termination topology shall be AC, rather than the DC model of earlier revisions of this Standard. AC termination networks shall consist of a series RC network. The resistance shall be equal to the characteristic impedance of the transmission line – 120 Ohms in series with 0.047µF. Termination components shall be chosen to withstand continuous voltages of at least 30 VAC/42 VDC. Provision of AC termination shall be declared as part of the TYPE mark as defined by clause 12.4 of this Standard.

To comply with this Standard, all equipment connected to a DMX512 data link shall operate in accordance with the stated manufacturer's specification when the data link is terminated with an external legacy DC model terminator (100-120 Ohms between Data + and Data-).

Unpowered connected DMX512 devices shall not degrade the performance of the DMX512 transmission system.

2.8 Port designations

A DMX512 port shall always provide for a primary data link with signals as defined in clauses 5 though 7. Provision may optionally be made for a secondary data link, a talkback data link or for limited current DC power.

2.8.1 Pin reference

Terminals and connector contacts are referred to as Pins in this Standard. Where the use of a particular style of connector is required by this Standard, pinout details are fully specified. Each DMX512 port on a device shall reference its functionality of Pins 4 and 5 by means of the designations detailed in table 2.8.2.1. Data link common is Pin 1, and the primary data link is defined on Pins 2 and 3.

2.8.2 TYPE classifications

A DMX512 port shall be classified as belonging to one of seven types listed in table 2.8.2.1.

Table 2.8.2.1 - TYPE classifications for DMX512 equipment

TYPE	Symbol	Description	Comment
TYPE 0	→	unidirectional DMX512 data Pins 2, 3 ONLY (EIA-485 levels)	no connection to Pins 4,5
TYPE 1	→ ═	unidirectional DMX512 data Pins 2, 3 (EIA-485 levels) AND loop-through on Pins 4, 5	direct wire or link connection of Pins 4 and Pins 5 on looping in/out connection. No other internal connection to these pins allowed.
TYPE 2	→ →	unidirectional DMX512 data Pins 2, 3 and unidirectional DMX512 data Pins 4, 5 (EIA-485 levels)	Two universes of DMX512
TYPE 3	→ ←	unidirectional DMX512 data Pins 2, 3 and return signals on Pins 4, 5 in accordance with talkback protocol as defined in Annex B	Interconnection of equipment of TYPE 3 has specific topology restrictions
TYPE 4	→ ←→	unidirectional DMX512 data Pins 2, 3 (EIA-485 levels) and any other signals on Pins 4, 5 using EIA-485 levels	refer to manufacturers instructions
TYPE 5	→	unidirectional DMX512 data Pins 2, 3 (EIA-485 levels) and NON-EIA-485 300 mA max current limited signals not exceeding -0 VDC / +12 VDC nominal tied to both Pins 4 & 5, and/or receiving devices that tie Pin 1 directly to Protective Ground.	Voltage on these pins must not cause damage to legacy equipment – see clause 3 for restrictions on implementing TYPE 5 product; refer to manufacturers instructions
TYPE 6	✍→✇ □▬▬▬□	Test Equipment capable of transmitting and/or receiving and evaluating DMX512 data on Pins 2, 3. Characteristics of Pins 1, 4, 5 not defined	refer to manufacturers instructions; note that in some operation modes, other parts of this Standard may not be adhered to

Note: References to unidirectional data are with respect to a transmitting device.

Different physical ports on a product may be of different TYPEs.

FPN: For example, a lighting controller may have two TYPE 0 ports and a TYPE 3 port; an entry level 6-way dimmer pack may have a single TYPE 0 port, or it may have a TYPE 5 port because it provides DC power to feed an entry level controller.

A concession to provide for 24 VDC accessory power requires the use of an alternate connector and is limited to products with only a primary data link. See clauses 9.1 and 10.4.

Table 2.8.2.2 - Signal designations summary

Function	Pin Reference within Standard	Legacy Product	TYPE 0	TYPE 1	TYPE 2	TYPE 3	TYPE 4	TYPE 5
Data Link Common	**1**	Common (Screen)	Common (Screen)	Common (Screen)	Common (Screen)	Common (Screen)	Common (Screen)	Common (Screen)
Primary Data Link	**2**	Data 1-	Data 1-	Data 1-	Data 1-	Data 1-	Data 1-	Data 1-
	3	Data 1+	Data 1+	Data 1+	Data 1+	Data 1+	Data 1+	Data 1+
Secondary Data Link / Talkback / Limited Current Supply	**4**	various	no connection	Loop-through (passive link)	Data 2-	Talkback -	various Data 2-	12 VDC 300 mA limited
	5	various	no connection	Loop-through (passive link)	Data 2+	Talkback +	various Data 2+	12 VDC 300 mA limited

WARNING: While the generic reference to Pins 1- 5 correlates to the physical pinout used on the XLR style connectors as defined in clause 10 of this Standard, there are other situations where different physical pinouts may be encountered

2.9 Talkback

TYPE 3 systems use the standard talkback scheme as defined in Annex B.

FPN: Products with other talkback schemes are permissible and would fin into the TYPE 4 classification. However, no level of cross-manufacturer interoperability of TYPE 4 talkback schemes could be assumed from compliance with this Standard.

2.10 Device interconnection

The TYPE classification of ports on products compliant with this Standard provides for a consistent means of predicting and utilizing features which were not clearly identified in earlier revisions of the Standard. Manufacturers will be required to mark and make available basic information about their products in accordance with clause 12.

2.12 Galvanic isolation from protective ground

DMX512 transmitting and receiving devices may be galvanically isolated. Should a transmitting or receiving device be galvanically isolated, it shall comply with the protection requirements defined by this Standard.

This Standard defines particular grounding and galvanic isolation topologies which must be followed in order to allow the use of the term “isolated” within the port TYPE mark. These topologies are described in clause 3.

3 Nominal Operating Characteristics

3.1 General

Operation limits generally follow the detailed requirements of EIA-485 for generator characteristics. Where appropriate, separate limits are given for galvanically isolated products.

3.2 Transmitter characteristics

All electrical characteristics shall be measured at the output terminals of the product. Transmitting devices shall deliver open circuit output voltage not less than 1.5V and not more than 6V as defined in EIA-485 clause 4.2.1

Transmitting devices shall comply with the requirements of EIA-485 clause 4.2.2 for differential and offset output voltages, which requires that the magnitude of the differential output voltage be not less than 1.5V and not more than 5V when connected to a test load of two 27 ohm resistors.

The requirements of EIA-485 clause 4.2.2 for generator offset voltage and EIA-485 clause 4.2.3 for Differential Output voltage (Common Mode loading) shall be met.

The requirements of EIA-485 clause 4.2.4 for Off-state output current shall be met, provided that the Unit load for the generator in the off state does not exceed 1.

Transmitting devices shall comply with the requirements of EIA-485 clause 4.2.7, for which the unit interval (t_{ui}) shall be regarded as 4 microseconds.

In battery operated equipment or equipment which has no inherent provision for connection to protective ground, chassis shall be deemed to be any exposed metal connector parts which do not carry signals. All such parts shall be at equal potential.

For Isolated devices, a capacitor shall be fitted between Pin 1 and chassis for the purpose of Radio Frequency bypass. The value of this is not mandated by the Standard, but is expected to be in the range 0.001-0.1µF.

All transmitting device outputs shall meet the following conditions in table 3.2 during normal operation under open circuit condition.

Table 3.2 Transmitter characteristics

Connection	Limit		Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	0 ≤ v ≤ +6 VDC		
Pin 4 to Pin 1 or Pin 5 to Pin 1	0 ≤ v ≤ +6 VDC		TYPE 0 - TYPE 4 Ports Only
Pin 4 to Pin 1 or Pin 5 to Pin 1	+12 VDC ± 4% current limited to 600 mA		note 1
Pin 4 to Pin 5	0 (no differential allowed)		note 1
Chassis to any Pin	≥ 22M ohm @ 42 VDC		Isolated Devices Only
	Ground Referenced	Galvanically Isolated	
Pin 1 to Chassis	0V	N/A	note 2
Pin 2 to Chassis or Pin 3 to Chassis	0 ≤ v ≤ +6 VDC	N/A	
Pin 4 to Chassis or Pin 5 to Chassis	0 ≤ v ≤ +6 VDC	N/A	TYPE 0 - TYPE 4 Ports Only
Pin 4 to Chassis or Pin 5 to Chassis	0 ≤ v ≤ +12 VDC	N/A	note 1
Pin 2 to Pin 3	+/- 6V (open circuit)	+/- 6 V	
Pin 4 to Pin 5	+/- 6V (open circuit)	+/- 6 V	

Notes:

1) This concession is ONLY available for equipment claiming compliance as TYPE 5 and marked in accordance with the provisions of this Standard.

2) Ground Referenced transmitting devices shall have a direct connection between Pin 1 and chassis.

3.3 Earth grounding of data link common for transmitters

In recognition of the need for DMX512 compliant product to be capable of interconnection as part of large and potentially complex systems, this Standard defines two allowable topologies for the earth grounding of data link common and signal common for transmitters, to be known as “Ground Referenced” and “Galvanically Isolated”.

3.3.1 Ground referenced transmitters

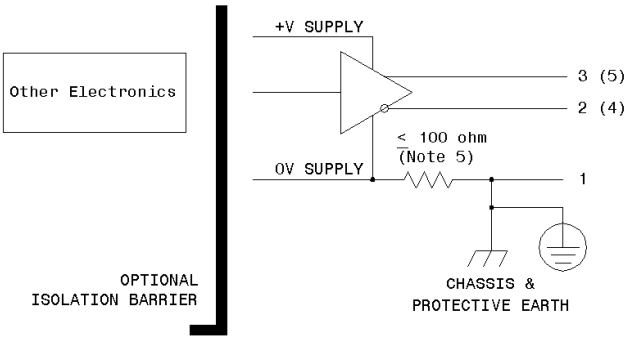

Figure 3.3.1 - Ground Referenced Transmitter

Notes Figure 3.3.1:

1) Output connections shall be marked in accordance with that detailed for Ground Referenced transmitter.

2) The existence of any isolation barrier does NOT qualify output for marking as ISOLATED.

3) Product shall be provided with provision for connection to protective earth.

4) Pin 1 to Chassis connection shall satisfy tests as defined in clause 4.6.

5) Manufacturers shall be permitted to fit a resistor as per clause 2.5.

3.3.2 Galvanically isolated transmitters

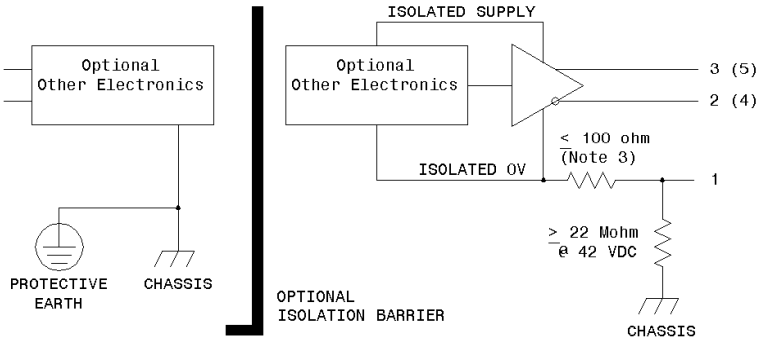

Figure 3.3.2 - Galvanically Isolated Transmitter

Notes Figure 3.3.2:

1) Any pin of the DMX512 output shall present an impedance $\geq$ 22 Mohm at 42 VDC with respect to Chassis, with respect to Protective Ground (where fitted), and with respect to any other signal inputs or outputs.

2) Adherence to this topology allows DMX512 transmitter connection to be marked as ISOLATED. In such cases, the power supply for the driver electronics will be floating.

3) Manufacturers shall be permitted to fit a resistor as per clause 2.5.

3.4 Receiver characteristics

For isolated devices, a capacitor shall be fitted between Pin 1 and chassis for the purpose of Radio Frequency bypass. The value of this is not mandated by the Standard, but is expected to be in the range 0.001-0.1µF.

Devices shall continue to operate correctly when exposed to any of the conditions in table 3.4.

Table 3.4 Receiver characteristics

Connection	Limit		Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	+12 / -7 VDC		Common Mode range
Pin 4 to Pin 1 or Pin 5 to Pin 1	+12 / -7 VDC		
	Non-Galvanically Isolated	Galvanically Isolated	
Pin 1 to Chassis	100 ohms -Note 1-	≥ 22M ohm @ 42 VDC	
Pin 2 to Chassis or Pin 3 to Chassis	+12 / -7 VDC	≥ 22M ohm @ 42 VDC	
Pin 4 to Chassis or Pin 5 to Chassis	+12 / -7 VDC	≥ 22M ohm @ 42 VDC	
Pin 2 to Pin 3	+/- 6V	+/- 6 V	
Pin 4 to Pin 5	+/- 6V	+/- 6 V	
Any Pin to Chassis	N/A	30 VAC / 42 VDC	

Note 1 : This cannot be characterized in terms of voltage. Manufacturers shall be permitted to fit a resistance of 100 ohms +/-20% between Chassis and Pin 1 for the purpose of limiting current in the screen due to small differential ground potentials. This method provides for reduction of Common Mode voltage at the line receiver.

3.5 Earth grounding of data link common for receivers

This Standard defines several allowable topologies for earth grounding of data link common and signal common for receiving devices. These are to be known as “non-isolated” and “isolated”. A specific concession is available to manufacturers of non-isolated receivers who, for reasons beyond the scope of this Standard, require a direct link between data link common and chassis.

3.5.1 Non-isolated receivers

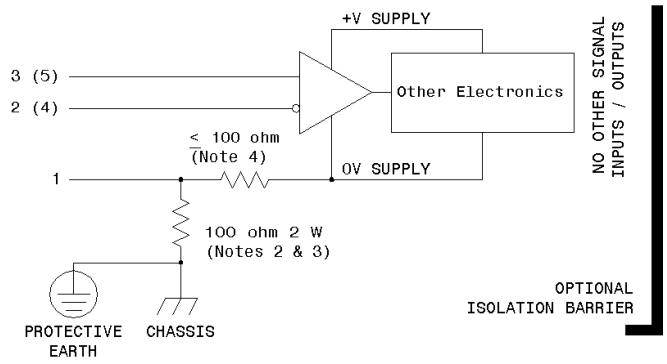

Figure 3.5.1.1 - Non-Isolated Receiver

Notes to Figure 3.5.1.1:

1) Since 0 V is not directly referenced to Chassis, local product safety standards may restrict choice of power supply (e.g., use of a Class 2 supply).

2) Manufacturers shall be permitted to fit a resistor as per Note 1, Table 3.4 Receiver Characteristics.

3) A concession to make a zero ohm connection in place of the 100 ohm resistor is available to manufacturers who mark the associated port as grounded, using the standard symbol representation ⚠ PIN 1 ⏚ ⚠ as defined in clause 12.3. When applying this concession, the data link common (Pin 1) to chassis connection shall satisfy the impedance tests as defined in clause 4.6 of this Standard. Unless this concession is applied, no other connection between circuit 0V supply and chassis is permitted.

4) Manufacturers shall be permitted to fit a resistor as per clause 2.5.

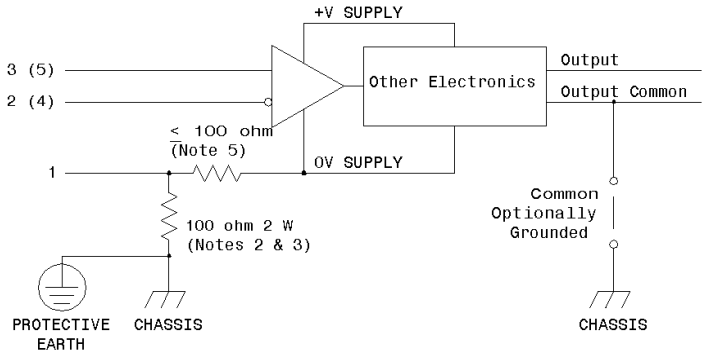

Figure 3.5.1.2 - Non-Isolated Receiver (other signal outputs)

Notes to Figure 3.5.1.2:

1) Since 0 V is not directly referenced to Chassis, local product safety standards may restrict choice of power supply (e.g., use of a Class 2 supply).

2) Manufacturers shall be permitted to fit a resistor as per Note 1, Table 3.4 Receiver Characteristics.

3) A concession to make a zero ohm connection in place of the 100 ohm resistor is available to manufacturers who mark the associated port as grounded, using the standard symbol representation ⚠ PIN 1 ⏚ ⚠ as defined in clause 12.3. When applying this concession, the data link common (Pin 1) to chassis connection shall satisfy the impedance tests as defined in clause 4.6 of this Standard. Unless this concession is applied, no other connection between circuit 0V supply and chassis is permitted.

4) Where other electrical outputs are present there shall be no low impedance path between the data link common/ signal common of the DMX512 receiver (Pin1) and such inputs or outputs including the signal I/O common. With the common mode 100ohm 2 watt resistor removed, the impedance between data link / signal common of the DMX512 port and any other signal I/O input or output shall be greater than 1000 ohms at 12 VDC. The removal of the resistor (or 0 ohm link as allowed in note 3) is only permitted for the purpose of making this test.

5) Manufacturers shall be permitted to fit a resistor as per clause 2.5.

6) Designs using this topology shall restrict the voltage levels on all such signal inputs and outputs to be within a 30 VAC / ±42 VDC limit.

3.5.2 Isolated receivers

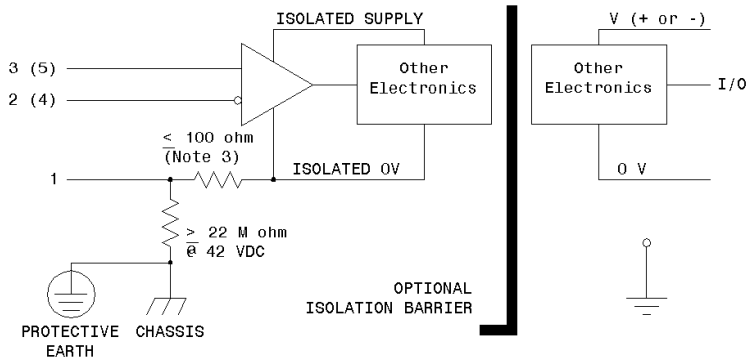

Figure 3.5.2 - Isolated Receiver

Notes Figure 3.5.2:

1) Any pin of the DMX512 input shall present an impedance ≥ 22 Mohm at 42 VDC with respect to Chassis, with respect to Protective Ground (where fitted), and with respect to any other signal inputs or outputs.

2) Adherence to this topology allows DMX512 receiver connection to be marked as ISOLATED. In such cases, the power supply for the receiver electronics will be floating

3) Manufacturers shall be permitted to fit a resistor as per clause 2.5.

4) Manufacturers may connect the “Other Electronics 0 V line to chassis or protective earth at their discretion.

3.5.3 Disallowed receiver topologies

This configuration is not permitted, although it may exist on some legacy products. While this topology is described as one possible topology in EIA-485, it is not appropriate when considering operation of DMX512 receiving devices in systems encountering differential ground potentials.

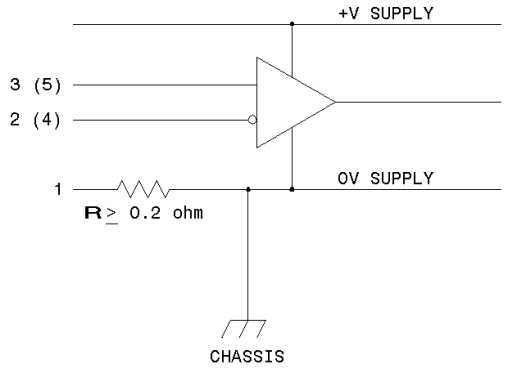

Figure 3.5.3 - Receiver Topology NOT Allowed

3.6 Earth grounding of data link common for other devices (signal processors)

3.6.1 Processing devices – floating

This Standard defines two allowed topologies for the earth grounding of data link common applicable to DMX512 Processing devices. These shall be known as “Floating” and “Ground Referenced”. It is also permissible to design processing devices based on the Isolated Receiver / Ground Referenced Transmitter or Isolated Receiver / Isolated Transmitter models already described.

As an aid to clarity and in order to minimize confusion with other schemes known to exist in legacy products, several topologies are specifically excluded. Manufacturers choosing to continue with the use of such topologies will be unable to claim compliance with this revision of the Standard.

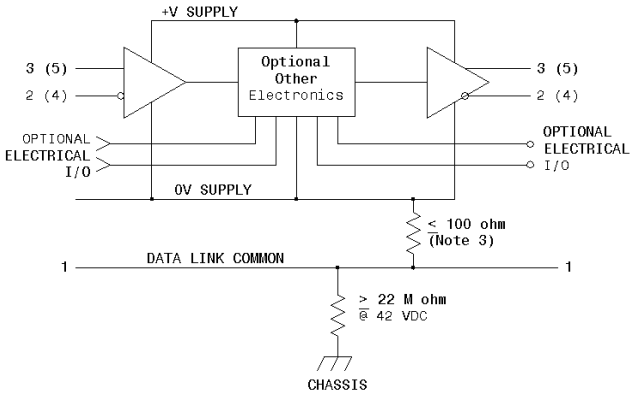

Figure 3.6.1- DMX512 Processing Device, Floating (Allowed)

Notes Figure 3.6.1:

1) Any input or output pin shall present an impedance $\geq$ 22 Mohm at 42 VDC with respect to Chassis, and with respect to Protective Ground (where fitted).

2) In operation, the grounding of a device using this topology is determined by the other DMX512 devices that it is connected to.

3) Manufacturers shall be permitted to fit a resistor as per clause 2.5.

3.6.2 Processing devices – ground referenced

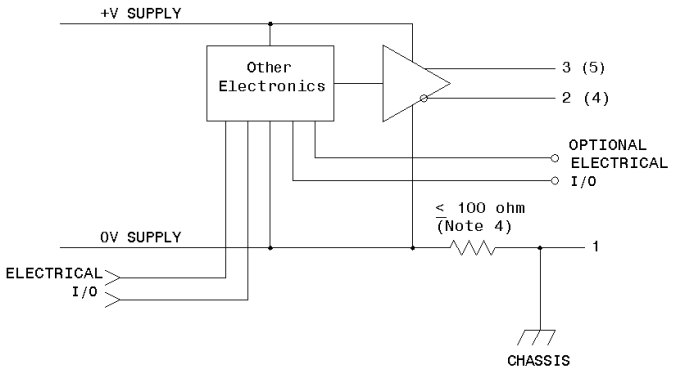

Figure 3.6.2 - DMX512 Processing Device, Grounded (Allowed)

Notes Figure 3.6.2:

1) A DMX512 processing device accepting electrical non-DMX512 inputs and providing one or more DMX512 outputs may ground the DMX512 output commons if it meets all the requirements shown for figure 3.3.1.

2) Output connections shall be marked in accordance with that detailed for Ground Referenced DMX512.

3) Pin 1 to Chassis connection shall satisfy tests as defined in clause 6.

4) Manufacturers shall be permitted to fit a resistor as per clause 2.5.

3.6.3 Processing devices – grounded

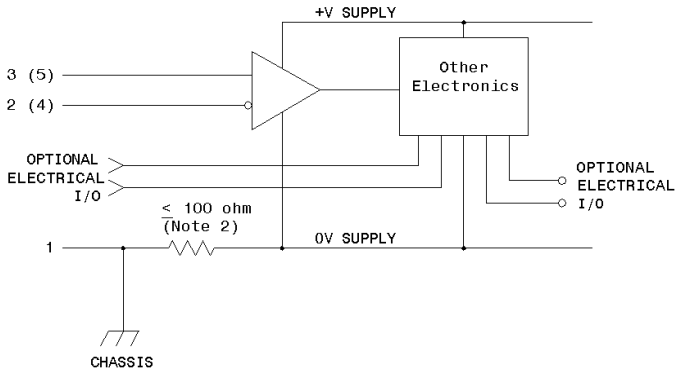

Figure 3.6.3 - DMX512 Processing Device, Grounded (Only Allowed when Marked ⚠ PIN 1 ⏚ ⚠)

Notes Figure 3.6.3:

1) A DMX512 processing device accepting a DMX512 input and providing one or more non-DMX512 outputs may ground the DMX512 input common if it meets all the requirements shown for a non-isolated receiver (other signal outputs) as detailed in figure 3.5.1.2, including the marking requirements of note 3.

2) Manufacturers shall be permitted to fit a resistor as per clause 2.5.

3.6.4 Disallowed processing device topologies

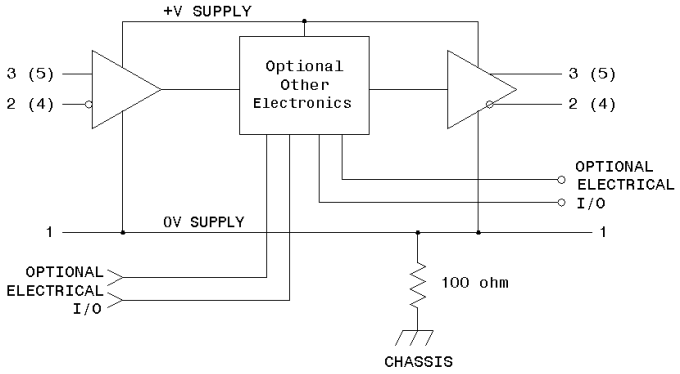

Figure 3.6.4.1 - DMX512 Processing Device, Non-Floating
(Not Allowed)

Notes Figure 3.6.4.1:

1) This configuration is not permitted (although it may exist on some legacy products). This topology is contradictory to the requirements of Figure 3.3.1, Note 4.

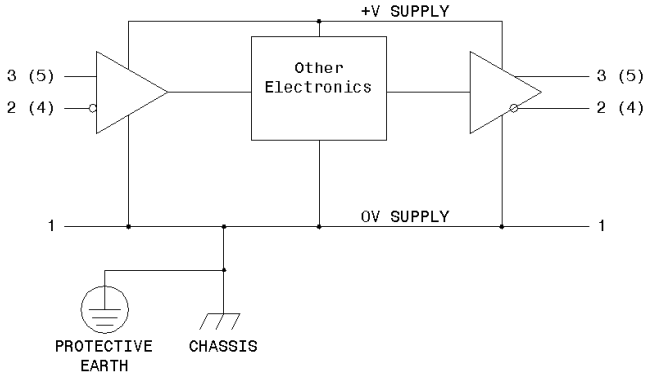

Figure 3.6.4.2 - DMX512 Processing Device, Grounded
(Not Allowed)

Notes Figure 3.6.4.2:

1) Grounding of the common is not allowed in a DMX512 processing device accepting one or more DMX512 inputs while simultaneously providing one or more DMX512 outputs.

3.7 Loading designation

The maximum number of devices permitted on a DMX512 data link is 32. Transmitters designed for this Standard shall be capable of driving 32 devices on a DMX512 data link. All DMX512 devices shall have a unit load of 1or less.

A receiver biased to any voltage from -5 to +10 volts shall not present a capacitive load to the line of more than 200pf. If this value is frequency dependent, the value given shall be the capacitive load when driven by a 650kHz sine wave.

4 Protection

4.1 General

To comply with this Standard, transmitting and receiving devices shall be protected against accidental connection of the data link to voltages beyond the range normally encountered for EIA-485 systems, in accordance with clauses 4.4 (DMX512 Transmitter Protection) and 4.7 (DMX512 Receiver Protection).

4.2 Minimum Electro Static Discharge (ESD) protection

Manufacturers shall ensure that any pins can withstand a minimum of 8KV ESD in accordance with the corresponding human body model as defined in EN61000-3-2 or other local regulations which may require higher levels of protection.

4.3 Minimum protection against interconnection damage

Clause 4.2 of the EIA-485 specification recognizes that certain other extraneous conditions may overstress the system and that these conditions should be specified in the referencing standard. Extensive use of temporary and portable equipment in Entertainment Lighting industry results in frequent connection and disconnection of equipment and gives rise to the possibility of equipment misconnection. Protection levels in excess of those defined in EIA-485 is required as detailed below.

To comply with this Standard, equipment shall be protected against damage resulting from accidental connection to voltages in excess of the minimum defined in EIA-485 clauses 4.2.5 and 4.2.6. Separate specification is provided for transmitting devices (Ground Referenced, Isolated, Floating) and receiving devices (Non-isolated, Isolated and Floating). This does not negate the need to comply with EIA-485 clause 4.2.6 - Transient overvoltage tolerance.

4.4 DMX512 Transmitter protection

Driver current limiting shall be in conformance with the requirements of EIA-485 clause 4.2.5. With the transmitting device output terminals shorted together, the transmitting device shall not be damaged.

In battery operated equipment, chassis shall be deemed to be any exposed connector parts which are metal and not carrying signals.

Transmitters shall not be damaged by voltages less than or equal to those listed in table 4.4 for both the power-on and power-off conditions.

Table 4.4 Transmitter protection

Connection	Minimum Protection Limit			Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	30 VAC / ± 42 VDC			
Pin 4 to Pin 1 or Pin 5 to Pin 1	30 VAC / ± 42 VDC			
Pin 2 to Pin 3	30 VAC / ± 42 VDC			
Pin 4 to Pin 5	30 VAC / ± 42 VDC			Not applicable to TYPE 5 ports
	Ground Referenced	Galvanically Isolated	Floating -Note 1-	
Pin 1 to Chassis	Must Pass Earth Continuity Test	N/A	N/A	See clause 4.5
Any other Pin to Chassis	30 VAC / ± 42 VDC	N/A	N/A	
Any Pin to Chassis	N/A	30 VAC / ± 42 VDC	30 VAC / ± 42 VDC	

Note 1 : Floating heading to indicate that this is only encountered on DMX512 Processing equipment.

4.5 Earth continuity for ground referenced transmitters

The resistance of the connection between the protective earth terminal or chassis and Pin 1 shall not exceed 0.2 ohms. Compliance with this shall be as per the test described in clause 4.6.

4.6 Data link common earth continuity test

The test shall be carried out for 1 minute with a test current of not less than 10 amps A.C. or D.C. The voltage drop between the protective earth terminal or chassis and Pin 1 shall be measured and the resistance calculated from the current and this voltage drop. This test shall not be required as a routine manufacturing test.

4.7 Receiver protection

A capacitor shall be fitted between Pin 1 and chassis for the purpose of Radio Frequency bypass. The value of this is not mandated by the Standard, but is expected to be in the range 0.001-0.1µF

Receivers shall not be damaged by voltages less than or equal to those listed in table 4.7.

Table 4.7 Receiver protection

Connection	Minimum Protection Limit			Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	30 VAC / ± 42 VDC			
Pin 4 to Pin 1 or Pin 5 to Pin 1	30 VAC / ± 42 VDC			
Pin 2 to Pin 3	30 VAC / ± 42 VDC			
Pin 4 to Pin 5	30 VAC / ± 42 VDC			Not applicable to TYPE 5 ports
	Non-Galvanically Isolated	Galvanically Isolated	Floating -Note 2-	
Pin 1 to Chassis	-note 1-	N/A	N/A	
Any other Pin to Chassis	30 VAC / ± 42 VDC	N/A	N/A	
Any Pin to Chassis	N/A	30 VAC / ± 42 VDC 100Mohm at 50 VDC	30 VAC / ± 42 VDC > 22Mohm at 50 VDC	

Note 1: This cannot be characterized in terms of voltage. Clause 3.4 (Receiver Characteristics) allows manufacturers to fit a resistance between chassis and Pin 1 for the purpose of limiting the current in the screen (shield) due to small ground differentials. Any such resistance shall survive continuous connection to voltages within the EIA-485 Common Mode range of -7/+12 VDC. Manufacturers shall ensure that any failure of this component due to exposure to voltages not exceeding 30 VAC / 42 VDC will not cause a safety hazard.

Note 2: Floating heading to indicate that this is only encountered on DMX512 Processing equipment.

4.8 Connection integrity

The link between input port data link common and loop-through port data link common (Pin 1) shall not be damaged by currents in the range 0 - 1 ampere over the voltage range 0-+12 VDC.

4.8.1 TYPE 1 ports - additional requirements

The link between input port Pin 4 and output port Pin 4 of a TYPE 1 device shall not be damaged by currents in the range 0 - 1 ampere over the voltage range 0-+12 VDC.

The link between input port Pin 5 and output port Pin 5 of a TYPE 1 device shall not be damaged by currents in the range 0 - 1 ampere over the voltage range 0-+12 VDC.

4.8.2 TYPE 5 ports - additional requirements

Where a TYPE 5 port makes limited current power available the power source shall not be damaged by continuous short circuit to any other pin.

Where a TYPE 5 product makes the limited current supply available on both an input or output port and corresponding loop or through port, the manufacturer shall ensure that the total current that can flow from any port is limited to 600mA even when the product is connected to other TYPE 5 devices.

4.9 Connection integrity - products with accessory power

For products using Accessory Power (and the prescribed 4 pin XLR connector as per clause10.4) the link between input port data link/power common and loop-through port data link/power common (Pin 1) shall not be damaged by currents in the range 0 - 5 amperes over the voltage range 0 - +25 VDC.

For products using Accessory Power (and the prescribed 4 pin XLR connector as per clause 10.4) the link between input port +24 VDC and loop-through port +24 VDC (Pin 4) shall not be damaged by currents in the range 0 - 5 amperes over the voltage range 0 - +25 VDC.

FPN : There are fundamental differences between TYPE 5 products and products using Accessory power. Unlike limited current (TYPE 5) devices, there is no requirement to limit the through current on Pin 4. For products supplying Accessory Power, and claiming compliance with this Standard, the current available at +24 VDC shall be current limited to not more than 5 Amps. The risk of accidental interconnection of devices using Accessory power with other DMX512 products is removed by the use of the 4 pin XLR connector as detailed in clause 10.4.

5 Data Protocol

5.1 Format

Data transmitted shall be in asynchronous serial format. DMX512 slots shall be transmitted sequentially, beginning with slot 1 and ending with the last implemented slot, up to a maximum of 512. Prior to the first slot being transmitted, a Reset Sequence shall be transmitted – a Break signal, followed by a MARK AFTER BREAK, and a properly framed START Code. Valid DMX512 slot values shall be 0 to 255 decimal.

5.2 Frame format

The data transmission format for each data value transmitted shall be as follows:

BIT POSITION	DESCRIPTION
1	Start Bit, Low or SPACE
2 through 9	Slot Value Data Bits, Least Significant Bit to Most Significant Bit Positive logic
10, 11	Stop Bits, High or MARK
Parity	Not transmitted

5.3 Packet format

The format of a DMX512 packet shall be a Reset Sequence followed by up to 512 slots of data. A packet is separated from the next packet by a Mark Before Break.

5.4 Break signal

The Break signal (Timing Diagram, Designation #1) may be of any length and shall last 88 microseconds (two frame times) duration or longer. A BREAK shall be defined as a high-to-low transition followed by a low of at least 88 microseconds. All receiving devices shall interpret any such BREAK as a terminator for any pending transmission/data packet and its end as the start of the MARK AFTER BREAK and START Code sequence at the beginning of the next packet.

5.5 Mark After Break

The duration of the MARK separating the BREAK and the START Code (Timing Diagram, Designation #2) shall be not less than 8 microseconds and not greater than 1 Second. All DMX512/1990 or later transmitters shall produce a MARK AFTER BREAK of not less than 8 microseconds. All receivers shall recognize an 8 microsecond MARK AFTER BREAK. Receivers capable of also recognizing the shorter 4 microsecond MARK AFTER BREAK (as specified in the 1986 version of this Standard) may be identified and marked as having this capability as per clause 12.1.

5.7 START Code

The START Code is the first properly framed byte following a BREAK. The START Code identifies the function of subsequent data in that packet.

5.7.1 NULL START Code

The NULL START Code shall be defined as a properly framed NULL byte (all zeros) following a BREAK. The NULL START identifies subsequent data as sequential 8-bit information.

5.7.2 Other START Codes

All other START Codes (1 through 255 decimal, 01 through FF hexadecimal) are referred to as Alternate START Codes. See clause 6 and Annex A.

5.8 Maximum number of slots

Each data link shall support up to 512 slots. Multiple links shall be used where larger numbers of slots are required.

5.9 Minimum number of slots

There shall be no minimum number of slots on the data link. DMX512 data packets with fewer than 512 slots may be transmitted, provided that the conditions of this Standard, including all of clause 5, are observed.

5.10 Defined line state between frames

The time between any two frames of a data packet (Timing Diagram, Designation #9) may vary between 0 microseconds and 1 Second. The line must remain in a "marking" state during any such idle period. A receiver must be capable of accepting a data packet having no idle time (0 microseconds) between any of its frames.

5.11 Defined line state between data packets (Mark Before Break)

Every data packet transmitted on the data link, regardless of START Code or length, must begin with a BREAK, MARK AFTER BREAK, and START Code sequence as defined above. The time between the second stop bit of the last data byte/frame of one data packet and the falling edge of the beginning of the BREAK for the next data packet (Timing Diagram, Designation #10) may vary between 0 microseconds and 1 Second. The line shall remain in an idle ("marking") state throughout any such period greater than 0 microseconds. Transmitters, therefore, shall not produce multiple BREAKs between data packets. Receivers, however, shall be capable of recovering from multiple BREAKs produced by data link line errors.

5.12 Minimum Break spacing

The period between the falling edge at the start of any one BREAK shall be not less than 1196 microseconds from the falling edge at the start of the next BREAK.

5.13 Dimmer class data

Valid dimmer levels shall be 0 to 255 decimal (00 to FF hexadecimal) representing dimmer control input. 0 shall represent a dimmer output of OFF or minimum and 255 shall represent an output of FULL. A dimmer shall respond to increasing the DMX512 slot level for 0 to 255 by fading from its minimum level (off) to its maximum level (full). The exact relationship between DMX512 slot levels and dimmer output is beyond the scope of this Standard.

5.14 Timing Diagram

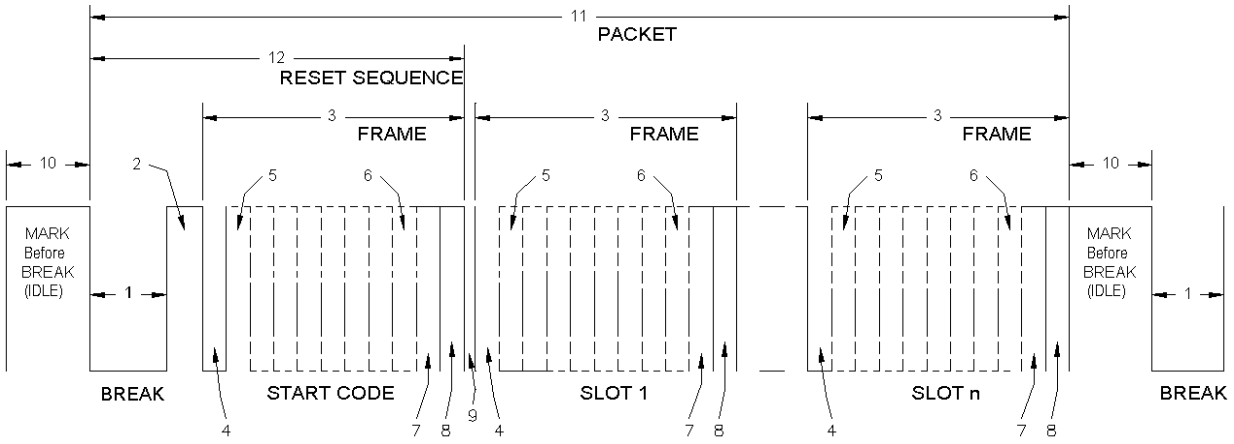

Figure 5.14 - Timing Diagram

Designation	Description	Min	Typical	Max	Unit
-	Baud Rate	245	250	255	kbaud / sec
-	Bit Time	3.92	4	4.08	µsec
-	Minimum Update Time for 512 slots	–	22.67	–	mS
-	Maximum Update Rate for 512 slots	–	44.11	–	/ Sec
1	"SPACE" for BREAK	88	–	–	µsec
2	"MARK" After BREAK (MAB)	8	–	1	µsec sec
3	FRAME Time	43.12	44	44.88	µsec
4	START Bit	3.92	4	4.08	µsec
5	LEAST SIGNIFICANT DATA Bit	3.92	4	4.08	µsec
6	MOST SIGNIFICANT DATA Bit	3.92	4	4.08	µsec
7	STOP Bit 1	3.92	4	4.08	µsec
8	STOP Bit 2	3.92	4	4.08	µsec
9	"MARK" Time between FRAMES	0	–	1	sec
10	"MARK" Before BREAK (MBB)	0	–	1	sec
11	BREAK to BREAK Time	1196	–	– 1.025	µsec sec
12	RESET Sequence (BREAK, MAB, START Code)	139.12	–	–	µsec

6 Alternate START Codes

6.1 Other Optional START Codes

In order to provide for future expansion and flexibility, this Standard makes provision for 255 additional START Codes (1 through 255 decimal, 01 through FF hexadecimal), henceforth referred to as Alternate START Codes. For this reason, a dedicated NULL START Code receiver must not accept as 8-bit level data any data packet with a START Code other than NULL START following the BREAK. See Annex A for Alternate START Code and Manufacturer/Organization ID Registration Policies and designations of Reserved Alternate START Codes.

Alternate START Code CF hexadecimal (207 decimal) is reserved for a System Information Packet (see clause 7 for description), Alternate START Code 55 hexadecimal (85 decimal) is reserved for a special Test Packet (see clause 6.6 for description), and Alternate START Code 17 hexadecimal (23 decimal) is reserved for a special text packet (see clause 6.7 for description).

6.2 Alternate START Code format

6.2.1 ASC timing parameters

Regardless of the function resulting from the Alternate START Code, DMX512 parameters not specifically modified when an Alternate START Code is implemented, shall be adhered to, including the following: MINIMUM BREAK DURATION (clause 5.12), TIMINGS as defined in the TIMING DIAGRAM (clause 5.14), and LOSS OF DATA TOLERANCE (clause 8), and a maximum of one START Code and 512 slots (513 frames) per packet.

6.2.2 ASC refresh interval

A DMX512 transmitter interleaving NULL START Code packets with Alternate START Code packets shall send a NULL START Code packet at least once per second.

6.2.3 ASC packet spacing

For any packet containing an Alternate START Code, the packet to packet timing requirements of this Standard shall be modified as follows:

6.2.3.1 ASC originating transmitters

For DMX512 originating transmitters such as consoles, show controller, and protocol bridges, the time from the beginning of the Alternate START Code to the beginning of the START Code of the next packet shall be not less than 110% of the time required to send the Alternate START Code packet with the minimum allowed Break, Mark After Break, and frame timings.

6.2.3.2 ASC in-line transmitters

DMX512 processing devices or any device that receives and re-transmits DMX512 shall as nearly as possible maintain START Code to START Code timing as defined above to not less than 110% of the time required to send that packet with the minimum allowed Break, MAB and frame timings. They may modify this time to accommodate baud rate tolerances while assuring that no Alternate START Code packets that they are designed to relay are lost.

In all cases the minimum Break to Break spacing set in clause 5.12 of this Standard shall also be adhered to.

6.5 Handling of Alternate START Code packets by in-line devices

DMX512 processing devices or any device that receives and re-transmits DMX512 wishing to claim conformance to this Standard shall state in the manual for the product how they process Alternate START Code packets. The acceptable processing methods are:

1) Block all packets containing particular Alternate START Codes. The START Codes blocked must be listed.

2) Pass unmodified all packets containing particular Alternate START Codes. The START Codes passed must be listed.

3) Process the information contained in packets containing particular Alternate START Codes. Optionally creating new packets containing Alternate START Codes. The processing algorithm must be appropriate for use intended for this START Code. The algorithm must be stated in enough detail to allow the user to decide if the device will satisfy their needs.

DMX512 in line repeating transmitters wishing to claim conformance to this Standard shall not pass some packets with a particular Alternate START Code while blocking other packets containing the same Alternate START Code unless doing so as part of a stated processing algorithm.

6.6 ASC test packet

Alternate START Code 55h (85 decimal) shall designate a special test packet of 512 slots, where all slots carry the value 55h (85 decimal). Test packets shall be sent so that the time from the start of the Break until the stop bit of the 512th slot shall be no more than 25 milliseconds. When test packets are sent back to back, the Mark Before Break time shall be no more than 88 microseconds. The Break timing for test packets shall be greater than or equal to 88 microseconds, and less than or equal to 120 microseconds. The Mark After Break time shall be greater than or equal to 8 microseconds and less than or equal to 16 microseconds.

6.7 ASC text packet

Alternate START Code 17h (23 decimal) shall designate a special packet of between 3 and 512 slots. The purpose of the ASC text packet is to allow equipment to send diagnostic information formatted for display.

Slot allocation is as follows:

Slot 1: Address of text viewer. A value of zero allows any DMX512 capable viewer to display the text. Values in the range 1-255 allow for addressing of text messages.

Slot 2: Characters per Line. Indicates the number of characters per line that the transmitting device has used for the purposes of formatting the text. A value of zero indicates ignore this field.

Slot 3-512: Consecutive display characters in ASCII format. All characters are allowed and where a DMX512 text viewer is capable, it shall display the data using the IBM standard character set.

When the ASC text packet is transmitted as part of the normal operation of a product, it shall be transmitted no more frequently than one packet per 256 packets of NULL START Code. When the ASC text packet is transmitted in a special diagnostic mode of the product, it may be transmitted continuously.

7 System Information Packet (SIP) Alternate START Code

7.1 System Information Packet (SIP)

Alternate START Code CF hexadecimal is reserved for a System Information Packet (SIP). The SIP provides (but is not restricted to) a means of sending checksum data relating to the previous packet on the data link.

7.2 SIP format

The format of the SIP is as Follows:
SIP Format - START Code = CFh (207 decimal)

Slot 1 Control Bit Field refer Clause 7.3
Slot 2 MSB of Optional 16 bit additive Checksum of previous packet
Slot 3 8 bit additive or the LSB of the Optional 16 bit Checksum of previous packet
Slot 4 SIP sequence number
Slot 5 DMX512 universe number refer Clause 7.6
Slot 6 DMX512 processing level refer Clause 7.7
Slot 7 Version of Software sending this SIP refer Clause 7.8
Slot 8 Standard Packet Len MSB
Slot 9 Standard Packet Len LSB refer Clause 7.9
Slot 10 Number of Packets transmitted by originating device since last SIP MSB
Slot 11 Number of Packets transmitted by originating device since last SIP LSB
Slot 12 Originating Device's Manufacturer ID MSB
Slot 13 Originating Device's Manufacturer ID LSB refer Clause 7.11
Slot 14 Last Device's Manufacturer ID MSB
Slot 15 Last Device's Manufacturer ID LSB
Slot 16 1st Predecessor to Last Device's Manufacturer ID MSB
Slot 17 1st Predecessor to Last Device's Manufacturer ID LSB
Slot 18 2nd Predecessor's Device Manufacturer ID MSB
Slot 19 2nd Predecessor's Device Manufacturer ID LSB
Slot 20 3rd Predecessor's Device Manufacturer ID MSB
Slot 21 3rd Predecessor's Device Manufacturer ID LSB
Slot 22 *reserved for future use*
Slot 23 *reserved for future use*
Slot 24 Checksum of the SIP

Equipment that implements SIPs shall be required to transmit them at least once every 15 seconds.

7.3 Control bit field

d7	d6	d5	d4	d3	d2	d1	d0
1 = LSB checksum exists	1=MSB checksum exists	reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	control bit set=1

Processing of the Control Bit is optional. If implemented, when the Control Bit is set (=1), the subsequent NULL START Code packet shall be held pending the reception of the next SIP for validation of the checksum. If a second NULL START Code packet is received without a preceding SIP, the receiver shall return to an immediate use mode and flag this as an error condition.

7.4 Checksums

8 bit additive checksum (or optional 16 bit additive checksum) of all frames in the previous packet. The checksum includes the START Code frame. Bits must be set in the control bit field to indicate which type of checksum is being sent.

7.5 SIP Sequence number

A free running 8 bit counter identifying the SIP and incremented by a SIP generator by 01h on every subsequent SIP. This field may be checked to ensure that SIPS are not being dropped randomly.

7.6 Originating universe

This slot indicate the (originating) DMX512 universe currently transmitted on this link. 00h is not used. Valid values 01h - FFh (1 decimal - 255 decimal).

7.7 DMX512 processing level

This slot indicates the level of post console processing. Originating devices shall always transmit a value of 00h in this field. Processing devices such as merge units or any that regenerate or provide a media conversion (e.g., Ethernet to DMX512) facility shall increment the value of this field by 01h. The content of this field indicates a level of process “hops” that data on the link has been subjected to relative to the originating transmitting device.

7.8 Software version

00h	not implemented
01h - FFh	firmware version of last device

FPN: This slot for use by the manufacturer and may not correlate with any formally published release identifier.

7.9 Packet lengths

This declares the standard length of packets for START Code 00, normally transmitted on this link.

Valid values are	0000h	packet length not declared
	0001h - 0200h	designates value of fixed packet length
	0201h - 7FFFh	are not used
	8000h	Dynamic Packet, length not declared
	8001h - 8200h	length of last dynamic packet
	8201h - FFFFh	are not used

7.10 Number of packets

A 16 bit count of the number of packets transmitted by the originating device since last SIP was transmitted. This count should not increment past FFFFh.

7.11 Manufacturer ID

Manufacturer ID will be the same 16 bit assignment as used for the Manufacturer's ID field used with Alternate START Code 91h (see Annex A - clause A4.2).

an ID == 0000h indicates that Manufacturer is not declared.
an ID == FFFFh indicates that Manufacturer has applied for, but not been granted, and ID and that this transmission originates from a product under development.

7.12 Packet history

Specialist DMX512 Processing devices and media converters shall be required to insert their own Manufacturers ID into the next available SIP slot. An originating device shall always send its Manufactures ID in SIP slots 12 and 13, with 0000h in slots 14, 15; 16, 17; 18, 19 and 20, 21. The next downstream processing device shall insert its own Manufacturers ID into slots 14, 15. The next+1 downstream processing device shall insert its own Manufacturers ID into slots 16, 17 and so on.

FPN: This scheme allows for a packet processing history to be traced back though a complex installation of products.

7.13 SIP Checksum

8 bit additive checksum of the SIP START Code (CFh) and first 23 slots of SIP data.

7.14 Application

Manufacturers of control consoles are encouraged to transmit SIPs, either as a background to normal processing or, in conjunction with the special test packet, as part of their suite of system test functions. One of the current problems with testing of DMX512 installations is that it must be done with static test packets – the flicker finder modes of testers cannot be used while a console is actually running the show, as by definition the DMX512 packets are varying as each cue runs. The interleaving of SIP's would allow some degree of live testing, particularly if one of more test packets were also sent applicable to the functionality of the receiving device.

FPN: For systems requiring a more secure link, manufacturers would have the option of following every normal packet with a SIP packet, although it is recognized that this would degrade data throughput. It could be used with systems that send packets of fewer than 512 DMX512 slots or refresh data at less than the maximum rate.

8 Receiver Performance

8.1 Loss of data tolerance / Resumption of acceptance of data

The receiving device must maintain, for a minimum of 1 Second, the last valid data value received for each slot.

A receiver not receiving a Reset Sequence within one second of the previous Reset Sequence shall be considered to have lost data input. Although this Standard does not specify loss of data handling procedures, it does require that manufacturers state what their Loss of Data handling procedures are.

8.2 Receiver performance at maximum update rate

The performance of any device incorporating a DMX512 receiver must not be degraded by the presence at its input of the continuous transmission of data packets containing any number of slot values up to the maximum update rates specified in clause 5.

8.3 Inactive receiver input circuitry

Unpowered connected DMX512 devices shall not degrade the performance of the DMX512 transmission system.

8.4 Packet processing latency

Some products may provide their specified functionality without processing or being able to process every consecutive DMX512 packet. Such products will have an inherent latency to data changes between packets, which shall be declared by the manufacturer in accordance with the disclosure requirements of clause 12.

9 DMX512 Systems Requiring DC Power

9.1 Accessory Power (24 VDC)

It is beyond the scope of this Standard to detail cable characteristics and system interconnection. This Standard defines only signal levels, protection levels, connector style and pinouts and marking requirements.

A special cable scheme is generally required for use with these products which provides for high current conductors on Pins 1 and 4 of the connector. In some situations it is advisable to daisy-chain products back to the power source, effectively supplying power from both ends of the cable. Refer to manufacturers for other details.

9.2 Limited current 12 VDC power for remote devices (TYPE 5 equipment)

9.2.1 Requirements for 12 VDC limited current power supplying devices

When a TYPE 5 DMX512 device provides limited current power, it shall provide this power on Pins 4 and 5 of either the male or the female connector. Both Pins 4 and 5 shall be connected by less than 2 ohms to the same positive voltage. This voltage is referenced to Pin 1.

If power is provided simultaneously on both male and female connectors, the manufacturer shall ensure that the total current that can flow from any port is limited to 600 mA, even when the product is connected to other TYPE 5 devices. One method of accomplishing this is diode isolating the connectors as shown in figure 9.2.1. Loop-through connections are subject to the restrictions in clause 4.8.2.

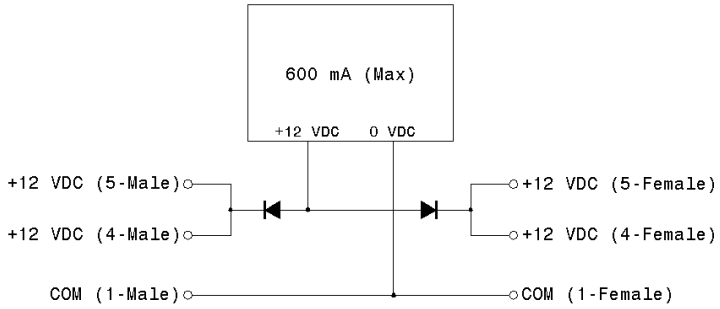

Figure 9.2.1 - TYPE 5 Dual Sex Power Diode Isolation

The voltage shall be least +11.5 VDC and shall never exceed +12.5 VDC. The available current shall be electronically limited to the range 300 mA - 600 mA, with the exception of battery powered devices which shall be limited to the range 50 mA - 600 mA..

Devices providing limited current power shall provide a means for disabling this power and for removing the connection between Pins 4 and 5. Devices shall provide a clear indication whether or not the power is enabled.

9.2.2 Requirements for devices designed to be powered by 12 VDC limited current

Devices designed to be powered by this supply shall function properly with input voltages in the range of +8 VDC to +12.5 VDC and shall not consume more than 300 mA. Devices designed to be powered by this supply shall not be damaged when powered by a voltage of +13 VDC.

10 Connection Methods

10.1 Equipment fitted with external user accessible pluggable data link connections

This category includes all portable products.

Female connectors shall be used on controllers and other transmitting devices and male connectors shall be used on dimmers and other receiving devices. Female connectors shall also be used where loop-through connections are provided.

Each DMX512 port shall be TYPEd in accordance with clauses 2.8 and 2.81.

10.1.1 Required Connector

Equipment in this category shall use 5 pin XLR connectors. The physical pinout of the 5 pin XLR shall be in accordance with the Pin reference in this Standard as defined in table 2.8.2.2.

Marking and identification of all ports shall be as required in clause 12.

10.1.2 Concession for use of an alternate connector (NCC DMX512)

A concession to use an alternate connector is available only when it is physically impossible to mount a 5 pin XLR connector on the product. In such cases the following additional requirements shall be met :

1) The alternate connector shall not be any type of XLR connector.
2) The alternate connector shall not be any type of RJ45 connector except as allowed in clause 11.5.
3) Where marking is applied to any such alternate connector, it shall be marked as NCC DMX512 (Not Connector Compatible), provided that all other requirements of this Standard are met.
4) The manufacturer shall provide an adapter cable with the appropriate connections to a standard 5 pin XLR connector for all DMX512 ports included in the alternate connector.
5) The TYPE and ground/isolation declarations shall continue to be declared for each port, and shall be unambiguously associated with each 5 pin XLR adapter connection.

10.2 Equipment intended for fixed installation with internal connections to the data link

Products in this category may optionally use the 5 pin XLR connector, but shall not use any other XLR connector. Where a non 5 pin XLR connector is used, this Standard makes no other restriction or stipulation on connector choice. Manufacturers are encouraged to make adequate provision for cable restraint, loop in and out of cables and provision of data link termination where necessary.

When use is made of the 5 pin XLR connector, female connectors shall be used on controllers and other transmitting devices and male connectors shall be used on dimmers and other receiving devices. Female connectors shall also be used where loop-through connections are provided.

In all other cases, the connector sex is not specified.

Products in this category shall be TYPEd and marked in accordance with the provisions of clause 12.5.2.

10.3 Passive Data Outlets or Wall plate panels

Products in this category designed for temporary and generally accessible access to DMX512 data links shall use 5 pin XLR connectors. Marking of such panels shall be in accordance with clause 12.5.3.

Panels which provide a data source on the primary data link shall use female connectors. Panels which are intended to provide primary data link input signals back to another location shall use male connectors.

10.4 Products providing or requiring 24 VDC Accessory Power

Products in this category shall use a 4 pin XLR, with pinout in accordance with table 10.4.

Table 10.4 - Accessory Power Signal designations summary

Function	Pin Reference within Standard	XLR Pin	DMX512/2000AP	Approved Abbreviation
Data Link Common / Supply Return	**1**	1	Common (Screen)	COM
Primary Data Link	**2**	2	Data 1-	D1-
	3	3	Data 1+	D1+
Accessory Supply		4	+24 VDC, Max 5 amps	24V

Female connectors shall be used on all sources of accessory power and male connectors shall be used on receiving devices requiring power. Female connectors shall also be used where loop-through connections are provided.

Manufacturers of accessory power sources shall be permitted to provide power output on a male connector, in order to allow the use of looped cable systems, provided that there is termination of the primary data link on Pins 2 and 3 of that male connector in accordance with clause 2.7 of this Standard.

Products in this category shall be marked in accordance with the provisions of clause 12.5.4.

10.5 Internal connections and specialized products for use with Category 5 cable schemes

Limited use of Category 5 cable schemes is permitted in accordance with clause 11.5 of this Standard. The use of RJ45 connectors (plugs/jacks) and punchdown terminal blocks shall be limited to connections which are part of a fixed installation and not normally accessible or intended for regular connection and disconnection.

RJ45 connectors (plugs/jacks) are permitted only on patch and data distribution products and only when installed in controlled access areas.

Any use of RJ45 connectors or punchdown terminal blocks shall use the wire color and cable pair reference in accordance with table 11.5.

Products in this category shall be TYPEd and marked in accordance with the provisions of clause 12.5.5.

10.6 Special provisions for TYPE 5 equipment

Systems using this auxiliary power shall be cabled so that the voltage drop in the return conductor (shield) of the control cable shall be limited to 2.5 VDC. Systems shall also be cabled so that the available supply voltage to the device shall be +8 VDC or higher.

11 Cable

11.1 Background

The high data transmission rate (250Kbaud) used by DMX512 requires the selection of a cable which does not significantly distort the signal or give rise to spurious signal reflections. Cables intended for use with audio systems (microphone cables), while having the convenience of flexibility, availability and relative low cost, are **NOT** suitable for use with DMX512 because of their high capacitance and incorrect characteristic impedance; at DMX512 data rates this will give rise to bit time distortion and signal reflections/overshoot, particularly over long (> 10m) distances.

11.2 General

Cabling systems shall provide a balanced, nominal 120 ohm terminated transmission system, and be made of cables with a characteristic impedance in the range 100-150 ohm.

> *FPN: Note that mixing cables of different impedances and other characteristics not isolated by buffers or other processing devices may affect system reliability.*

Installations using cables with one pair are referred to as Cable Scheme C1 in this Standard. The use of Cable Scheme C1 limits systems to the basic functionality offered by TYPE 0 ports. Other types of product may be interconnected but operation will be limited to transfer of data on the primary data link.

Installations using cables with two pairs are referred to as Cable Scheme C2 in this Standard. The use of Cable Scheme C2 is required for the interconnection of products with TYPE 1, TYPE 2, TYPE 3, TYPE 4 or TYPE 5 ports.

11.3 General Applications and between all Portable Equipment

Cable for general application shall be shielded twisted pair approved by its manufacturer for EIA-422/EIA-485 use at high data transmission rates and distances of at least 500 meters. Conductors in cable for portable equipment shall be of stranded construction.

11.4 Cable between permanently installed fixed equipment

Any cable satisfying the requirements of clauses 11.2 and 11.3 may be used for connections between items of fixed equipment, subject to local regulatory requirements regarding voltage and insulation styles.

The use of Category 5 cable shall be permitted and shall follow the specific installation and termination requirements of clauses 11.5.

11.5 Specific Requirements relating to the use of Category 5 cable

Installations using Category 5 cable implementing the one pair functionality of Cable Scheme C1 are referred to as Cable Scheme C5.1. This configuration limits systems to the basic functionality offered by TYPE 0 ports, but does permit two universes to be carried on one cable.

Installations using Category 5 cable implementing the two pair functionality of Cable Scheme C2 are referred to as Cable Scheme C5.2. The use of Cable Scheme C2 is required for the interconnection of products with TYPE 1, TYPE 2, TYPE 3, TYPE 4 or TYPE 5 ports., and is the preferred implementation.

Table 11.5 Connection Schedule for DMX512 systems using Category 5 Cable

Pair	Wire #	Color	Function	Cable Scheme C5.1	Cable Scheme C5.2
Pair 2	1	white / orange	data A +	DMX512 Pin 3	DMX512 Pin 3
	2	orange	data A -	DMX512 Pin 2	DMX512 Pin 2
Pair 3	3	white / green	data B+	DMX512 b Pin 3	DMX512 Pin 5
	6	green	data B -	DMX512 b Pin 2	DMX512 Pin 4
Pair 1	4	blue	v not exceeding - 0 / + 25 VDC		
	5	white / blue	0 v (signal common) | Wire 4 common	DMX512 Pin 1	DMX512 Pin 1
Pair 4	7	white / brown	v not exceeding - 0 / + 25 VDC		
	8	brown	0 v (signal common) | Wire 7 common	DMX512 b Pin 1	Wire 7 common
Shield		drain			

Note: Category 5 cable wire pair numbering and color in accordance with TIA T568B.

***Warning**: Accidental connection of legacy or TYPE 5 equipment to non-DMX512 equipment likely to be encountered (e.g., an Ethernet Hub at a patch bay) may result in damage to equipment.*

***Warning**: Wires 4 and 7 are reserved for general power use by manufacturers whose distributed DMX512 buffering products require low voltage DC power. As this voltage is never connected to an end user XLR connector, it should not be confused with TYPE 5 limited current power arrangements, nor is it Accessory Power as it is not accessible to the end user. Such systems are currently beyond the scope of this Standard.*

11.5.1 Shielded (Foiled) Twisted Pair Category 5 cable (STP/FTP)

Earth grounding of the Shield shall be in accordance with arrangements detailed in figures 11.5.4.1 and 11.5.4.2.

11.5.2 Unshielded Twisted Pair Category 5 cable (UTP)

UTP shall only be installed in earth grounded metal conduit.

11.5.3 Category 5 cable termination requirements

Product intended for use with Category 5 Cable such as receptacle plates or hard-wired signal processors, shall be suitable for termination of both UTP or STP/FTP Cable.

11.5.4 Category 5 grounding practices

Figures 11.5.4.1 and 11.5.4.2.1illustrate conversion from XLR Connector and EIA-485 cable to Category 5 cable with a Punchdown block and back, along with required grounding practices.

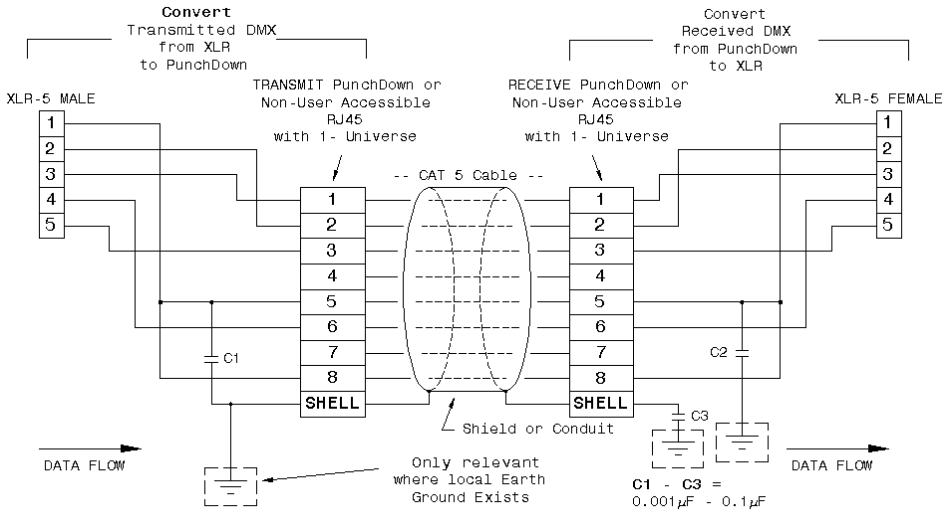

Figure 11.5.4.1 - Scheme C5.2 with (1) Universe in a TYPE 1 - 5 Implementation

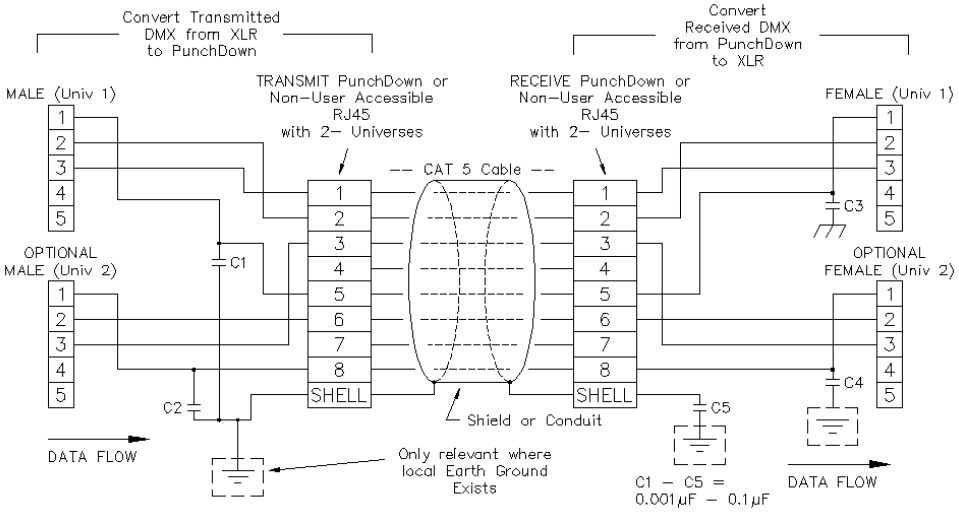

Figure 11.5.4.2 - Scheme C5.1 with (2) universes & (2) TYPE 0 Implementations

11.5.5 Category 5 grounding practices with UTP and STP/FTP cable

Figure 11.5.5 illustrates conversion from Shielded Category 5 cable to Unshielded and back and required grounding practices.

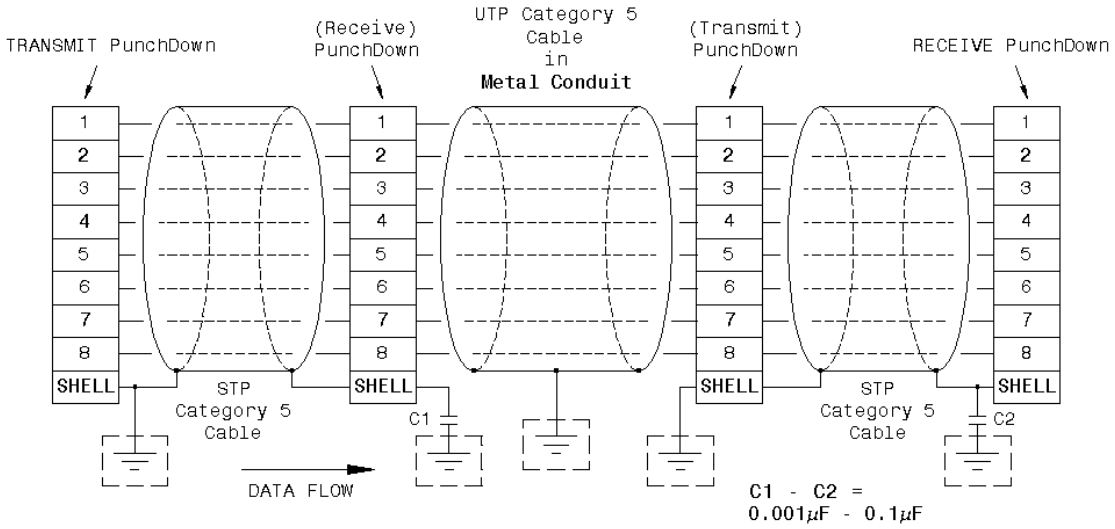

Figure 11.5.5 - Mixed UTP & STP / FTP Installation

Note: Use of buffers or other means to mitigate different impedances of the different cable types is not addressed in this figure.

11.6 Cable application rules

Table 11.6 summarizes the various constructions of cable suitable for use with DMX512 and how they can be implemented.

Table 11.6 - Cable application rules

Type / Use	Solid Conductors			Stranded Conductors		
	EIA-485	UTP Category 5	STP/FTP Category 5	EIA-485	UTP Category 5	STP/FTP Category 5
Portable	No	No	No	OK - Note 1 -	No	OK - Note 1 -
Permanent	OK	In Earthed Metal Conduit Only	OK - Note 2 -	OK - Note 2 -	In Earthed Metal Conduit Only	OK - Note 2 -

Note 1: It is recommended that braided shield be used for better durability

Note 2: Use of Plenum Rated cable without conduit allowed

12 Marking and Disclosures

12.1 Identification

Only equipment conforming to this Standard may be marked and identified with "USITT DMX512/2000" or "DMX512/2000".

Only receivers also capable of accepting a 4 microsecond MARK AFTER BREAK may be marked and identified as "USITT DMX512/2000 (4µSec)" or "DMX512/2000 (4µSec)".

FPN: The original version of this Standard (1986) allowed transmit packets with a 4 microsecond Mark After Break. This minimum was revised to 8 microseconds in the 1990 edition.

All marking shall comply with the style sheet requirements shown in Annex D – Port Marking Style Sheet. All information provided by marking shall also be provided in the equipment manual.

12.2 TYPE and Pin marking

Where required by clauses 12.3 through 12.5, all ports shall be marked as to the applicable TYPE as defined in table 2.8.2.1.

Where declaration of pinout detail is required by clauses 12.3 through 12.5, manufacturers shall use the signal designations from table 2.8.2.2 in any marking of pin, contact or terminal functions appearing on or within a product and associated with installation or connection. Such details are dependent on the declared TYPE of the port.

Where it is necessary to use abbreviations, only those detailed in table 12.2 shall be permitted.

Table 12.2 - Signal designations abbreviations allowed for marking

Function	Abbreviation
Common (Screen)	COM
Primary Data Link – Data 1-	D1-
Primary Data Link – Data 1+	D1+
Secondary Data Link – Data 2-	D2-
Secondary Data Link – Data 2+	D2+
Secondary Data Link – Talkback-	TB-
Secondary Data Link – Talkback+	TB+
12 VDC	12V
24 VDC Accessory Power	24V or AP

12.3 Ground / Isolation marking

All DMX512 ports shall also be marked as to the relationship between Pin 1 and earth ground. The allowed grounding topologies are shown in table 12.3.

Table 12.3 Ground / Isolation marking

Function of Port	Defining Figure	Comment	Approved Marking
Transmitter	fig 3.3.1	Ground Referenced	*no mark required*
Transmitter	fig 3.3.2	Isolated	ISOLATED
Transmitter as part of buffer or processing device	fig 3.6.1	Floating	FLOATING
Transmitter as part of DMX512 source with non-DMX512 inputs	fig 3.6.2	Ground Referenced	*no mark required*
Receiver	fig 3.5.1.1 or 3.5.1.2	Non-isolated, 100 ohm 2 Watt resistor	*no mark required*
Receiver	fig 3.5.1.1 or 3.5.1.2	Non-isolated with concession per note 3 of the figures	⚠ PIN 1 ⏚ ⚠
Receiver as part of a processing device	fig 3.6.3	Grounded	⚠ PIN 1 ⏚ ⚠
Receiver	fig 3.5.2	Isolated	ISOLATED
Receiver as part of a buffer or processing device	fig 3.6.1	Floating	FLOATING

12.4 Data line termination marking

The marking for DMX512 input ports that are permanently terminated shall include the word ‘TERM’. Marking for DMX512 input ports with switched termination shall not include the word ‘TERM’. The means controlling the termination shall be identified in an appropriate manner.

12.5 Required disclosures

12.5.1 Portable products and products fitted with external pluggable data link connectors

Ports on these products shall be TYPE marked in accordance with clause 12.2.

Ports on these products shall provide Ground/Isolation marking in accordance with clause 12.3.

Connector pinout detail on all TYPE 5 ports shall be provided in accordance with clause 12.2. The declaration of pinout detail for other TYPEs remains optional.

If use has been made on any non XLR connector in conjunction with the supply of an adapter cable, the non-XLR connector shall be also be marked as NCC DMX512/2000.

12.5.2 Equipment intended for fixed installation with internal connections to the data link

Ports on these products shall be TYPE marked in accordance with clause 12.2.

Ports on these products shall provide Ground/Isolation marking in accordance with clause 12.3.

Clearly identified connector pinout detail shall be marked on or within any product in accordance with clause 12.2.

12.5.3 Data outlet or wall plates fitted with 5 pin XLR connectors

Where a 5 pin XLR female or male connector is fitted to a wall plate or facility panel in a manner that links it directly back to a patch panel or data distribution buffer, its TYPE cannot be determined without reference to the product to which it is ultimately patched and the cable scheme implemented.

Manufacturers and Installers of such data outlets shall be permitted to mark the XLR connectors in accordance with table 12.5.3. If the site cable scheme or pinout does not follow this table, no reference to DMX512, including use of the term “DMX”, shall be permitted.

No reference to DMX512/2000 shall be permitted.

FPN: the “/2000" indicates electrical characteristics of active electronics compliant with this edition of the Standard, which are not known at the passive wall plate.

Table 12.5.3 - 5 pin XLR data outlet / wall plate marking

5 Pin XLR - Pins Wired	Cable Scheme	Permitted Marking at XLR	Comments
1, 2, 3	C1	DMX512 Scheme C1	
1, 2, 3	C2	DMX512 Scheme C1	Can be upgraded to full wiring of XLR and remarked for Scheme C2 at later date if required
1, 2, 3, 4, 5	C1	not permitted -Note 1-	
1, 2, 3, 4, 5	C2	DMX512 Scheme C2	necessary for use with TYPE 2 – TYPE 5 ports
a(1, 2, 3) b(1, 2, 3)	C5.1	DMX512 Scheme C1	One CAT 5 Cable w/ two universes
1, 2, 3	C5.2	DMX512 Scheme C1	Can be upgraded to full wiring of XLR and remarked for Scheme C2 at later date if required
1, 2, 3, 4, 5	C5.2	DMX512 Scheme C2	necessary for use with TYPE 1 – TYPE 5 ports

Note 1 : this is inconsistent with designated cable scheme.

12.5.4 Products providing or requiring 24 VDC Accessory Power

Accessory power equipment claiming compliance and using the designated 4 pin connector may be marked as DMX512/2000AP (AP for Accessory Power).

Pinout details shall appear on the product in accordance with either the DMX512/2000AP or approved abbreviation columns of table 10.4.

No reference to TYPE is permitted.

Ports on these products shall provide Ground / Isolation marking in accordance with clause 12.3

12.5.5 Internal connections and specialized products for use with Category 5 cable schemes

Ports on these products shall be TYPE marked in accordance with clause 12.2.
Ports on these products shall provide Ground/Isolation marking in accordance with clause 12.3.

Ports on these products may marked as NCC DMX512/2000.

12.5.6 Equipment with Type 5 ports - additional disclosures

12.5.6.1 Required disclosure for TYPE 5 devices

The current capacity for supplying devices and the current requirements for consuming devices shall be provided in the device manual. The manual must state that using remotely powered devices may disable other DMX512 features and may cause damage to non-compliant DMX512 legacy equipment.

The manual shall declare the method used to limit current on loop-through ports as required by clause 4.8.2.

The manual shall clearly describe how to disable the remote powering. It shall describe any changes needed to make the device coexist with other DMX512 devices that require the use of Pins 4 and 5 for data.

12.5.6.2 Cable information requirements for TYPE 5 equipment

Manufacturers of devices intended to be remotely powered shall provide clear instructions to allow a user to construct systems that meet all cable voltage drop requirements. An example of such instructions would be to specify the length of a particular gauge cable that may be used between the power supplying device and the power consuming device. If a particular kind of cable is specified, that cable type shall be readily available.

12.5.7 Loss of data handling procedure

This Standard does not define loss of data handling procedures (clause 8.1) beyond requiring that manufacturers declare their own products' procedure(s). Such declarations shall be made in the equipment manual.

12.5.8 Packet Processing latency

Manufacturers shall declare any inherent latency to data changes between packets in the equipment manual. This may be in terms of response time or other wording as chosen by the manufacturer, but shall clearly indicate if the product design might legitimately ignore some packets in normal operation.

12.5.9 NULL START Code functionality

Manufacturers of transmitting devices shall declare in the device manual the full range of slot values transmitted in conjunction with packets sent using the NULL START Code.

Manufacturers of receiving devices shall declare the response to packets received containing the NULL START Code, with particular reference to any functionality requiring limited or restricted slot data values, in the equipment manual.

12.5.10 Slot footprint

Manufacturers of receiving devices shall declare the slot footprint in the equipment manual.

12.5.11 Device interconnection

Manufacturers claiming compliance with this Standard shall include the table and text of Annex C in their product documentation. Manufacturers of TYPE 0 through TYPE 5 equipment shall shade or otherwise indicate the column and row that apply to their product. Manufacturers of cable and passive cabling systems are not covered by this requirement.

12.6 Compliance

Manufacturers claiming compliance with this Standard shall complete and hold on file a Protocol Implementation Compliance Statement (PICS) as defined in Annex E. Copies of the PICS shall be made available on request.

= END =

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ANNEX A (Normative) - Alternate START Codes Registration & Reserved Codes

A1 Alternate START Code Registration Policy: 1 - 255 decimal (01 - FF hexadecimal).

The first frame of a DMX512 packet is the START Code. The value of this frame identifies intended use of data in the rest of the packet. The Standard provides for a non NULL or "Alternate" START Code. Where it is required to send proprietary information over a DMX512 data link, a packet starting with a registered Alternate START Code shall be used.

A2 Alternate START Codes Reserved

A2.1 Authorized use

The E1 Accredited Standards Committee or any organization that it authorizes may use an Alternate START Code to provide further extensions to the DMX512 Standard.

A2.2 Future revisions

Alternate START Codes from 92 to CE hexadecimal shall be reserved for possible future revisions of this Standard. No equipment shall be manufactured that generates any of these codes until their use is defined by the Standard. 90h is reserved for future expansion. 91h followed by a 2 byte Manufacturer ID field is reserved for Manufacturer/Organization specific use.

A2.3 Test, Text, and System information packets

Alternate START Code 55 hexadecimal is reserved for a special Test Packet, Alternate START Code 17 hexadecimal is reserved for a Text Packet, and Alternate START Code CF hexadecimal is reserved for a System Information Packet. See clauses 6.6, 6.7, and 7 for descriptions.

A2.4 Alternate START Codes reserved for development

Alternate START Codes F0 - F7 shall be reserved for prototyping/experimental use while the manufacturer/organization is waiting for their registered Alternate START Code to be assigned. Any manufacturer/organization can use any of these during the development process without risking conflict with production equipment during field tests. Manufacturers shall not advertise or sell products or devices that use Alternate START Codes F0 - F7.

A3 Requests For Registration of New START Codes and Manufacturer IDs

Any manufacturer or organizations involved in the use of DMX512 may request that a START Code or Manufacturer ID be registered for their use. Requests shall be forwarded to the Secretariat for the E1 Accredited Standards Committee – ESTA. ESTA will attempt to honor such reasonable requests as described below.

A4 Number of Alternate START Codes per entity

No more than one Alternate START Code may be registered to any one manufacturer/organization. Manufacturers and Organizations with Alternate START Codes registered prior to the publication of this edition of this Standard may request one additional Alternate START Code this issue of the Standard.

A5 Selection of the Alternate START Code value and Manufacturer ID

The assignment of any particular numeric START Code or Manufacturer ID value to any particular entity is solely up to the E1 Accredited Standards Committee. Assignment depends on the availability of unused and unreserved START Codes and Manufacturer IDs.

A6 Documentation Register

A6.1 Documentation for use of Alternate START Codes

The manufacturer/organization requesting registration of an Alternate START Code shall provide a 2-line description of the purpose of the Alternate START Code. They shall list the minimum and maximum number of frames, including the START Code, in any proposed packet. Any provided description (subject to editing) shall be included in the Register. This is not required for functions associated with a manufacturer specific ID under Alternate START Code 91. It is recommended, but not required, for Alternate START Codes assigned prior to the adoption of this version of the Standard.

A6.2 Maintenance and Publication

The E1 Accredited Standards Committee through its secretariat (ESTA) shall maintain a Register of Alternate START Codes and Manufacturer IDs. ESTA will publish the Registry on a regular basis, not less than once per year, and will provide updates in its publications as they occur.

A7 Supplemental documentation

If the manufacturer/organization wishes detailed documentation to be in the Public Domain, a note will be added to the Registry, but they will be responsible for such publication.

A8 Ownership

The DMX512 Standard is copyrighted. By registering a START Code or Manufacturer ID, no ownership rights are conferred to any third party. Alternate START Codes are registered to particular entities solely to allow for orderly management of the Standard. The registrant does not own the Alternate START Code.

-end of Annex A-

Annex B (Normative) - Type 3 DMX512

Preface (not part of the Standard)
Until adoption of this Standard, all designs, constructions and other disclosures set forth herein are the property of ROSCO/Entertainment Technology and such information is imparted to you in confidence. In accepting this information you agree not to reproduce it, to disclose it, or to have it manufactured in whole or part without our written permission. This information is not in the public domain. ROSCO/Entertainment Technology retains full copyright protection. It is made available as a "royalty-free license" to parties who have signed an agreement of compliance. Upon adoption of this Standard, ROSCO/Entertainment Technology will either transfer the copyright to USITT and ANSI ASC E1 (ESTA) for administration or make other appropriate arrangements to ensure that this is not an obstacle to publication.

Annex B Foreword

This document describes the communications protocol originally implemented as an extension to USITT DMX512/1990 by ROSCO/Entertainment Technology's Intelligent Power System (IPS) dimmers to return data from the dimmers to the console, a separate status monitor, or other device. This protocol, originally known as the Intelligent Diagnostic Specification (IDS), is a strict superset of E1.11 (DMX512/2000).

Rights are granted only to the data return technique described herein. This agreement grants no rights of any kind to ROSCO/Entertainment Technology's patented IPS power control technology, which are covered in whole or in part by one or more of the following U.S. patents: 5,004,969 and 5,239,255. Other Patents Pending, foreign and domestic.

B1 Introduction

B1.1 General

The advantage of the talkback scheme described herein is its simplicity, adaptability to a variety of DMX512 devices, response speed, and automatic response to any standard DMX512 data stream. The adoption of this protocol as TYPE 3 DMX512 avoids incompatible use of the DMX512 spare pair and saves manufacturers and end users from the problems of integrating incompatible systems.

This document defines an extension to the DMX512 Standard to allow data to be returned from lighting equipment and accessories by making use of the two "optional" data lines on the standard cable, defined in the Standard as "second data link" and located on DMX512 port Pins 4 and 5. The TYPE 3 specification in no way prevents a manufacturer from incorporating a proprietary "query-and-response" protocol using alternate DMX512 START Codes into a product. The TYPE 3 DMX512 talkback specification simply allows for both a simple universal and a vendor-specific data return format to peacefully coexist on Pins 4 and 5 of a DMX512 port.

This annex is organized into three major sections - an overview of the return data extension to the DMX512 Standard, a summary of the original data return format as implemented by ROSCO/Entertainment Technology, and an example detailing the data returned by ROSCO/Entertainment Technology's IPS products.

B1.2 Compliance

Manufacturers implementing TYPE 3 DMX512 shall support as a minimum, identification of manufacturer device type and on-line/off-line status in their talkback monitoring system. It is hoped that vendors will support as much data as possible.

B1.3 Definitions

A system implementing this protocol extension consists of three types of devices connected to the DMX512 data link:

B1.3.1 Transmitter: generates the standard-conforming stream of DMX512 control packets. This function is generally performed by the console. There can be at most one active transmitter on a DMX512 data link.

B1.3.2 Responder: is a dimmer or other DMX512-compatible device which generates responses in reaction to packets from the transmitter. There can be many (up to 171) responders on a data link.

B1.3.3 Monitor: is a device which receives and interprets the data returned by the responders. This function may be performed by a stand-alone device (e.g., the IPS Status Monitor) or may be combined with the transmitter function in a console. A system can have zero, one, or many monitors.

B2 TYPE 3 Protocol

B2.1 Synchronizing the return data

To permit operation with existing DMX512 transmitters, the returned data must be synchronized with the outbound control data on at the DMX512 port Pins 2 and 3 (see Figure B2.1 below). Ideally, each responder would supply one byte of response data precisely synchronized to the level byte that was transmitted to it in the control stream. However, propagation delays in any real-world distributed DMX512 installation would prohibit precise synchronization and data "collisions" would result.

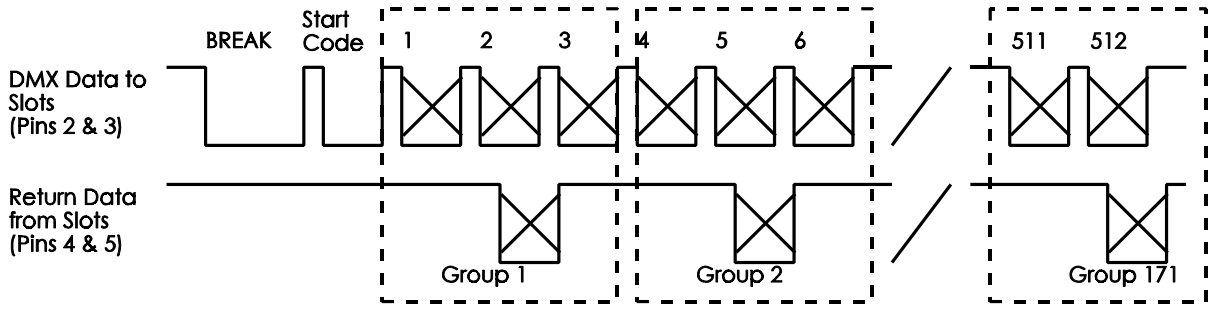

Figure B2.1 - Synchronization of Return Data to Control Stream

To guarantee that independent, distributed DMX512 devices can reliably return data without collisions, the return data protocol requires that only one byte of data be returned for every three slots in each DMX512 packet. The 512 possible DMX512 addresses are divided into 171 possible groups, with group 1 comprising

slots 1, 2, and 3; group 2 of slots 4, 5, and 6, and so on. In general, group *i* consists of slots 3*i*-2, 3*i*-1, and 3*i*. Note that, if the number of slots transmitted is not an exact multiple of 3, the last group will consist of one or two slots. (See Figure B2.1 above, for the example of group 171.)

The protocol, therefore, requires that one responder answer for each group of three slots that wish to return data. That responder is responsible for transmitting one byte of return data per DMX512 packet that addresses it. The responder shall transmit its data on receipt of the first slot in its associated group. The start bit of the response frame shall start no earlier than the rising edge of the DMX512 slot stop bit #1 and no later than 40 microseconds after that rising edge.

Each responder transmits a repeating sequence of bytes, the format of which is indicated by the RESPONSE START ID byte which flags the beginning of the sequence. In general, the RESPONSE START ID is followed by zero or more bytes of data common to all three slots in the group, followed by zero or more bytes of data per slot. Once all bytes in the sequence have been sent, a new sequence commences with a new RESPONSE START ID. It is obvious that the update rate of the talkback data is directly proportional to the update rate of the transmitted DMX512 data.

FPN: For example, at a 44Hz DMX512 update rate, returning 26 bytes of data for all 171 response groups takes 1.7 seconds

B2.2 Response frame format

Response frames are 11-bit characters, sent at a 250 Kbps data rate. Response frames comprise one start bit, eight data bits, one flag bit and one stop bit. The flag bit is set to one only on RESPONSE START ID bytes. This allows the monitor to find the beginning of a response sequence and resynchronize.

A maximum sequence of 32 bytes, including the RESPONSE START ID byte, are permitted per group.

(Ed. Note: ROSCO/Entertainment Technology is currently maintaining the list of RESPONSE START ID byte assignments).

B2.3 Monitor implementation issues

Due to the synchronization described above, a monitor must observe both the data from the transmitter and the data returned from the responders to be able to correctly interpret which group of slots should be associated with a response byte. The monitor must also maintain a separate state for each of the 171 possible groups, as each responder can operate asynchronously and be at a different point in its return data sequence from other responders on the same link.

The monitor should read the captured response data after the rising edge of the stop bit of the third data slot of each group. The capture shall happen no later than 40 microseconds from that rising edge. If no character is received during the transmission of the three slots comprising the group, the monitor should assume that the return data stream for that group has been interrupted, and ignore any subsequent characters until another RESPONSE START ID is received.

After startup, or after any serious error condition, the monitor should ignore all response data from each group until a RESPONSE START ID byte (i.e., a byte with a flag bit = 1) is seen. If the RESPONSE START ID byte is not one that the monitor recognizes, it should again ignore data until a valid one is seen for the group in question, as a responder may chose to interleave sequences with different formats.

B3 Hardware Implementation Issues

B3.1 Introduction

The hardware required to implement talkback is straightforward. The return data channel is EIA-485 and shall comply with all other provisions of this Standard, including clauses 2 through 4. Each responder drives the line in response in coming data according to the format described in Figure B2.1.

B3.2 Line Driver

Each responder shall have an EIA-485 line driver with a driver enable control. The driver enable control should be connected to the responder UART's RTS (Request-to-Send) pin through logic that will enable the driver when RTS is asserted by the UART. This will automatically gate the driver on and off at the proper time. If the UART does not have RTS control, responder software must control the line driver and gate it on and off the line at the proper time. In general, the line driver should be enabled one bit time prior to transmission, and disabled one bit time after the last bit has been sent.

B3.3 UART

The UART should support 9-bit mode since RESPONSE START ID bytes use this bit as a flag. Many microcontrollers and UARTs directly incorporate this mode. Others emulate it by allowing the 9th bit (which is the parity bit position) to be directly set or cleared.

B3.4 Line Termination

The return data line must be terminated at both ends with a 120 ohm termination. This termination must also be "fail-safed" at the return data receiver to hold the line in the MARK state when none of the responders is driving the line. The termination at the bidirectional distribution amp receiver is always active since this point is always the end of a particular DMX512 link. **It is critical that receiver inputs be properly terminated/failsafed at all times.**

The overall termination resistance value must result in a value equal to the characteristic impedance of the line. The EIA-485 specification calls for a 120 ohm termination resistor at each end of the line. Therefore, the termination value must be 120 ohms. A basic schematic of the circuit is shown in Figure B3.4.

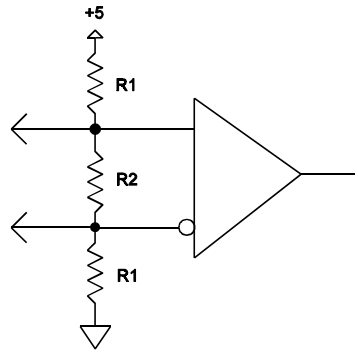

Figure B3.4 - External Line Termination

The effect of the pull-up and pull-down resistors, R1, are that they will appear to be summed together in parallel with the termination resistor R2.

Reducing R1 will increase the threshold voltage, increasing the noise immunity when the line is high impedance. It is desirable to have at least 250mV of threshold voltage when both ends of the line are terminated. The EIA-485 specification requires a 200 mV maximum threshold for a receiver, so 250mV provides a 20% margin. Since the link will be terminated at each end, the threshold set for each termination must be twice the desired threshold of the fully-terminated case.

A threshold of 500mV is selected, since it will decrease to 250mV when both ends of the cable are terminated. Because it is desirable to use standard resistors, R2 is increased to 133 ohms, the nearest standard 1% value. It is also desirable to make R1 part of a resistor package, which will ensure close tolerance and matching. The nearest standard value which will give the desired threshold voltage is 560 ohms. The actual noise margin is 0.530V, and the impedance is 118.9 ohms.

B3.5 Bi-directional distribution amplifiers

The return data standard requires bi-directional distribution/return data combiners. The DMX512 output data may be split and separately buffered as in standard DMX512 buffers. Return data receivers must be "wire-OR" connected within a unit. This combined received data signal is used to drive back to the return data monitor. Distribution amplifier talkback outputs are active at all times.

Optoisolation should be provided between the EIA-485 circuits. Power for each link may be provided by separate transformers and voltage regulators, or by isolated DC-to-DC convertors. The bidirectional distribution amplifier should not perform any processing on the data, since the talkback protocol depends upon the relationship with outbound DMX512 to synchronize the return data.

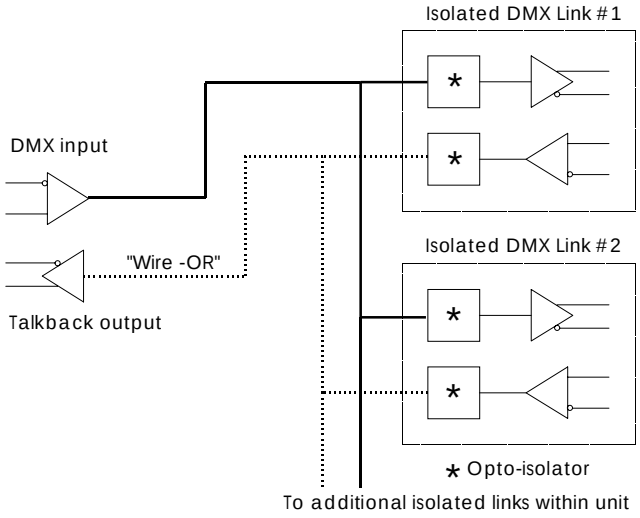

Figure B3.5.1 - Bi-directional TYPE 3 DMX512 Distribution Amplifier

Multiple units may be cascaded to provided a large number of separate DMX512 links. No DMX512 responders can be present on the DMX512 links between distribution amplifiers or between the status monitoring device, shown in Figure B3.5.2 as dashed lines. This is because the return data lines on this links are always driven by the distribution amplifiers.

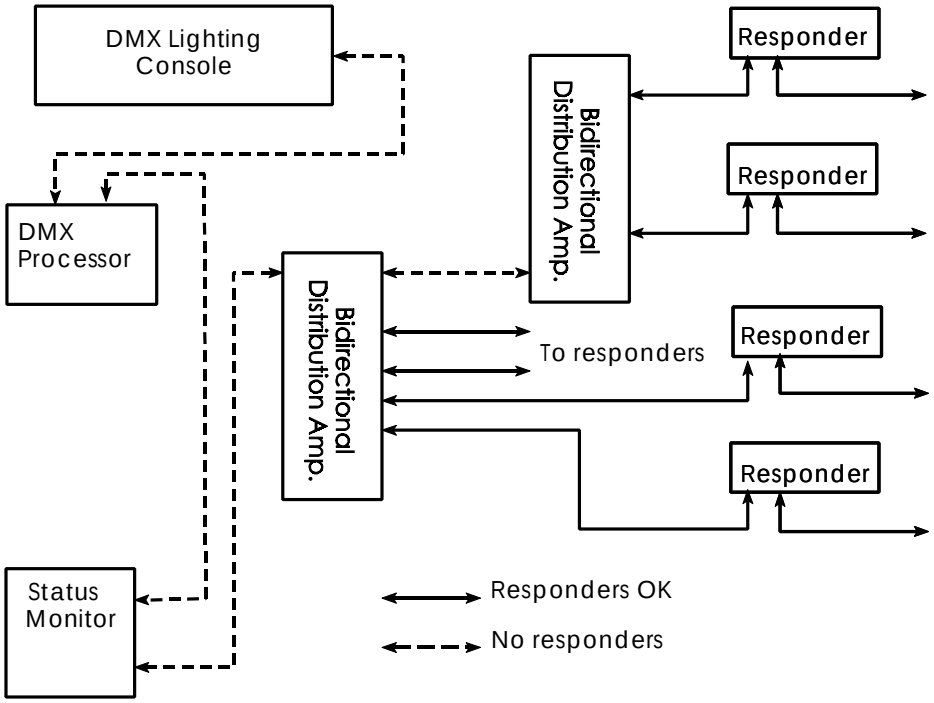

Figure B3.5.2 - Cascaded bidirectional distribution amplifiers

Figure B3.5.2 shows the proper usage of distribution amplifiers and proper placement of responders. If a DMX512 processor unit (i.e., a DMX512 combiner or backup unit) is installed, it is considered to be the source of the DMX512 data stream. If the console in Figure B3.5.2 supported talkback, it would not work because of the DMX512 processor, which would be generating a new data stream. The status monitor would work correctly since it is "downstream" of the DMX512 processor.

B4 Basic Dimmer Status Data Format

This clause is a summary of the data return format as implemented by ROSCO/Entertainment Technology. It may also be used a guideline for developing a specific format for any type of DMX512 device.

ROSCO/Entertainment Technology IPS dimmer strip and dimmer box products use RESPONSE START ID = 0, indicating that a 26-byte sequence follows the start id, in the following format:

+0	*+1*	*+2*
RESPONSE START ID	FIRMWARE VERSION	CONFIGURATION

Headend Data

+3	*+4*	*+5*	*+6*	*+7*	*+8*	*+9*	*+10*
STATUS FLAGS	ERROR FLAGS	CONFIG-URATION	DETAIL FLAGS	TEMPER-ATURE	LOAD SIZE	PRESENT LEVEL	LINE VOLT.

Dimmer # 1 Data

+11	*+12*	*+13*	*+14*	*+15*	*+16*	*+17*	*+18*
STATUS FLAGS	ERROR FLAGS	CONFIG-URATION	DETAIL FLAGS	TEMPER-ATURE	LOAD SIZE	PRESENT LEVEL	LINE VOLT.

Dimmer # 2 Data

+19	*+20*	*+21*	*+22*	*+23*	*+24*	*+25*	*+26*
STATUS FLAGS	ERROR FLAGS	CONFIG-URATION	DETAIL FLAGS	TEMPER-ATURE	LOAD SIZE	PRESENT LEVEL	LINE VOLT.

Dimmer # 3 Data

Figure B4 - IPS Return Data Stream Format

The sequence starts with two bytes describing data common to all three dimmers in the group, followed by eight bytes specific to each dimmer, in the order dimmer 1, dimmer 2, dimmer 3. The detailed format of each byte is noted in the following sections.

B5 Example return data format detail

B5.1 Headend Firmware Version

This byte allows the console or status monitor to determine what release of the operating firmware is present in the addresses bar/box. The response is formatted as follows:

BIT(S)	SIGNIFY	EXPLANATION
7-4	MAJOR	The major release level of the head-end firmware, coded as a BCD digit.
3-0	MINOR	The sub-level within a major release, as a BCD digit.

B5.2 Headend Configuration

The headend CONFIGURATION BYTE conveys information common to all dimmers in the present group, in the following format:

BIT(S)	SIGNIFY	EXPLANATION
7	ERROR AT POWER UP	If set, the headend detected a significant error during its power-up diagnostics. The specific error encountered can be determined by observing the display on the headend of the bar/box during power-up.
6	PREHEAT	If set, preheat is enabled for the bar/box. If clear, preheat is disabled for the bar/box.
5-4	FULL OUTPUT	Show the voltage to be provided as full output (i.e., level value = 255) according to the following table: Value of FULL OUTPUT / Full Voltage If 240 VOLT = 0 / Full Voltage If 240 VOLT = 1 00 / 120 / 240 01 / 115 / 230 10 / 110 / 220 11 / 100 / 200 In addition, if FULL OUTPUT = 11, a modified square law dimmer curve (customized for the 100V environment) is substituted for the standard square law curve.
3	DIMMERS 4-6	If set, this data stream is from the second group of three dimmers in a six-dimmer bar or box (see SIX DIMMER, below). If reset, the data stream is from the first group of dimmers. This bit, when used with SIX DIMMER, allows a monitor to correctly determine the base address of the bar/box associated with a data stream.
2	ANALOG OPTION ABSENT	If set, the headend does not have AMX192 or 0-10V analog control capabilities. If reset, an analog option is present.
1	SIX DIMMER	If set, the bar/box contains six dimmers; if reset, the bar/box is configured for three dimmers.
0	120 VOLT	If set, the bar/box is configured for 100/120V operation; if reset, the bar/box is configured for 220/230/240V operation.

B5.3 Dimmer Status

The dimmer status byte summarizes the dimmer's operating status, including an indication if any serious errors are present, in the following format:

BIT(S)	SIGNIFY	EXPLANATION
7	NO RESPONSE	Set if the dimmer did not respond to the last command and may be absent or non-functional.
6	NON-DIM	Indicates that the dimmer is now running as a non-dim if set; if clear indicates normal operation.
5	VARIABLE FREQUENCY	Set if the line frequency has been outside the range 59.5-60.5 Hz or 49.5-50.5 Hz for at least eight consecutive line cycles.
4	LOCAL MODE	Set if the level now implemented by the dimmer came from the local FOCUS button.
3	NO LOAD	Set if the load current is too small to be accurately sensed, hence there is no load or a very small load.
2	INDUCTIVE LOAD	Set if the load or source has been determined to be inductive, and the dimmer is operating in Forward Phase Control mode as a result. (Additional information on how the inductive load was sensed is supplied by the FPC CAUSE bit in the DIMMER DETAIL byte.)
1	REDUCED RISE/FALL	Set if the dimmer is using short (250 µS) rise and falltimes due to high power device temperature.
0	ERROR PRESENT	Set if at least one of the error flags in DIMMER ERRORS is now set.

B5.4 Dimmer Errors

The DIMMER ERRORS byte notes all fatal and non-fatal error conditions. Fatal conditions will also be flagged by lighting the red LED on the dimmer. As soon as a fatal error has been reported, the dimmer will rerun its startup diagnostics in an attempt to clear the error condition.

DIMMER ERRORS has the following format:

BIT(S)	SIGNIFY	EXPLANATION
7	MISWIRE	Set if dimmer power-up diagnostics sense a line voltage greater than approximately 185 Vrms in 120V units (370 VRMS in 240V units), indicating a likely miswire. (FATAL)
6	WATCHDOG RESET	Set if dimmer firmware has been restarted after a software loop took too long (>49.2 mS) to execute. This bit is automatically reset after 10 seconds.
5	DIMMER POWER SUPPLY UNDERVOLT	Set if the dimmer's power supply output drops below a determined value. This bit is reset when the supply output exceeds another determined value, and the line voltage is at least 90 VRMS for 120 V units (180 VRMS for 240V units).
4	TEMPERATURE SHUTDOWN	Set if the dimmer is shutdown due to the temperature of the power devices being too high or too low. Shutdown occurs if the temperature is below -20° C or above 95° C. This condition is reset when the temperature is in the range -15-90° C and the dimmer's operating level has been set to zero by a level message or the FOCUS button.
3	OVERLOAD SHUTDOWN	Set if the dimmer has detected an overload (excessive current) condition, either due to a short circuit or because the connected load exceeds its rating, based on the CAPACITY field of its configuration data: Value of CAPACITY / Overload if Full Output = 120/220/230/240V / Output if Full Output = 100V 000 — 1700W — 1300W 001 — 3300W — 2600W 010 — 4900W — 3800W 011 — 6500W — 5100W 100 — 8200W — 6300W 101 — 9800W — 7600W 110 — 1700W — 1300W 111 — 16300W — 12600W This condition is reset when the dimmer's operating level has been set to zero by a level message or by the FOCUS button; if the overload is still present, the dimmer will shutdown again in several seconds.
2	NEGATIVE SWITCH FAILURE	Set by power-up diagnostics if the negative power device conducts current even when off. This condition can be detected only if a load is present. (FATAL)
1	ROM CHECKSUM FAILURE	Set by power-up diagnostics if the dimmer firmware shows an incorrect checksum and may damaged. (FATAL)
0	ANALOG SECTION FAILURE	Set by power-up diagnostics if the voltage or current sensing electronics are non-functional. (FATAL)

B5.5 Dimmer Configuration

The dimmer configuration byte describes software- and hardware-selected configuration attributes, in the following format:

BIT(S)	SIGNIFY	Explanation
7	NON-DIM	Set if configured as a non-dim; cleared if configured as dimmer.
6	LINEAR VOLTAGE	Set if linear voltage curve is selected; reset if standard or modified square law.
5	FORCE FORWARD PHASE CONTROL	Set if dimmer is forced to operate only in forward (conventional) phase control mode; reset if dimmer is operating normally and chooses either reverse or forward phase control based on the load type.
4	FORCE REDUCED RISE/FALL	Set if dimmer is forced to operate with short (250 µS) rise/falltime; reset if dimmer is operating normally and chooses appropriate rise/falltime based on power device temperature.
3	240 VOLT	Set if 220/230/240V unit; reset if 100/120V unit. If the unit is a hybrid 120/240V dimmer, this bit indicates the present line voltage.
2-0	CAPACITY	Indicates the power handling capacity of the dimmer: Value of CAPACITY — Output if Full Output = 120/220/230/240V — Output if Full Output = 100V 000 — 1200W — 1000W 001 — 2400W — 2000W 010 — 3600W — 3000W 011 — 4800W — 4000W 100 — 6000W — 5000W 101 — 7200W — 6000W 110 — 1200W — 1000W 111 — 12000W — 10000W

B5.6 Dimmer Detail

The DIMMER DETAIL byte provides additional status information, in the following format:

BIT(S)	SIGNIFY	EXPLANATION
7-6	RESERVED	Reserved by ET for future use; presently used for debugging/maintenance information and should be ignored.
5	FPC CAUSE	When the dimmer reports an inductive load and has switched to Forward Phase Control mode (see STATUS, above) this bit indicates why the load was determined to be inductive. If cleared, the load showed inductive characteristics during the first cycle of conduction; if set, the load initially did not appear inductive, but a large number of subsequent cycles showed large voltage kickbacks.
4	OVER 140 VOLTS	If set, the last line voltage determined exceeded 140 VRMS in 120V units (280VRMS in 240V units) and cannot be reported accurately. When this bit is set, line voltage will be reported as 140. Reset as soon as the line voltage drops below 140VRMS in 120V units (280VRMS in 240V units).
3	NOT CONFIGURED	Set if the dimmer has just executed power-up diagnostics and requires initialization by the associated headend processor. Note that this condition can occur during normal operation if the headend and the dimmer are operating on different power sources or phases, and only the dimmer's power fails. This bit clears automatically after the dimmer is re-initialized.
2	EXTENDED RISE/FALL	Set if dimmer is configured to support extended (800 µS) falltime and device temperatures allow that mode to be used now.
1-0	OVERLOAD CAUSE	Specifies why an overload shutdown (see ERRORS above) occurred. Code — Explanation 00 — Too many hardware-detected overloads (load current is not controllable) 01 — Load has "warmed up" but size of load exceeds dimmer's rated safe capacity 10 — Unit is operating as a non-dim and has detected too many inductive kickbacks 11 — Load will not "warm up" - after 7-8 seconds current has not dropped to valid level

B5.7 Dimmer Temperature

The DIMMER TEMPERATURE byte is an 8-bit unsigned number denoting the present temperature of one of the dimmer's pair of power devices (where possible, the "case temperature" of the power device is what is measured). The value is returned in degrees Centigrade, in the range 0-100; temperatures less than 0 will report as 0, and temperatures greater than 100 will report as 100. The device temperature is updated once per line cycle.

Note that a broken thermistor connection will cause the dimmer to report a temperature of 0. Any attempt to bring the dimmer to a non-zero level with a missing or broken thermistor will cause a TEMPERATURE SHUTDOWN (see ERRORS, above).

B5.8 Dimmer Load Size

The DIMMER LOAD size byte gives the dimmer's most recent determination of the size of the connected load. The response is an 8-bit unsigned integer denoting the load size in hundred of watts. The load size is defined as the rating printed on the lamp (i.e., power consumption at nominal full voltage), as opposed to the instantaneous power being used by the lamp, which would vary with the level requested.

Dimmers configured for 120V operation assume a nominal lamp voltage of 120V, unless full output voltage is set to 100V, in which case the nominal lamp voltage is 100V. For 240V units, load sizes are computed for a nominal lamp voltage that matches the set full output voltage of either 220V, 230V or 240V.

The load size is recomputed ever sixty line cycles, once the lamp has "warmed up" and is operating at a level greater than or equal to 20% (i.e., a level value of 51 out of 255). The dimmer computes the load size from the RMS load current, which may take a number of seconds to stabilize for very large lamps, hence there can be a five to ten second delay after the lamp warms up before a new load size is reported.

Please note that reported load sizes are accurate to roughly $\pm$10%, and that many incandescent lamps have a substantial manufacturing tolerance, consequently the reported size may not always exactly match the value marked on the lamps.

B5.9 Dimmer Level

The DIMMER LEVEL byte is an 8-bit unsigned integer (range 0-255) denoting the present operating level. That level may have been set through a DMX512 packet transmitted by the console, or from the action of the local FOCUS button. If the dimmer is presently in TEMPERATURE SHUTDOWN or OVERLOAD SHUTDOWN (see ERRORS, above), the level reported will be that which is presently requested, even though the dimmer is at zero conduction.

B5.10 Dimmer Line Voltage

DIMMER LINE VOLTAGE notes the dimmer's most recent determination of the RMS line voltage as an 8-bit unsigned integer. For 120V units (i.e., units that report configuration bit 240 VOLT as a zero), the value returned is the voltage, in the range 0-140. For 240V units (i.e., 240 VOLT = 1), the value returned is one-half of the voltage. If the line voltage exceeds the maximum specification (140 VRMS for 120V units; 280 VRMS for 240V units), the dimmer cannot accurately determine the exact voltage, and will return the value 140 with the OVER 140 VOLTS bit set in the response to DIMMER DETAIL.

The dimmer recomputes the line voltage once per line cycle, except during the lamp warmup and during load size determination cycles.

-end of Annex B-

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Annex C (Normative) - Device Interconnection Table

The following table provides a means for identifying legitimate ways in which the interconnection of different TYPEs of equipment may be made. It is a guide to whether the user may expect enhanced functionality of interconnected products using Pins 4 & 5. Generally only like types provide increased functionality. Since TYPE 1 is simply a device that passes through any signals present on Pins 4 & 5 (loop-through), the TYPE of equipment upstream (transmitting) or downstream (receiving) of the TYPE 1 device must be examined to determine functionality of the system.

If enhanced functionality is needed, a C2 Scheme cable is required and is equivalent to a TYPE 1 device. For isolating conflicting uses of Pins 4 & 5, a C1 Scheme cable (equivalent to a TYPE 0 device) is used.

The interconnection of products using Accessory Power (+24 VDC) and claiming compliance with this standard as DMX512/2000AP is outside the scope of this Standard. Such equipment requires the use of special cables with an EIA-485 data pair and high current conductors. Such cables shall not be labeled as DMX512 cables. Users of such products should refer to the manufacturers for guidance.

Table C - Interconnection cross-check (electrical / functional)

Rx / Tx	Legacy Product	Rx TYPE 0	Rx TYPE 1	Rx TYPE 2	Rx TYPE 3	Rx TYPE 4	Rx TYPE 5
Legacy Product	note 4		notes 1, 4	note 4	note 4	note 4	note 4
Tx TYPE 0							note 5
Tx TYPE 1	notes 1, 4		note 1	note 1	note 1	note 1	note 1
Tx TYPE 2	note 4		note 1	note 2	note 6	note 6	note 6
Tx TYPE 3	note 4		note 1	note 6	note 2	note 6	note 6
Tx TYPE 4	note 4		note 1	note 6	note 6	note 3	note 6
Tx TYPE 5	note 4	note 5	note 1	note 6	note 6	note 6	note 3

Notes:
Blank Cell - No enhanced functionality possible. Use of a C1 (C5.1) Scheme cable is all that is required. Use of a C2 (C5.2) scheme cable does no harm.

1) Loop-through (passive link) functionality when used with a C2 (C5.2) scheme cable. The TYPE of the upstream (transmitting) or downstream (receiving) device must be examined.
2) Enhanced functionality requires use of C2 (C5.2) scheme cable.
3) Refer to manufacturers' data, as enhanced functionality is unlikely with products of different manufacturers. Enhanced functionality, requires use of C2 (C5.2) scheme cable.
4) Refer to manufacturers' data, as enhanced functionality is unlikely with products of different manufacturers. Enhanced functionality requires use of C2 (C5.2) scheme cable. Connection to legacy product compliant with EIA-485 should not cause damage. Use of a C1 (C5.1) Scheme cable would ensure no electrical damage or conflict is possible.
5) No enhanced functionality expected. Note that TYPE 5 equipment may be dependent of the existence of signals on Pins 4 and 5 of the connected equipment for basic operation.
6) No enhanced functionality. Direct interconnection of these types of device should not cause electrical failure as this has been covered by the limits for electrical protection defined in this Standard. Use of a C1 (C5.1) Scheme cable would ensure no electrical damage or conflict.

-end of Annex C-

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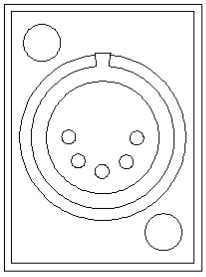
Annex D (Normative) - Port Marking Style Sheet

DESIGN CRITERIA

(1) Simple but informative
(2) Single color - to simplify silk screen applications – Manufacturer free to choose color
(3) Small enough to use adjacent to XLR connector
(4) Available as encapsulated postscript file and suitable for silkscreen at (typically) 60 dpi resolution
(5) TYPE and Grounding schemes shall be identified – Use of TYPE Symbols is optional



Optional TYPE Symbols
TYPE 0
TYPE 1
TYPE 2
TYPE 3
TYPE 4
TYPE 5
TYPE 6

DMX512/2000
TYPE 0 : ISOLATED

TYPE 0 Isolated Transmitter -
Pins 4 & 5 Not Used

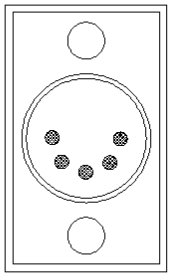
USITT DMX512/2000
TYPE 1

TYPE 1 Ground Referenced
Transmitter (Processor) -
Pins 4 & 5 Loop-Through

DMX512/2000
TYPE 2 : FLOATING

TYPE 2 Floating Transmitter -
2nd DMX512 Universe
on Pins 4 & 5

Receiver Pin 1 Grounding
Concession Marking
⚠ PIN 1 ⏚ ⚠



TYPE 5 Isolated Receiver -
Limited Current 12 VDC
on Pins 4 & 5;
Permanently Terminated

DMX512/2000
TYPE 5 : ISOLATED
TERM

TYPE 2 Grounded Receiver -
2nd DMX512 Universe on Pins 4 & 5;
Termination is Switchable;
Can Accept a 4µSec MAB

DMX512/2000 (4 µSec)
TYPE 2 :
⚠ PIN 1 ⏚ ⚠

-end of Annex D-

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Annex E (Normative) - Protocol Implementation Compliance Statement (PICS)

Manufacturers claiming compliance with this Standard shall complete and hold on file a Protocol Implementation Compliance Statement (PICS) as defined in this Annex E. Copies of the PICS shall be made available on request.

Question		Reference			Response	
#	Compliance	Page	Clause	Lines	Y / N / NA	Notes

-end of Annex E-

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Inside Back Cover

ESTA Technical Standards Manager:
Karl Ruling

ESTA Control Protocols Working Group - Co-Chairs:
Steve Carlson, Rosco / ET
Steve Terry, Production Arts - Production Resource Group

ESTA Control Protocols Working Group - DMX512 Task Group Members:
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Milton Davis, Strand Lighting
Doug Fleenor, Doug Fleenor Design
Bob Goddard, Goddard Design
Ted Paget, Jones & Phillips
Steve Terry, Production Arts - Production Resource Group

Germany
Eckart Steffens, Soundlight; VPLT

UK
Tim Cox, PLASA
Tony Douglas-Beveridge, PLASA
Wayne Howell, Artistic Licence
Paul Mardon, Pulsar Light of Cambridge
Steve Unwin, Pulsar Light of Cambridge
Peter Willis, Andera Ltd.

Back Cover

Comments submittal form for: BSR E1.11, Entertainment Technology - USITT DMX512, Asynchronous Serial Digital Data Transmission Standard for Controlling Lighting Equipment and Accessories (CP98/1031r1.1a)

Clause, page, and line numbers:

Proposed changes:

(Please use ~~strikethrough~~ to indicate deletions, and <u>underline</u> to indicate additions)

Substantiation:

I hereby grant ASC E1 and ESTA the non-exclusive, royalty-free rights to use my comments, and I understand that I acquire no rights in any publication in which my comments are used.

Signature: _____

Date: _____

Name: _____
(Please print)

Organization: _____

Street Address: _____

City: _____

State/Prov: _____ Postal Code: _____

Country: _____

Telephone: _____

Fax: _____

Email: _____

Please return the completed comments form to dmx-rfc@DesignRelief.com via e-mail, or mail it to:

Technical Standards Manager
ESTA
875 Sixth Avenue, Suite 2302
New York, NY 10001
Fax: 212-244-1502

Deadline for comments: 4:00 p.m. EST, January 12, 2000

Comment form instructions:

When commenting, please provide the following:

- clear identification of the relevant clause, page, and line numbers;
- the proposed change marked in legislative format, with strikethroughs to indicate deleted text and underlines to indicate new text;
- substantiation for the change; and
- a wordprocessing file of the proposed changes (Word Perfect, Word 97 or lower, or RTF), with each proposal on a separate page.

Please send yoru comments as electronic submissions to dmx-rfc@DesignRelief.com. If you want to mail hard copy submissions, please send them to:

Technical Standards Manager
ESTA
875 Sixth Avenue, Suite 2302
New York, NY 10001
USA
Fax: +1-212-244-1502

All submissions must be received no later than 4:00 p.m. ET, January 12, 2000.

Background and what's new in this draft standard document:

The original version of the DMX512 standard was developed in 1986 by the Engineering Commission of the United States Institute for Theatre Technology, Inc. (USITT). Minor revisions were made in 1990 to create "DMX512/1990, Digital Data Transmission Standard for Dimmers and Controllers." The 1986 and 1990 versions covered only data used by dimmers. In practice, the standard has been used for controlling a wide variety of devices.

In 1998 it became evident that additional updates to the standard were necessary and that formal recognition through an internationally recognized standards organization was required. The USITT DMX512 Subcommittee issued a Call for Comments in order to solicit recommendations for changes to the standard. At the same time, USITT transferred maintenance of DMX512 to the Entertainment Services and Technology Association (ESTA).

The revision effort was taken up by the ESTA Technical Standards Program's Control Protocols Working Group, which appointed a task group to act on the proposals received from USITT's Call for Comments. The task group established several goals as part of their work:

1. Produce a consensus document following proper standards procedures.
2. Make editorial updates to DMX512 appropriate for current times.
3. Add technical features while maintaining a balance with backward compatibility, including formalizing the management of alternate start codes.
4. Identify among the proposals received in response to the Call for Comments which ones belong in an application note or a recommended practice instead of in the standard.
5. Take actions on these proposals and deliver a draft of a revised DMX512 standard to the Control Protocols Working Group (CPWG).

New concepts introduced in this current draft standard include:

- Structural changes to the written document, including the use of annexes
- Definitions & terminology
- Physical layer details / Earth grounding practices
- DMX512 Types (classification of the uses of the second pair)
- Protection

- Marking of ports
- Two distinct methods of delivering DC power
- System information packet (e.g., checksums - Clause 7)
- Alternate START code management

Changes already anticipated include the addition of an introductory overview clause and relocation of portions of the body of the standard to annexes.