AN11158

Understanding power MOSFET data sheet parameters

Rev. 3 — 7 January 2013 Application note

Document information

Info	Content
Keywords	MOSFET.
Abstract	This application note describes the content of power MOSFET data sheet parameters

Revision history

Rev	Date	Description
v.3	20130107	figure cross reference correction and temperature qualifier added on page 10
v.2	20120816	second release
v.1	20120416	initial release

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1. Introduction

This user manual explains the parameters and diagrams given in an NXP Semiconductors Power MOSFET data sheet. The goal is to help an engineer decide what device is most suitable for a particular application.

It is important to pay attention to the conditions for which the parameters are listed, as they can vary between suppliers. These conditions can affect the values of the parameters making it difficult to choose between different suppliers. Throughout this document, the data sheet for the BUK7Y12-55B is used as an example. BUK7Y12-55B is an automotive-qualified part in an SOT669 (LFPAK56) package, with a voltage rating of 55 V.

The layout of this data sheet is representative of the general arrangement of NXP power MOSFET data sheets.

NXP Power MOSFETs are designed with particular applications in mind. For example, switching charge is minimized where switching losses dominate, whereas on-resistance is minimized where conductive losses dominate.

2. Data sheet technical sections

2.1 Product profile

This section provides the overview of the device; giving the designer the key information regarding device suitability. The general description describes the technology used; key features and example applications are listed.

The quick reference data table contains more detailed information and the key parameters for the intended application. An example of a quick reference data table is shown in Table 1 “Quick reference data”.

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	55	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Figure 1	-	-	61.8	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Table 3	-	-	105	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C;	-	8.2	12	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	I_D = 20 A; V_{DS} = 44 V; V_{GS} = 10 V;	-	14.8	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 61.8 A; $V_{sup} \leq 55$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C: unclamped	-	-	129	mJ

The general format for describing a parameter is to provide the official symbol and then the correct parameter name. Any relevant conditions and information are listed after the parameter names. The values and units of the values are entered in the last two columns. All entries conform to IEC60747-8.

The quick reference data parameters are described in more detail in the characteristics section of the data sheet. The following list is an introduction to some of the key issues together with their interpretation:

V_{DS} - the maximum voltage between drain and source that the device is guaranteed to block in the off state. This section of the data sheet deals with the most commonly used temperature range, as opposed to the full temperature range of the device.

I_D - the maximum continuous current the device can carry with the mounting base held continuously at 25 °C with the device fully on. In the example provided in Table 1, **I_D** requires a V_{GS} of 10 V.

P_{tot} - the maximum continuous power the device can dissipate with the mounting base held continuously at 25 °C.

$R_{DS(on)}$ (drain-source on state resistance) - the typical and maximum resistance of the device in the on-state under the conditions described. $R_{DS(on)}$ varies greatly with both T_j and the gate-source voltage (V_{GS}). Graphs are provided in the data sheet to assist in determining $R_{DS(on)}$ under various conditions.

Q_{GD} (gate-drain charge) - an important switching parameter that relates to switching loss, along with Q_{GS} and $Q_{G(tot)}$. Q_{GD} is inversely proportional to $R_{DS(on)}$, therefore choosing an appropriate balance between $R_{DS(on)}$ and Q_{GD} is critical for optimal circuit performance.

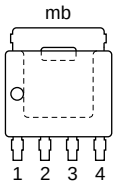
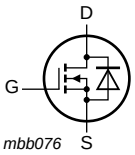
Q_{OSS} (output charge) - an increasingly important switching parameter in modern MOSFETs, as the other switching parameters have been optimized.

$E_{DS(AL)S}$ (non-repetitive drain-source avalanche energy) - describes the maximum energy allowed in any voltage spike or pulse that exceeds the V_{DS} rating of the device. Exceeding this rating, runs the risk of damaging the device. This parameter describes what is commonly referred to as "ruggedness" that is the ability of the device to withstand overvoltage events.

2.2 Pinning information

This section describes the internal connections and general layout of the device. Note that the symbol is for an enhancement n-channel MOSFET with the source and body tied together, and a parallel diode between the source and drain. The parallel diode is known as the body diode and is inherent in power MOSFETs. N-channel power MOSFETs have the body diode between drain and source, as shown in Table 2.

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mount base: connected to drain		

2.3 Ordering information

The ordering section provides information on how to order the device.

2.4 Limiting values

The limiting values table provides the range of operating conditions allowed for the MOSFET. The conditions are defined in accordance with the absolute maximum rating system (IEC60134). Operation outside of these conditions is not guaranteed, so it is recommended that these values are not exceeded. Doing so runs the risk of immediate device failure or reduced lifetime of the MOSFET. The avalanche ruggedness conditions, when given, describe the limited conditions for which the V_{DS} rating can be exceeded.

To calculate how the limiting values change with temperature, they are read together with the derating curves provided.

The limiting values table for the BUK7Y12-55B is given as an example of a standard limiting values table, in Table 3.

Table 3. Limiting values

In accordance with the absolute maximum rating system IEC 60134

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	55	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ	-	-	55	V
V_{GS}	gate-source voltage		–20	-	+20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Table 1; Figure 1	-	-	61.8	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Table 1	-	-	43.7	A
I_{DM}	peak drain current	V_{GS} = 10 V; T_{mb} = 25 °C; pulsed; Figure 1	-	-	247	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	-	-	105	W
T_{stg}	storage temperature		–55	-	+175	°C
T_j	junction temperature		–55	-	+175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	-	-	61.8	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C	-	-	247	A

Table 3. Limiting values *...continued*

In accordance with the absolute maximum rating system IEC 60134

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 61.8 A; $V_{sup} \leq$ 55 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C: unclamped		-	-	129	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[1][2][3]	-	-	-	mJ

[1] Single pulse avalanche rating limited by a maximum junction temperature of 175 °C

[2] Repetitive avalanche rating limited by an average junction temperature of 170 °C

[3] Refer to application note *AN10273* for further information

V_{DS} (drain-source voltage) - the maximum voltage the device is guaranteed to block between the drain and source terminals in the off-state for the specified temperature range. For the BUK7Y12-55B, the temperature range is from +25 °C to +175 °C. For operation below 25 °C, the V_{DS} rating reduces due to the positive temperature coefficient of avalanche breakdown. This is covered in Section 2.4.1 of this document.

V_{GS} (gate-source voltage) - the maximum voltage the device is specified to block between the gate and source terminals. Some NXP data sheets specify different values for DC and pulsed V_{GS}. In these cases the DC value is a constant gate voltage over the lifetime of the device at the maximum T_j, whilst the higher-value pulsed-rating is for a shorter, specified accumulated pulse duration at the maximum specified T_j.

Gate-oxide lifetime reduces with increasing temperature and/or increasing gate voltage. This means that V_{GS} lifetimes or ratings quoted for lower junction temperatures are significantly greater than if specified at higher temperatures. This can be important when comparing data sheet values from different manufacturers.

V_{DGR} (drain-gate voltage) is typically the same value as the V_{DS} rating.

I_D (drain current) - the maximum continuous current the device is allowed to carry under the conditions described. This value can be related to either package construction, or the maximum current that would result in the maximum T_j. As such it depends on an assumed mounting base temperature (T_{mb}), the thermal resistance (R_{th}) of the device, and its $R_{DS(on)}$ at maximum T_j.

Note that some suppliers quote the "theoretical" silicon limit, while indicating the package limited limit in the characteristic curves.

I_{DM} (peak drain current) - the maximum drain current the device is allowed to carry for a pulse of 10 μs or less.

P_{tot} (total power dissipation) is the maximum allowed continuous power dissipation for a device with a mounting base at 25 °C. The power dissipation is calculated as that which would take the device to the maximum allowed junction temperature while keeping the mounting base at 25 °C. In reality, it is difficult to keep the mounting base at this temperature while dissipating the 105 W that is the calculated power dissipation for the BUK7Y12-55B. In other words, P_{tot} indicates how good the thermal conductivity of the device is, and its maximum allowed junction temperature.

Note that some other semiconductor vendors quote performance when mounted on a copper PCB usually 1 inch square. In practice, this information is rather meaningless as the semiconductor vendor has no control over how the device is cooled. See *AN10874 - LFPAK MOSFET thermal design guide*. AN10874 describes different techniques that can be used during the design phase to ensure that the PCB layout provides optimum thermal performance.

T_{stg} (storage temperature) is the temperature range in which the device can be stored without affecting its reliability. Long term storage should be in an inert atmosphere to prevent device degradation, for example, by tarnishing of the metal leads.

T_j (junction temperature) is the operational temperature range of the device. Typically, **T_j** is the same as the storage temperature. Outside of this range, device parameters are outside the range of the data sheet and device lifetime is reduced.

I_S (source current) - the maximum continuous current of the MOSFET body diode, which is briefly discussed in Section 2.2. The same considerations apply as for I_D.

I_{SM} (peak source current) - the maximum current pulse that the MOSFET body diode is guaranteed to carry. The same considerations apply as for I_{DM}.

$E_{DS(AL)S}$ (non-repetitive drain-source avalanche energy) - the maximum allowed single overvoltage energy pulse under the conditions specified. For this example, the conditions are the maximum continuous drain current allowed for a mounting base temperature of 25 °C. The avalanche energy allowed is the energy pulse that would raise the device temperature from 25 °C to its maximum allowed T_j, while the mounting base temperature is held at 25 °C.

The avalanche energy is specified for the maximum continuous drain current. Some vendors specify the avalanche energy for a different current and higher inductive load, which can increase the apparent avalanche energy for an inferior performance. An example is given with the derating curve as described in Section 2.4.3 of this document.

$E_{DS(AL)R}$ (repetitive drain-source avalanche energy) - the maximum amount of energy allowed in any single avalanche event when there is more than one avalanche event. There are thermal constraints on a repeated avalanche operation that are in section 2.4.3 of this document. There are also the standard thermal requirements in addition to the energy requirements for repetitive avalanche events. These requirements are assessed with the thermal characteristic curves as described in Section 2.5. *Avalanche performance is covered in detail in application note AN10273.*

This parameter is only listed on NXP data sheets where the repetitive avalanche capability has been assessed. It is not shown in NXP data sheets where it has not been assessed, for example non-automotive MOSFETs.

2.4.1 Derating curves

The derating curves are provided immediately after the tabulated limiting value data, and help the designer calculate how the limits change with temperature.

2.4.1.1 Continuous drain current

The followings procedure serves as an example to calculate the maximum continuous drain current for the BUK7Y12-55B. Assume an application with a mounting base temperature T_{mb} of 75 °C.

Refer to the graph depicted in Figure 1 which depicts the continuous drain current as a function of mounting base temperature.

Figure 1 shows that for a T_{mb} of 75 °C, the maximum continuous drain current has reduced from 61.8 A, listed at 25 °C, to 50 A.

The maximum current at any T_{mb}, is the current that increases T_j to the maximum allowed temperature (175 °C). $P = I^2 \times R_{DS(on)}$ represents the power dissipation at T_j, where the $R_{DS(on)}$ used is the maximum value for the maximum T_j. Therefore, the allowed current is proportional to the square root of the allowed power dissipation.

The power dissipation allowed for a given T_{mb} is proportional to the allowed temperature increase. This means that the derating curve shown, is based on the following equations:

$$I_D{}^2(T_{mb}) \propto \frac{T_j - T_{mb}}{T_j - 25\ ^\circ C} \quad (1)$$

$$I_D{}^2(T_{mb}) = I_D(25\ ^\circ C) \times \sqrt{\frac{T_j - T_{mb}}{T_j - 25\ ^\circ C}} \quad (2)$$

At the maximum allowed junction temperature of 175 °C, this current has decreased to zero.

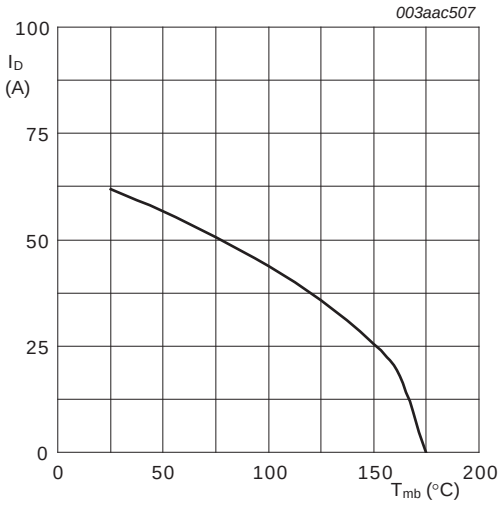


Fig 1. Continuous drain current as a function of mounting base temperature

2.4.2 Power dissipation

Power dissipation varies with different temperatures. However, in this case, the power dissipation curve is normalized. The allowed power is presented as a percentage of the allowed power dissipation at 25 °C, as opposed to an absolute value.

Example:

By observing the curve in Figure 2, the allowed power dissipation for a T_{mb} of 75 °C is approximately 66 % of that allowed at 25 °C.

The graphic data in Figure 2, shows the maximum continuous power dissipation (P_{tot}) at 25 °C is 105 W.

This means that the maximum power dissipation allowed at 75 °C, is 66 % of 105 W which is 70 W.

Equation 3 is the equation to calculate power dissipation:

$$P_{tot}(T_{mb}) = P_{tot}(25\ ^{\circ}C) \times \frac{T_j - T_{mb}}{T_j - 25\ ^{\circ}C} \quad (3)$$

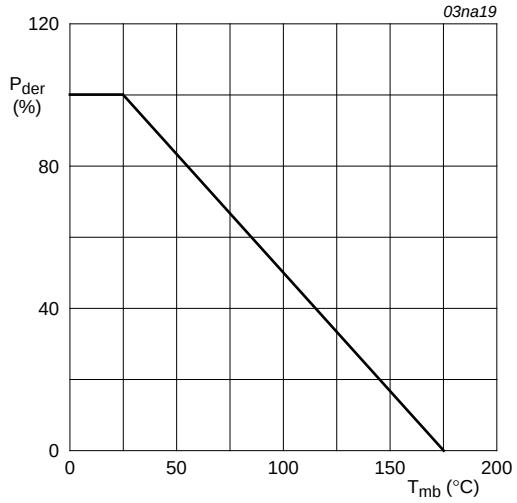
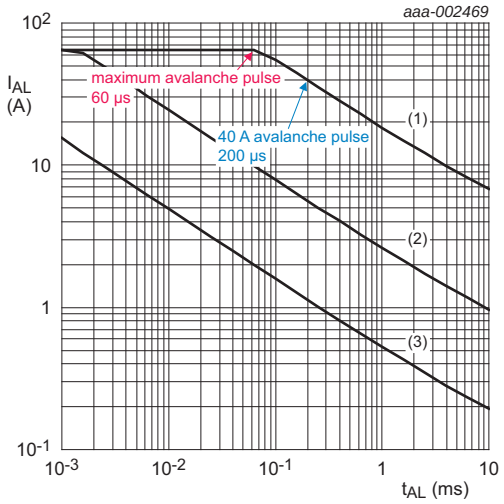


Fig 2. Normalized total power dissipation as a function of mounting base temperature

The curves provided in Figure 1 and Figure 2 are read in conjunction with the limiting values tables. The information extracted, assists in calculating the maximum current allowed and the power dissipation with respect to temperature.

2.4.3 Avalanche ruggedness

Avalanche ruggedness is covered in detail in *AN10273*.



Single-shot and repetitive avalanche rating

(1) Single pulse; T_j = 25 °C

(2) Single pulse; T_j = 150 °C

(3) Repetitive

Fig 3. Avalanche current as a function of avalanche period

A simple example for the BUK7Y12-55B, using the information in *AN10273*, is extracted from the limiting values Table 3:

With I_D = 61.8 A, $V_{sup} \leq$ 55 V, R_{GS} = 50 Ω, V_{GS} = 10 V and $T_{j(init)}$ = 25 °C unclamped, the maximum $E_{DS(AL)S}$ is 129 mJ.

An avalanche event has a triangular pulse shape, so the average power is calculated as ($0.5 \times V_{DS} \times I_{DS}$).

AN10273 states that the assumed breakdown voltage is 130 % of the rated voltage (55 V × 1.3).

Figure 3 shows a maximum current of just above 60 A at 25 °C (the limiting values Table 3 shows that it is actually 61.8 A).

The time for the maximum avalanche energy can be read from Figure 3 as 60 µs.

This means that the maximum avalanche energy allowed is:
0.5 × (55 V × 1.3) × 61.8 A × 60 µs = 133 mJ.

This value is approximately the 129 mJ quoted in the limiting value Table 3.

If a competitor quotes avalanche energy at 40 A, the graph shows that the avalanche time is now 200 µs. The avalanche energy is now 0.5 × (55 V × 1.3) × 40 A × 200 µs = 286 mJ.

Ruggedness events lie outside the Safe Operating Area (SOA).

2.4.4 Safe Operating Area (SOA)

The Safe Operating Area (SOA) curves are some of the most important on the data sheet.

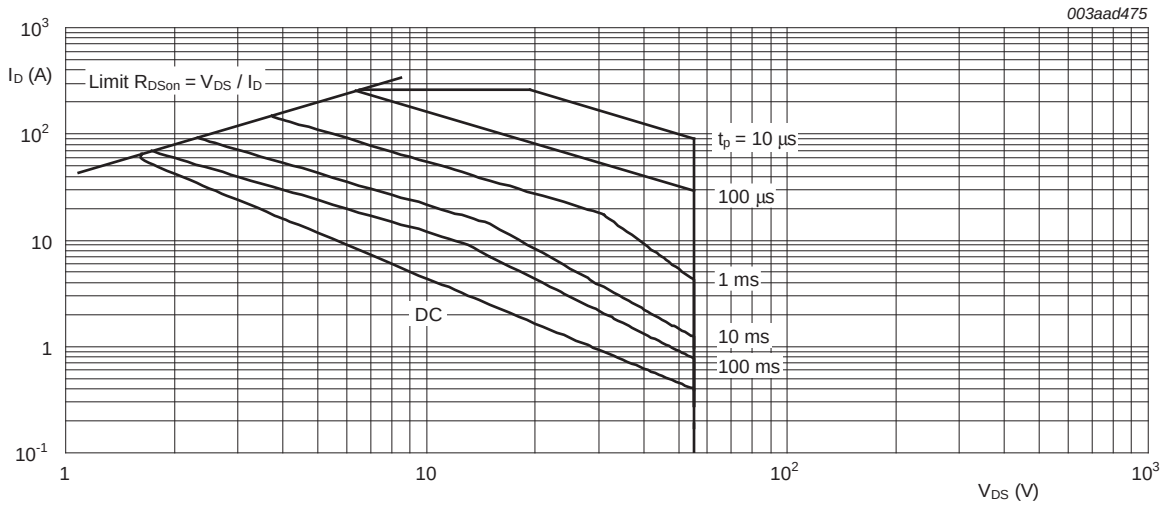


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

The SOA curves show the voltage allowed, the current and time envelope of operation for the MOSFET. These values are for an initial T_{mb} of 25 °C and a single current pulse. This is a complex subject which is further discussed in the appendix (Section 3.1).

2.5 Thermal characteristics

This section describes the thermal impedance as a function of pulse duration for different duty cycles. This information is required to determine the temperature that the silicon reaches under particular operating conditions, and whether it is within the guaranteed operation envelope.

The thermal characteristics are shown in Figure 5. The thermal impedance changes with pulse length because the MOSFET is made from different materials. For shorter durations, the thermal capacity is more important, while for longer pulses, the thermal resistance is more important.

The thermal characteristics are used to check whether particular power loading pulses above the DC limit would take T_j above its safe maximum limit. Repetitive avalanche pulses must be considered in addition to the constraints specific to avalanche and repetitive avalanche events.

Table 4. Characteristics table

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	1.42	K/W

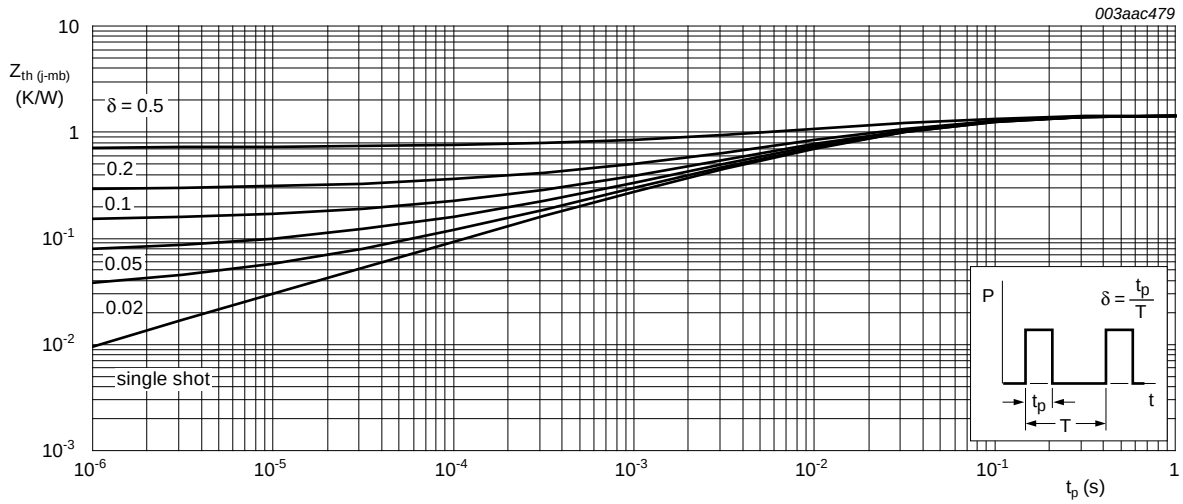


Fig 5. Thermal characteristics

Thermal resistance (R_{th}) and thermal impedance (Z_{th}) are related because the thermal resistance is the steady-state measure of how the device blocks heat flow. Thermal impedance is how the device responds to transient thermal events. It involves different thermal capacities of parts of the device and the thermal resistances between these parts. Under DC conditions, Z_{th} is equal to R_{th}. Equation 4 represents the temperature rise for a particular power dissipation:

$$\Delta T_j = \left|Z_{th(j-mb))}\right| \times Power \tag{4}$$

A worked example is discussed in the appendix (Section 3.1.2).

2.6 Electrical characteristics

This section is used to determine whether the MOSFET would be suitable in a particular application. This section differs from the previous two sections that are used to determine whether the MOSFET would survive within the application. The examples in this section are taken from the data sheet for the *BUK7Y12-55B* unless otherwise stated.

2.6.1 Static characteristics

The static characteristics are the first set of parameters listed in this section and an example is shown in Table 5:

Table 5. Static characteristics

List of constants and limitations relating to the table i.e. voltages, currents and temperatures

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V; T_j = 25 °C	55	-	-	V
		I_D = 250 μA; V_{GS} = 0 V; T_j = −55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C	2	3	4	V
		I_D = 250 mA; V_{DS} = V_{GS}; T_j = −55 °C	-	-	4.4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C	1	-	-	V

Table 5. Static characteristics *...continued*

List of constants and limitations relating to the table i.e. voltages, currents and temperatures

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSS}	drain leakage current	V_{DS} = 55 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	μA
		V_{DS} = 55 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	μA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = −20 V; T_j = 25 °C	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 175 °C;	-	-	27.6	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C;	-	8.2	12	mΩ

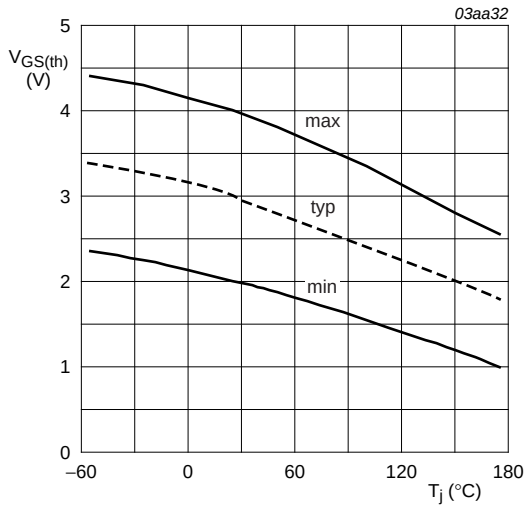
$V_{BR(DSS)}$ (drain-source breakdown voltage) - an expansion of the parameter listed and explained in Section 2.4. This section lists the maximum voltage the device is guaranteed to block between the drain and source terminals in the off-state over the entire MOSFET temperature range. The temperature range is from −55 °C to +175 °C. The current between the drain and the source terminals of the BUK7Y12-55B, is guaranteed to be below 250 μA for the voltage and temperature range. The range is 50 V or less if the device is cooler than +25 °C, and 55 V or below if the device is between +25 °C and +175 °C.

The effect of temperature on the off-state characteristics is twofold. The leakage current increases with temperature, turning the device on. Competing against the leakage current increase, the breakdown voltage also increases with temperature.

$V_{GS(th)}$ (gate-source threshold voltage) is important for determining the on-state and the off-state of the MOSFET. $V_{GS(th)}$ is defined where $V_{DS} = V_{GS}$, although it is sometimes quoted for a fixed V_{DS} (e.g. 10 V).

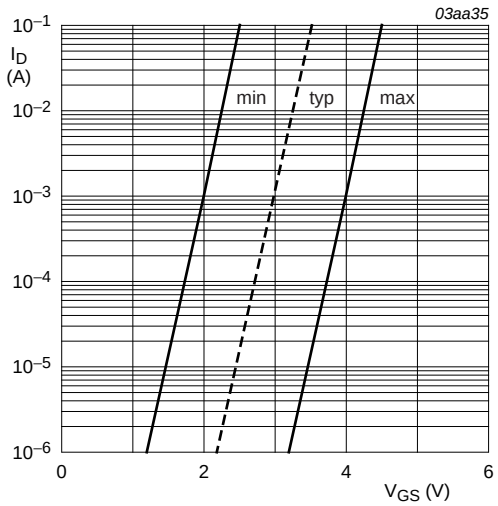
Note that the definition of the threshold voltage for a particular current where the gate and drain are shorted together, can differ from examples in textbooks. The parameter in textbooks describes a change in the physical state of the MOSFET and is independent of the MOSFET chip size. The parameter used in the data sheet is for a specified current and is dependent on the chip size, as the current flow is proportional to the chip area.

The threshold voltage in the data sheet is defined in a way that is best for routine measurement, but not how the actual device would typically be used. Consequently, the graphs provided in Figure 6 support the parameter.



Gate-source threshold voltage as a function of junction temperature

I_D = 1 mA; V_{DS} = V_{GS}



Subthreshold drain current as a function of gate-source voltage

T_j = 25 °C; V_{DS} = 5 V

Fig 6. Supporting figures for threshold voltage parameter

The first graph shows the variation in the threshold voltage for the typical and limit devices over the rated temperature range. All the MOSFETs are guaranteed to have a threshold voltage between the lines.

Consequently, for the BUK7Y12-55B at 25 °C, if V_{DS} and V_{GS} are both less than 2 V, all devices carry less than 1 mA. Also, all devices carry more than 1 mA if V_{DS} and V_{GS} are both greater than 4 V. At 175 °C, the lower limit has fallen to 1 V, while the upper limit has fallen to 2.5 V. The lower limit is usually more important as it determines when the device is guaranteed to be turned off, and what noise headroom an application needs.

The second graph shows how the device turns on around this threshold voltage. For the BUK7Y12-55B, the current increases 100,000 times for an increase in gate voltage of less than 1 V. An example is given for the situation when the drain-source voltage is fixed at 5 V.

I_{DSS} (drain leakage current) guarantees the maximum leakage current that the device passes at its maximum rated drain-source voltage during the off-state. It is important to note how much higher I_{DSS} is at high temperature, which is the worst case.

I_{GSS} (gate leakage current) guarantees the maximum leakage current through the gate of the MOSFET. The I_{GSS} is important when calculating how much current is required to keep the device turned on. Because it is a leakage current through an insulator, this current is independent of temperature, unlike I_{DSS}.

$R_{DS(on)}$ (drain-source on-state resistance) is one of the most important parameters. The previous parameters guarantee how the device functions when it is off, how it turns off and what leakage currents could be expected. These factors are important when battery capacity is an issue in the application.

$R_{DS(on)}$ is a measure of how good a closed-switch the MOSFET is, when turned-on. It is a key factor in determining the power loss and efficiency of a circuit containing a MOSFET. The on-resistance $R_{DS(on)} \times I_D^2$ gives the power dissipated in the MOSFET when it is turned **fully** on. Power MOSFETs are capable of carrying tens or hundreds of amps in the on-state.

Power dissipated in the MOSFET makes the die temperature rise above that of its mounting base. Also when the MOSFET die temperature increases, its $R_{DS(on)}$ increases proportionally. Maximum recommended junction temperature is 175 °C (for all NXP **packaged** MOSFETs).

Using the BUK7Y12-55B data sheet as an example:

$R_{th(j\text{-}mb)}$ temperature rise per Watt between junction (die) and mounting base = 1.42 K/W (1.42 °C/W).

Maximum power dissipation for temperature rise of 150 K (T_{mb} = 25 °C, T_j = 175 °C) = $^{150}/_{1.42}$ = 105.63 W.

Maximum $R_{DS(on)}$ at a die temperature (T_j) of 175 °C = 27.6 mΩ.

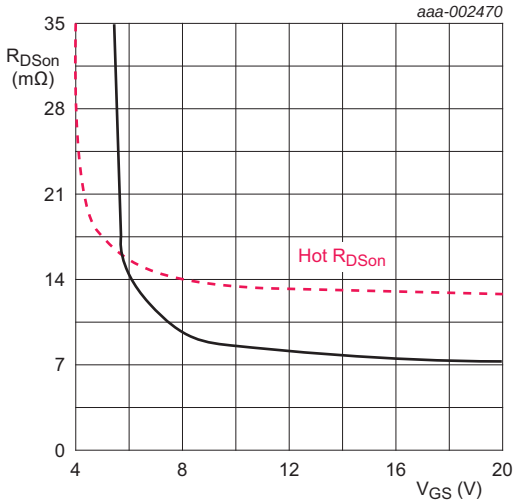
Therefore, at steady state with T_{mb} = 25 °C and T_j = 175 °C, P = 105.63 W = $I_{max}^2 \times R_{DS(on)(175\ °C)}$.

Therefore:

$$I_{max} = \sqrt{\frac{P_{(max)175°C}}{R_{DS(on)175°C}}} = \sqrt{\frac{105.63W}{0.0276\Omega}} \quad (5)$$

= 61.86 A (rounded down to 61.8 A in the data sheet).

The $R_{DS(on)}$ of the MOSFET depends on gate-source voltage, and there is a lower value below which it rises very sharply. The ratio of the $R_{DS(on)}$ increase over temperature is different for different gate drives. The red dashed line in Figure 7 shows the curve for a higher temperature and demonstrates the differences.

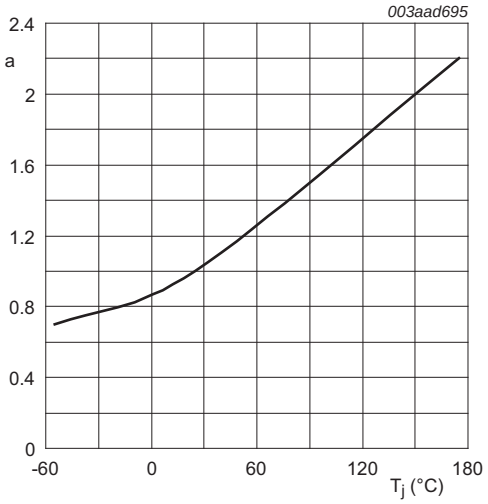


This diagram is for illustrative purposes only and not to be taken as an indication of hot R_{dson} performance for any device

Fig 7. Drain-source on-state resistance as a function of gate-source voltage at 25 °C and high temperature

If an application requires good $R_{DS(on)}$ performance for lower gate-source voltages, then MOSFETs are made with lower threshold voltages, e.g. the BUK9Y12-55B. However, the lower threshold voltage of such a device means that it has a lower headroom for its off-state at high temperature. This lower headroom often means that a device with a higher threshold voltage is needed.

A typical curve showing how resistance increases with temperature is shown in Figure 8.



$$a = \frac{R_{DS(on)}}{R_{DS(on)25\ °C}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature

2.6.2 Dynamic characteristics

The dynamic characteristics determine the switching performance of the device. Several of these parameters are highly dependent on the measurement conditions. Consequently, understand the dynamic characteristics before comparing data sheets from suppliers with different standard conditions. Table 6 is a sample dynamic characteristics table.

Table 6. Dynamic characteristics

List of constants and limitations relating to the table i.e. voltages, currents and temperatures

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 44 V; V_{GS} = 10 V	-	35.2	-	nC
Q_{GS}	gate source charge		-	9.24	-	nC
Q_{GD}	gate drain charge		-	14.8	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	1550	2067	pF
C_{oss}	output capacitance		-	328	394	pF
C_{rss}	reverse transfer capacitance		-	153	210	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; V_{GS} = 10 V; R_L = 1.5 Ω; $R_{G(ext)}$ = 10 Ω	-	19.3	-	ns
t_r	rise time		-	29.4	-	ns
$t_{d(off)}$	turn-off delay time		-	43.2	-	ns
t_f	fall time		-	22	-	ns

2.6.2.1 Gate charge

$Q_{G(tot)}$, Q_{GS}, and Q_{GD} are all parameters from the same gate charge curve. They describe how much gate charge the MOSFET requires to switch, for certain conditions. This is particularly important in high frequency switching applications. Much of the power loss occurs during switching, when there are significant voltage and current changes simultaneously between the drain, gate and source. In the blocking state, there are significant voltages but negligible currents. In the full-on state, there are significant currents and small voltages.

The gate charge parameters are dependent on the threshold voltage and the switching dynamics as well as the load that is being switched. There is a difference between a resistive load and an inductive load.

An example of a gate charge curve is shown in Figure 9:

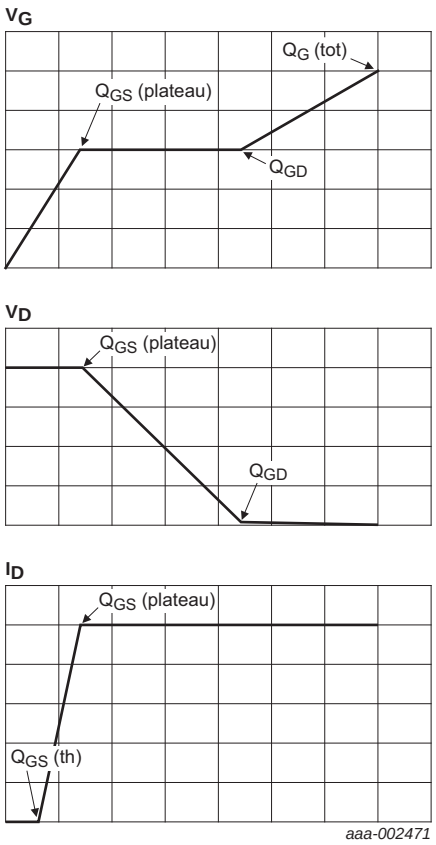


Fig 9. Gate charge curve also showing drain-source currents and voltages

Because the capacitance varies with voltage and current, it is better to look at the gate charge data than the capacitance data when determining switching performance. This is especially true if the gate-driver circuit for the MOSFET is limited to a particular current, and a rapid switch is required.

The gate charge curve describes what happens to a MOSFET which has a drain supply limited to a particular current and voltage. The operation of the test circuit means that during the gate charge curve, the MOSFET is provided with either a constant voltage or a constant current.

During this time, the drain-source voltage begins to fall because the increased charge on the MOSFET allows easier conduction. Consequently, although the gate-source voltage is constant, the drain-gate voltage is falling.

Eventually the capacitance stops increasing and any further increases in gate charge increase the gate-source voltage. This characteristic is sometimes referred to as the "Miller plateau" as it refers to the time during which the so-called Miller capacitance increases. The Miller plateau is also known as the gate-drain charge (Q_{GD}).

During this period, there are significant currents and voltages between the drain and source, so Q_{GD} is important when determining switching losses.

Once the end of the Miller plateau is reached, the gate-source voltage increases again, but with a larger capacitance than before Q_{GS} had been reached. The gradient of the gate charge curve is less above the Miller plateau.

The gate-charge parameters are highly dependent on the measurement conditions. Different suppliers often quote their gate-charge parameters for different conditions, demanding care when comparing gate charge parameters from different sources.

Higher currents lead to higher values of gate-source charge because the plateau voltage is also higher. Higher drain-source voltages, lead to higher values of gate-drain charge and total gate charge, as the plateau increases.

The drain-source currents and voltages during the gate charge switching period are shown in Figure 10

If the MOSFET starts in the off state (V_{GS} = 0 V), an increase in charge on the gate initially leads to an increase in the gate-source voltage. In this mode, a constant voltage (V_{DS}) is supplied between the source and drain.

When the gate-source voltage reaches the threshold voltage for the limiting current at that drain-source voltage, the capacitance of the MOSFET increases and the gate-voltage stays constant. This is known as the plateau voltage and the onset charge is referred to as Q_{GS}. The higher the current is, the higher the plateau voltage (see Figure 10).

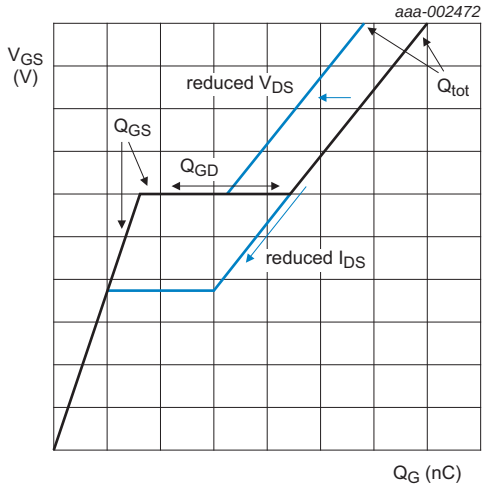


Fig 10. Features of gate charge curve

2.6.2.2 Capacitances

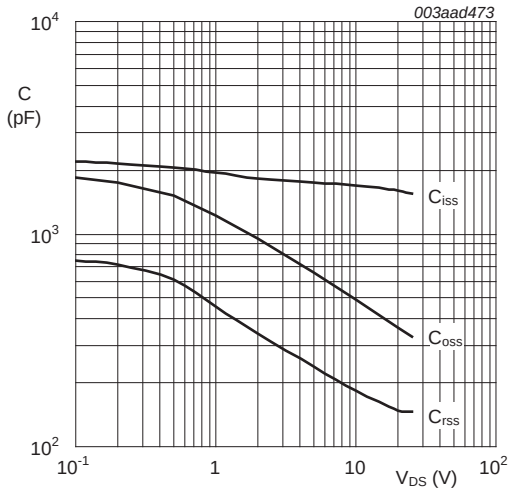
Capacitance characteristics are generally less useful than the gate charge parameters, for the reasons already discussed. However, they are still listed on data sheets. The three capacitances that are normally listed are as follows:

- **C_{ISS}** (input capacitance) is the capacitance between the gate and the other two terminals (source and drain).
- **C_{OSS}** (output capacitance) is the capacitance between the drain and the other two terminals (gate and source).

- C_{RSS} (reverse transfer capacitance) is the capacitance between the drain and the gate.

Semiconductor capacitances generally depend on both voltage and the frequency of the capacitance measurement. Although it is difficult to compare capacitances measured under different conditions, many suppliers specify a measurement frequency of 1 MHz. Consequently, the capacitances vary with drain-source voltage (see Figure 11). However, the capacitances also vary with gate-source voltage, which is why the gradients in the gate-charge curve vary for different voltages (see Figure 9).

The relationship between charge, voltage and capacitance in the gate charge curve is $\Delta Q = \Delta C \times \Delta V$. For different gradients at different gate voltages, the capacitance changes significantly with gate-source voltage.



V_{GS} = 0 V; f = 1 MHz

Fig 11. Capacitances as a function of drain source voltage

2.6.2.3 Switching times

Most manufacturers quote resistive load switching times. However, extreme care is needed when comparing data from different manufacturers, as they are highly dependent on the resistance of the gate drive circuit used for the test. In devices for fast switching applications, the gate resistance of the MOSFET is often quoted as capacitive time constants which are equally dependent on resistance and capacitance.

2.6.3 Diode characteristics

The diode characteristics are important if the MOSFET is being used in the so-called "third quadrant". The third quadrant is a typical arrangement where the MOSFET replaces a diode to reduce the voltage drop from the inherent diode forward voltage drop. In such a situation, there is always a small time period when the MOSFET parasitic diode is conducting before the MOSFET turns on. For such applications, the diode switching parameters are important. In addition, diode reverse recovery contributes to the power losses as well as oscillation, which can cause EMC concern.

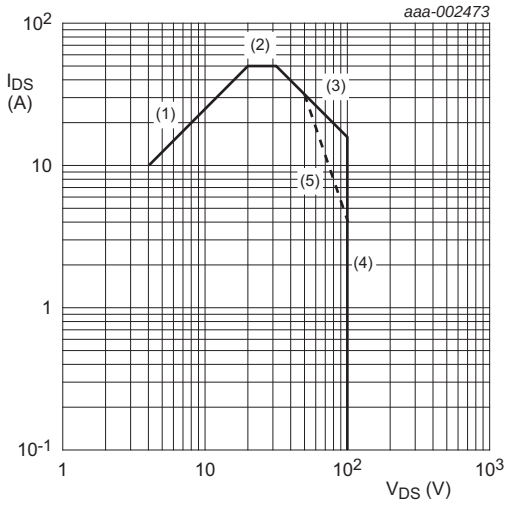
2.7 Package outline

This section describes the package outline dimensions and tolerances.

3. Appendices

3.1 Safe Operating Area (SOA) curves

To highlight the key features, Figure 12 provides an idealized SOA curve for a hypothetical MOSFET. Data for a hypothetical MOSFET for a single pulse length, is shown to highlight the region where it deviates from the ideal curve.



(1) $R_{DS(on)}$ limit (V_{DS}/I_{DS} is constant)

(2) Maximum pulsed drain current (I_{DS} is constant)

(3) Maximum pulsed power dissipation ($V_{DS} \times I_{DS}$ is constant)

(4) Maximum allowed voltage (V_{DS} is constant)

(5) Linear mode derating - a departure from the ideal behavior shown in (3) due to operation within a regime of positive feedback, and potential thermal runaway

Fig 12. Idealized SOA curve at a single time pulse for hypothetical MOSFET

The dashed line (5) is to emphasize where the curve deviates from the ideal. In reality, there is a single curve with a change of gradient where the linear mode derating becomes important.

$R_{DS(on)}$ limit

$R_{DS(on)}$ is region (1) of the graph and Equation 6 represents the limiting line:

$$\frac{V_{DS}}{I_{DS}} \leq R_{DS(on)}\ (175\ ^{\circ}C) \tag{6}$$

The limit is when the MOSFET is fully on and acting as a closed switch with a resistance that is no greater than the hot $R_{DS(on)}$.

Constant current region

The constant current region is region (2) of the graph. It is the maximum pulsed drain current, which is limited by the device manufacturer (for example, the wire-bonds within the package).

Maximum power dissipation (linear mode) limit

In this region, the MOSFET is acting as a (gate) voltage-controlled current source. This means that there are significant voltages and currents applied simultaneously, leading to significant power dissipation. Line (3) shows the idealized curve, whereas the dotted line (5) shows where it deviates from the ideal.

The limiting factor for the SOA curve in region (5), is the heating applied during a rectangular current and voltage pulse. Even in the ideal situation, this curve depends on the transient thermal impedance of the MOSFET, which is covered in Section 2.5.

The transient thermal impedance varies with the pulse length. This is due to the different materials in the MOSFET having different thermal resistances and capacities. The differences create a thermal equivalent to an RC network from the junction (where the heat is generated) to the mounting base. Equation 7 is the calculation used to determine the ideal curve in this region.

$$P = I_D \times V_{DS} = \frac{T_{j(max))} - T_{mb}}{Z_{th(j\text{-}mb)}} = Constant \quad (7)$$

The ideal situation accurately describes the situation for sufficiently high current densities. However, it is overly optimistic for low current-densities, i.e. towards the bottom right of region (3). Low current densities and high voltages can lead to thermal runaway in the linear mode operation. Thermal runaway is discussed in the following section.

Thermal runaway in linear mode

Power MOSFETs are often considered to be immune to thermal runaway due to the temperature coefficient of resistance, which means that as temperature rises, current falls.

This is only true for MOSFETs that are fully on (i.e. in region 1), but it is not the whole story.

When a MOSFET is turned on, there are two competing effects that determine how its current behaves with increasing temperature. As the temperature rises, the threshold voltage falls. The MOSFET is effectively turned on more strongly, thereby increasing the current. In opposition, the resistance of the silicon increases with increasing temperature, thereby reducing the current. The resultant effect for a constant drain-source voltage, is shown in Figure 13. This situation occurs when the gate-source voltage of a MOSFET is being used to control the current, or when the MOSFET is switched sufficiently slowly.

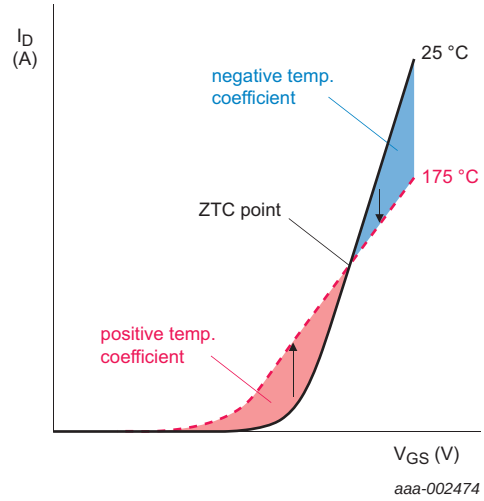


Fig 13. Transfer characteristics for a hypothetical MOSFET, showing regions of positive and negative temperature coefficient

The resistance increase dominates at high currents, meaning that localized heating leads to lower currents. The threshold-voltage drop dominates at low currents, meaning that localized heating lowers the threshold voltage. This condition effectively turns on the device more, leading to higher currents and a risk of thermal runaway.

Consequently, for a given V_{DS}, there is a critical current below which there is a positive-feedback regime and a subsequent risk of thermal runaway. Above this critical current, there is negative feedback and thermal stability. This critical current is known as the Zero Temperature Coefficient (ZTC) point.

This effect reduces the SOA performance for low currents and high drain-source voltages. The constant power line must be reduced as shown in region (5). For short switching events, this effect is insignificant. However, as the duration of the switching event becomes longer, for example to reduce electromagnetic interference, the effect becomes more important and potentially hazardous.

Voltage-limited region

The device is limited by its breakdown voltage V_{DS} which is shown in region (4). The quick reference data provides values for V_{DS} at temperatures of 25 °C and above. In the hypothetical MOSFET shown in Figure 13, the rating is 100 V. For the BUK7Y12-55B, the voltage is 55 V.

3.1.1 Safe operating area for temperatures above 25 °C

When taking measurements from the SOA curve there are two main assumptions:

1. Operation temperature of 25 °C
2. It is a rectangular pulse

However, some pulses are not rectangular and do not occur at 25 °C. For these instances, the use of Equation 8 can be used.

$$T_{j(rise)\max} = T_{j(max)} - T_{j(amb)} = \frac{2}{3} P_{av} \cdot Z_{th\left(\frac{t_{av}}{2}\right)} \quad (8)$$

Where $T_{j(max)}$ is the maximum die temperature of 175 °C and $T_{j(amb)}$ is the ambient temperature of the system. For example, in automotive applications, the two main ambient temperatures used are 85 °C for in-cabin (inside the driver compartment) and 105 °C for under the hood (near and around the engine).

It is worth noting that using the ambient temperature in calculations for worst case analysis, can be misleading. It is misleading because the temperature of the MOSFET mounting base before it is switched on can be higher. For example, a design has 10 MOSFETs and 9 are powered. The mounting base temperature of the 10th MOSFET (which is off) is likely to be similar to that of the other 9 MOSFETs that are ON. So if the ambient is 105 °C, and the mounting base temperature of the 9 MOSFETs that are ON is 125 °C, $T_{j(amb)}$ of the 10th MOSFET is 125 °C and not 105 °C. Calculations under these conditions are conservative and are more suitable for worst case analysis (Equation 9).

$$T_{j(rise)\max} = T_{j(max)} - T_{j(amb)} = P_{av} \cdot Z_{th(t_{av})} \quad (9)$$

Note: Use $R_{th(j\text{-}mb)}$ instead of $Z_{th(j\text{-}mb)}$ in a DC application (not pulsed). Above approximately 100 ms, Z_{th} is indistinguishable from R_{th}.

3.1.1.1 Example calculations

Calculate the max DC I_{DS} for a BUK9277-55A, with V_{DS} = 40 V at 25 °C

Rewrite Equation 10 to bring out I_{DS} as the main subject (P_{av} is the average power, and is $I_{DS} \times V_{DS}$ for the DC situation). As it is a DC situation, replace Z_{th} with R_{th}.

$$T_{j(rise)} = I_{DS} \times V_{DS} \times Z_{th(av)} \quad (10)$$

$$\frac{T_{j(rise)}}{V_{DS} \times R_{th}} = I_{DS} \quad (11)$$

$$\frac{175\ °C - 25\ °C}{40\ \text{V} \times 2.93\ K/W} = 1.28\ \text{A} \quad (12)$$

Therefore, the maximum DC current rating for these conditions is 1.28 A.

3.1.2 Example using the SOA curve and thermal characteristics

Consider the following application during linear mode operation:

- Device BUK7Y12-55B, square current pulses of the following:
  - I_{pulse} = 20 A
  - V_{pulse} = 40 V
  - f = 2 kHz
  - t_{pulse} = 100 µs
  - T_{amb} = 25 °C

3.1.2.1 Calculation steps

The SOA curve is initially checked to see whether any single pulse would cause a problem. Observing the SOA curve, it can be seen that the 20 A, 40 V pulse lies between the 100 μs and 1 ms lines. This indicates that the pulse lies within acceptable limits.

The duty cycle for the pulses is now calculated using a frequency of 2 kHz for 100 μs pulses. These values give a duty cycle of 0.2. The SOA curve demonstrates that for 100 μs, the line with the duty cycle (δ) has a transient thermal impedance of 0.4 K/W.

The power dissipation for the square pulse is 20 A × 40 V, which equals 800 W.

Using Equation 8, the temperature rise for the 100 μs pulse is calculated as being 800 W × 0.4 K/W, which equals 320 K. With a starting temperature of 25 °C, the temperature rise results in a finishing temperature of 345 °C. As the MOSFET junction temperature must not exceed 175 °C, the MOSFET is not suitable for this application.

If the application requires a single pulse, then the curve shows that the transient thermal impedance for a 100 μs pulse is 0.1 K/W. As a result, the temperature rise is 800 W × 0.1 K/W which equals 80 K. The finishing temperature is then 105 °C for a starting temperature of 25 °C. The device is able to withstand this, thereby confirming what the SOA curve already indicated.

3.1.2.2 Derating for higher starting temperatures

The example Safe Operating Area calculations were performed for a mounting base temperature of 25 °C. At higher mounting base temperatures, the SOA curves must be derated, as the allowed temperature rise is reduced. The allowed power of the pulse is reduced proportionally to the reduced temperature rise. For example, with a mounting base temperature of 25 °C, the allowed temperature rise is 150 °C. At 100 °C, the allowed temperature rise is half of that (75 °C). The allowed power is half of that allowed at 25 °C.

Because of the effects of linear-mode operation, the current is maintained but the allowed drain-source voltage is derated.

The 100 °C derating for the BUK7Y12-55B is shown in Figure 14.

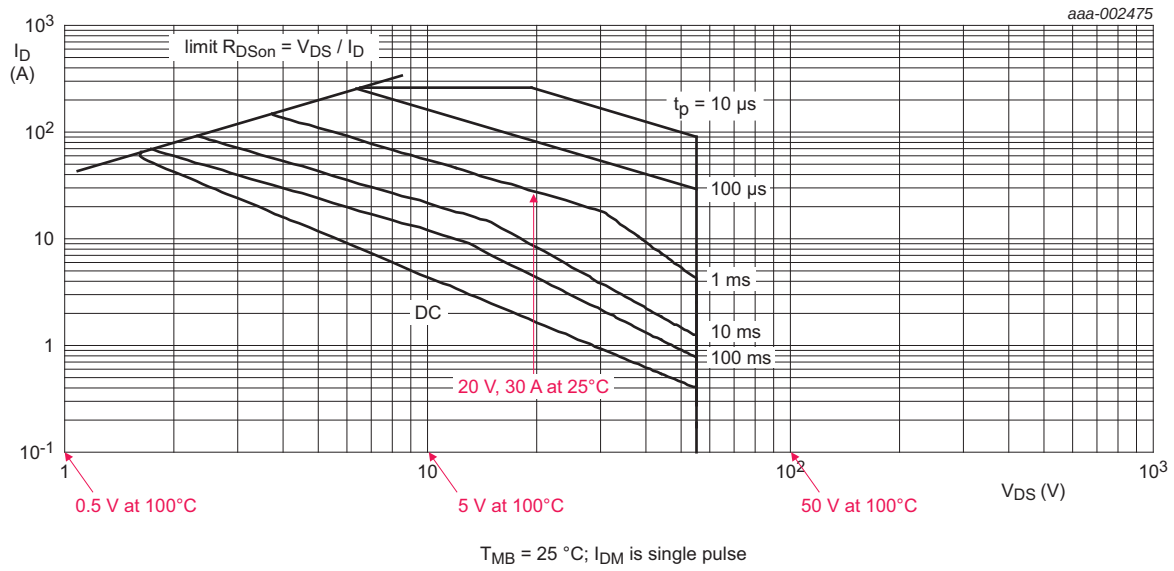


Fig 14. SOA curve showing derating for 100 °C

Example:

Is a 1 ms pulse of 30 A and 15 V allowed at 100 °C for the BUK7Y12-55B?

At 25 °C, it can be seen that a V_{DS} of 20 V is allowed for 30 A, and 1 ms. Therefore, at 100 °C, a V_{DS} of 10 V is allowed.

A 1 ms pulse of 30 A and 15 V at 100 °C is outside the permitted safe operating area and is consequently not allowed.

4. References

[1] The Impact of Trench Depth on the Reliability of Repetitively Avalanched Low-Voltage Discrete Power Trench nMOSFETs - Alatise et al, IEE Electron Device Letters, Volume 31, No7, July 2010, pages 713-715.

[2] Semiconductor Devices - Physics and Technology S.M.Sze, 1985, John Wiley & Sons.

[3] Application Note AN10273 - Power MOSFET single-shot and repetitive avalanche ruggedness rating.

[4] Application Note AN10874 - LFPAK MOSFET thermal design guide.

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Date of release: 7 January 2013
Document identifier: AN11158