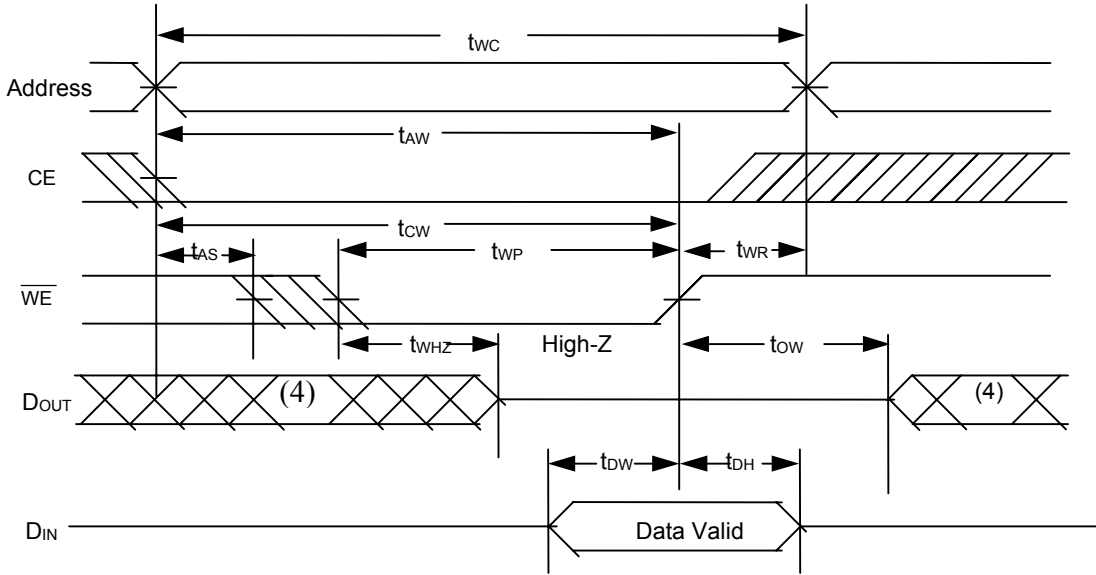
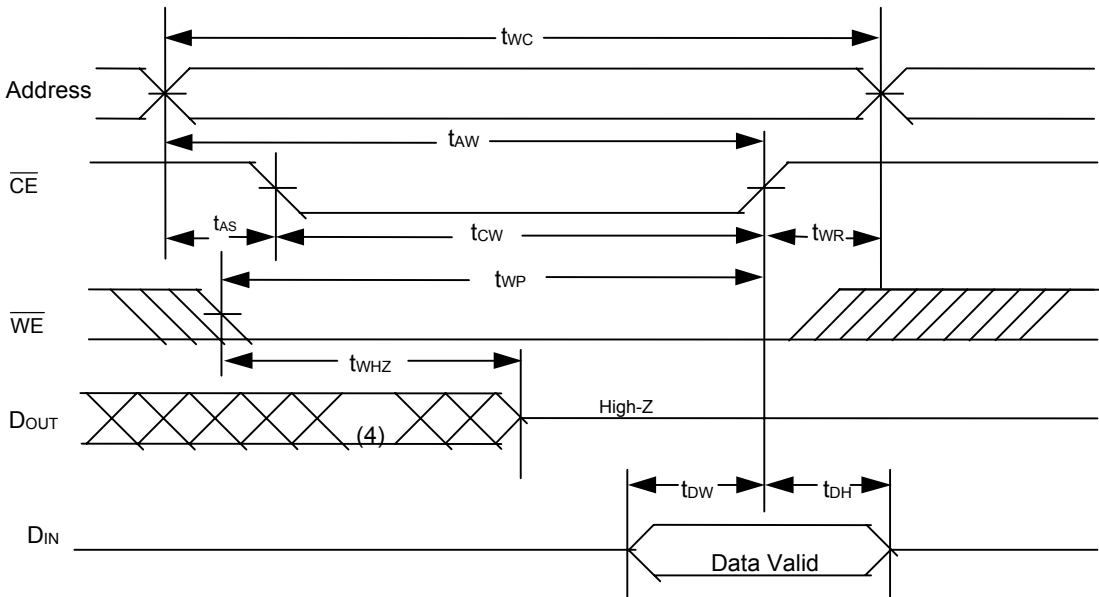




**WRITE CYCLE 1 ( $\overline{WE}$  Controlled) (1,2,3,5)**



**WRITE CYCLE 2 ( $\overline{CE}$  Controlled) (1,2,5)**



Notes :

1.  $\overline{WE}$  or  $\overline{CE}$  must be HIGH during all address transitions.
2. A write occurs during the overlap of a low  $\overline{CE}$  and a low  $\overline{WE}$ .
3. During a  $\overline{WE}$  controlled with write cycle with  $\overline{OE}$  LOW,  $t_{wp}$  must be greater than  $t_{whz} + t_{dw}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after  $\overline{WE}$  LOW transition, the outputs remain in a high impedance state.
6.  $t_{ow}$  and  $t_{whz}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.