CAPACITANCE (TA=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF, I_{OH}/I_{OL} = -4mA/8mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, TA = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT61256-8		UT61256-10		UT61256-12		UT61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ*}	2	-	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ*}	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns

(2) WRITE CYCLE

PARAMETER	SYMBOL	UT61256-8		UT61256-10		UT61256-12		UT61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	6.5	-	8	-	12	-	15	-	ns
Chip Enable to End of Write	t_{CW}	6.5	-	8	-	12	-	15	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	6.5	-	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	1.5	-	2	-	3	-	4	-	ns
Write to Output in High Z	t_{WHZ*}	-	5	-	6	-	7	-	8	ns

*These parameters are guaranteed by device characterization, but not production tested.