fbas_enc: FBAS(CVBS) encoder for PAL and/or NTSC

V0.21 (c) 2007 Jörg Wolfram

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2 History and features

After some projects of rgb colour video output with AVR microcontrollers there was the question about FBAS (cvbs) signal generation on a simple and easy way. For example, to be able to feed a modulated HF signal into an aerial arrangement.
Because a microcontroller is rather inexpedient for it on account of the necessary processing speed, the decision fell in favour of a CPLD. Of course there is for such things also Spezial-IC's, but I did not want to choose this way. As result there is a simple design which also fits in a XC9536 of Xilinx. The Encoder can be also integrated into other designs, provided, the regulations of the LGPL are kept.

- the colour carrier frequency is generated from the system clock of 16 or 20 MHz
- inputs: hsync, vsync and rgb
- outputs: five resistors drive the 75 ohm load (which is located in the TV)
- 8 basic colours / 8 grey steps eligible
- the same hardware can be used for PAL and NTSC

3 A little bit of theory

There are many usefull addresses on the Internet and so I only want to tell briefly the most important to know about the PAL system. Horizontal timing and vertical timing are identical to the black and white BAS signal as much as possible. The main difference is the colour carrier signal which is used to encode the additional information. To avoid moires on black'n white pattern the colour carrier has a crooked frequency. Namely the horizontal frequency of 15,625 hertz * 283.75 plus the half vertical frequency (25 hertz). With it one comes on 4,433,618.75 hertz. To generate this we can use a quartz oscillator or find a way to use the system clock from teh rgb source (e.g. microcontroller). This can be done by using DDS (Direct Digitally Synthesis) and a error of just abovementioned 25 hertz must be accepted, otherwise we need very wide counters to the signal production. With a clock frequency of 16 MHz we need such a counter (accumulator register) with 12-bit width. Every clock the counter adds 1135 (283.75 * 4) and so we get the (approximate) value of the colour carrier. With 20 MHz clock speed this would be theoretical 908, a 10-bit-wide counter should be also enough with addition of 227.

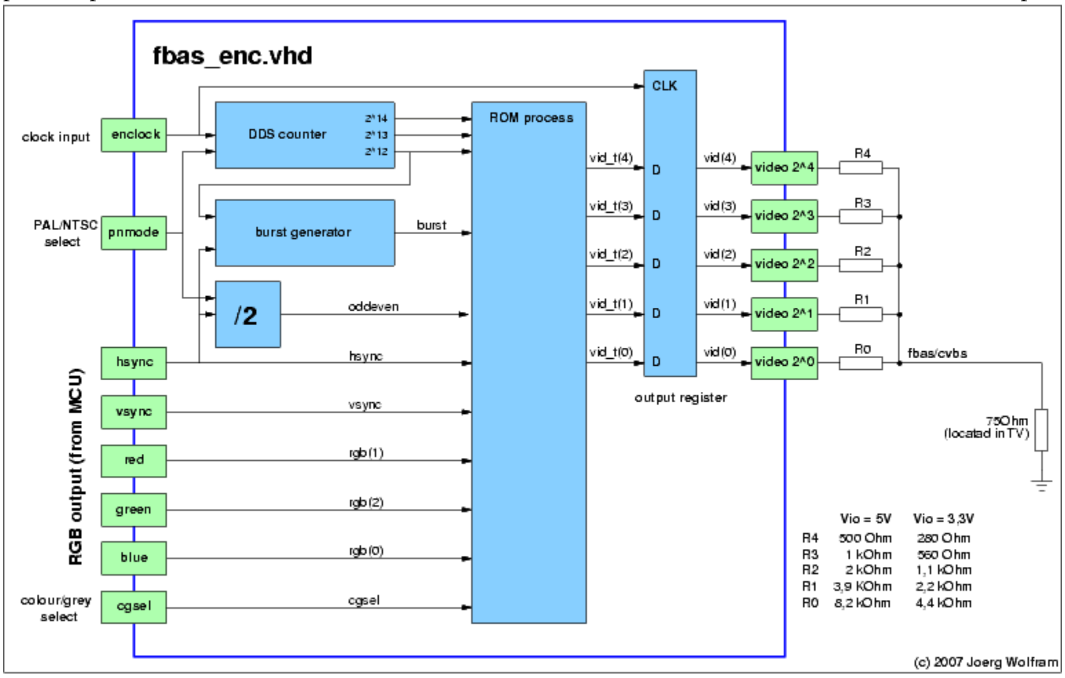
To identify a colour signal and to synchronise the quartz oscillator in the TV, the normally quadrature-modulated colour carrier will be sent unmodulated shortly after the synchronous impulse for approx. 10 periods. This is named as the **burst**. If burst is sent the phase changes from line to line between -135 and +135 degrees. However, after my experiences 8 periods are also sufficient. The amplitude of the Bursts amounts to 0,15V exactly 50of the maximum amplitude with maximum colour saturation. For the basic colours a saturation of about 50completely sufficient but its also possible to create a table with another saturation. The FBAS (CVBS) signal consists of three signals:

- the luminance signal Y = 0,299*R + 0,587*G + 0,114*B
- the U colour signal U = 0,493 * (B-Y)
- the V colour signal U = 0,877 * (R-Y)

The Y signal will transfer directly, the U and V signals modulates the colour carrier by quadrature-modulation. In brief the U signal is multiplied by the cosinus wave of the colour carrier and the V signal with about 0 or 180 degrees of the sinus wave of the colour carrier. Besides, the tone is encoded in the phase and the colour saturation in the amplitude of the modulated colour carrier. In the last stage the three signals will be added and during the synchronous impulses it must be set to 0 V.

4 Realisation

And now te big question, how can we fit these functions in a small CPLD. The colour carrier and the Burst signal do the least problems, the modulation and mixture with the Y signal is less trivial. With the first attempts appeared that it is possible theoretically to generate a FBAS signal, while rebuild the signal path digitally. But, the logic expenditure is rather high. The main idea behind this project is to use a table with precalculated video amplitudes. And so I've written a perl script to create the whole VHDL code of the encoder module. If there is interest, i can also publish this tool.



The encoder module exists in two variants one for 16 and one for 20 MHz. It uses the following signals:

- **enclock** the main encoder clock
- **hsync** the horizontal sync pulse
- **vsync** the vertical sync pulse
- **rgb(2 downto 0)** the green(2),red(1) and blue(0) signal
- **cgsel** color/grey select
- **pnmode** pal/ntsc select
- **vid(4 downto 0)** video signal output

The cgsel signal can used as an fourth bit to select one of 8 grey levels or with an external switch. '0' selects colour mode and '1' selects greylevel mode. With the pnmode signal it is possible to switch between PAL ('0') and NTSC ('1') without any hardware changes. If only PAL or NTSC is needed, feeding this signal with statically '0' or '1' results in decreasing the amount of logic cells. In the examples I use this to fit the design in a XC9536 CPLD. To use only one design for PAL and NTSC, it uses a 15-bit counter for DDS. In some cases (only PAL mode) some low significant bits not used and will be eliminated by the synthesis tool.

5 Result

The design written in VHDL fits in a XC9536 CPLD. Unfortunately, on some TV devices and on different colours a light, quickly walking pattern is visible whose cause I could exactly determine not yet. It can lie with the relation of colour carrier to the horizontal frequency or also with the Experimentierboard construction. In connection with an AVR microcontroller this design was developed for, the internal quartz oscillator was not really useable. An external quartz oscillator makes sense anyway.

6 Changelog

17.2.2007 the first public version (0.21)

- PAL and version NTSC for 16, 20, 32 and 40 MHz clock frequency