HD61104,HD61104A
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

HD61104, HD61104A is a column (segment) driver for large-area dot matrix liquid crystal graphic display systems.

Features

- Display duty cycle: 1/64–1/200
- Internal liquid crystal display driver: 80 drivers
- 4-bit bus, bidirectional shift data transfer
- Cascade connection with enable format
- Data transfer rate: 3.5 MHz
- Power supply for logic circuit: 5 V ±10%
- Power supply for LCD drive circuits :
  10 to 26 V (HD61104)
  10 to 28 V (HD61104A)
- Standby function
- CMOS process
- 100-pin flat plastic package

Ordering Information

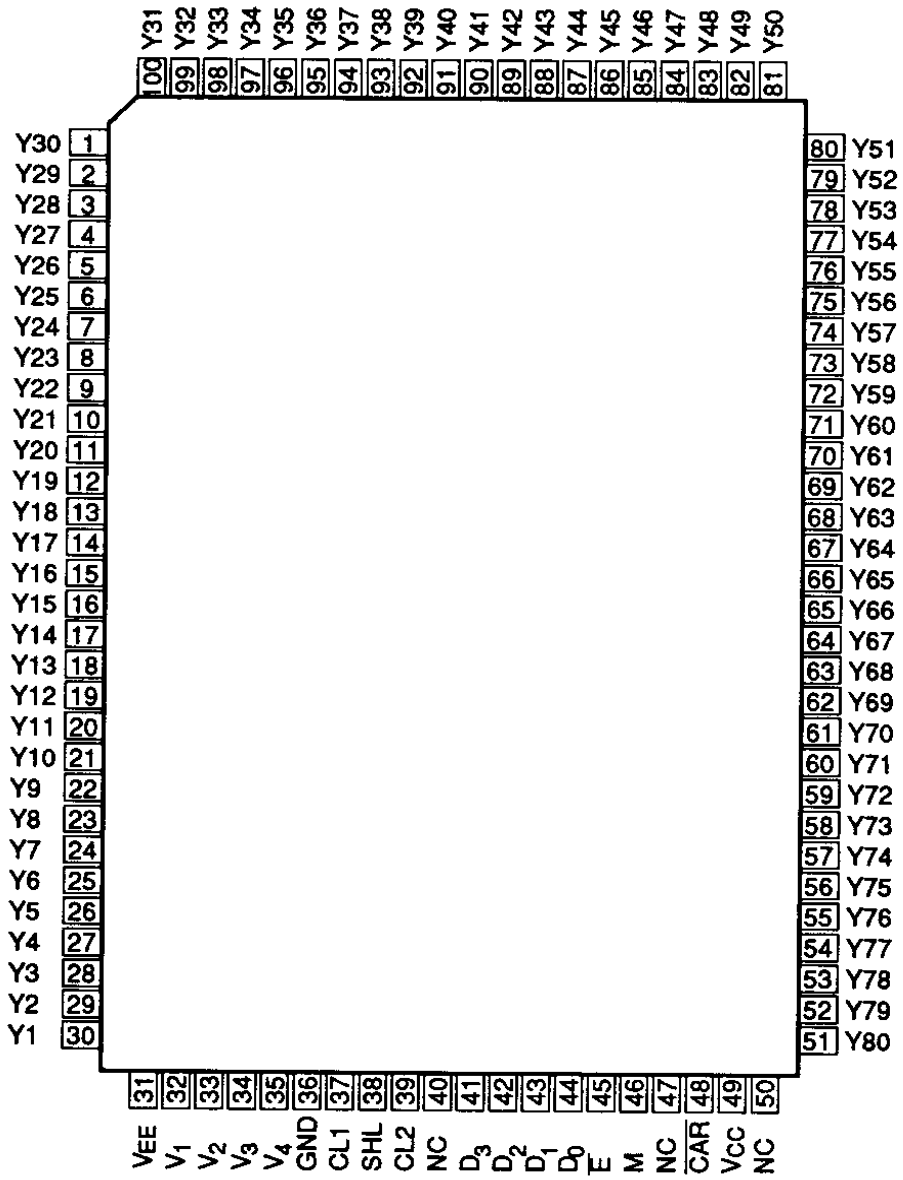
Type No.	LCD Driving Level (V)	Package
HD61104	+10 to +26	100 pin plastic QFP (FP-100)
HD61104A	+10 to +28V	
HD61104TF	+10 to +28V	100 pin plastic T-QFP (TFP-100)

Absolute Maximum Ratings

Item		Symbol	Value	Unit	Note
Supply voltage (1)		V_{CC}	–0.3 to +7.0	V	2
Supply voltage (2)	HD61104	V_{EE}	V_{CC} – 28.0 to V_{CC} + 0.3	V	
	HD61104A	V_{EE}	V_{CC} – 28.5 to V_{CC} + 0.3		
Terminal voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)		V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

Notes:
1. LSIs may be permanently destroyed if used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to input terminals, SHL, CL1, CL2, D_0–D_3, $\overline{E}$, and M.
4. Applies to V_1, V_2, V_3, and V_4. Must maintain
   $V_{CC} \geq V_1 \geq V_3 \geq V_4 \geq V_2 \geq V_{EE}$
   Connect a protection resister of 15 Ω ± 10% to each terminal in series.

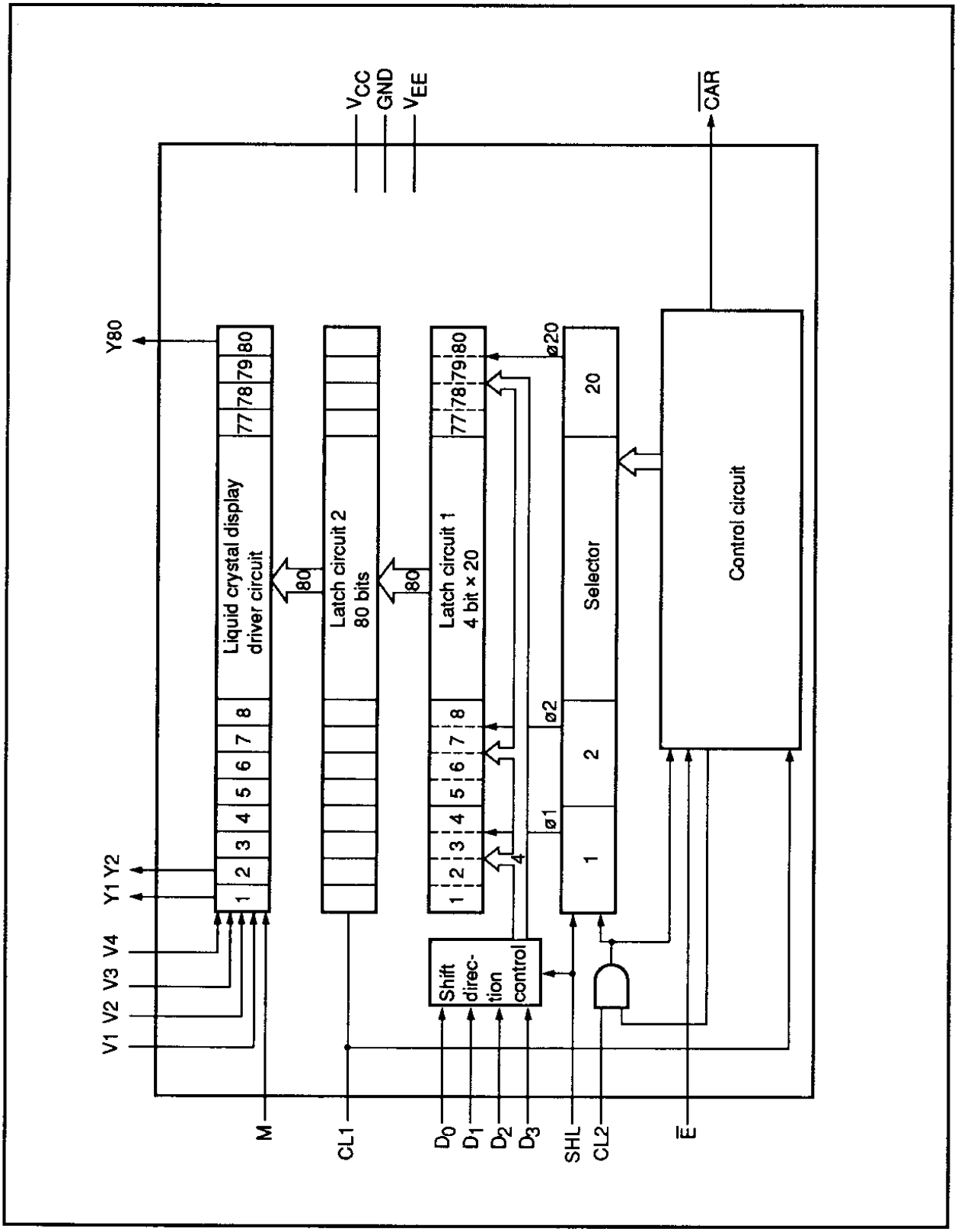
Pin Arrangement



(Top View)

(FP–100/TFP–100)

Block Diagram



Electrical Characteristics

DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 26 V (HD61104), V_{CC} – V_{EE} = 10 to 28 V (HD61104A), Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$0.7 \times V_{CC}$		V_{CC}	V		1
Input low voltage	V_{IL}	0		$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	$V_{CC} - 0.4$			V	$I_{OH} = -400$ µA	2
Output low voltage	V_{OL}			0.4	V	$I_{OL} = 400$ µA	2
Driver on resistance	R_{ON}			7.5	kΩ	$V_{EE} = -1$ 0V,Load current =100 µA	5
Input leakage current	I_{IL1}	–1		1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	–25		25	µA	$V_{IN} = V_{EE}$ to V_{CC}	3
Dissipation current (1)	I_{GND}			2.0	mA		4
Dissipation current (2)	I_{EE}			0.2	mA	HD61104	4
				0.4		HD61104A	
Dissipation current (3)	I_{ST}			100	µA		4 5

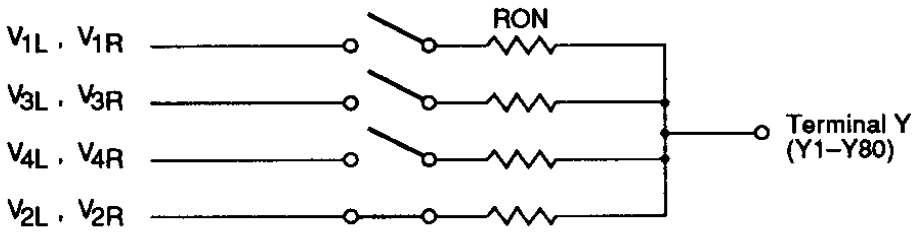
Notes:
1. Applies to CL1, CL2, SHL, E, M, and D_0-D_3.
2. Applies to $\overline{CAR}$.
3. Applies to V_1, V_2, V_3, and V_4.
4. Specified when display data is transferred under following conditions:
   - CL2 frequency fcp2 = 2.5 MHz (data transfer rate)
   - CL1 frequency fcp1 = 14.0 kHz (data latch frequency)
   - M frequency f_M = 35 Hz (frame frequency/2)
   - Display duty ratio 1/200

   Specified when $V_{IH} = V_{CC}$, V_{IL} = GND and no load on outputs.
   - I_{GND}: currents between V_{CC} and GND
   - I_{EE}: currents between V_{CC} and V_{EE}
5. Currents between V_{CC} and GND at standby ($\overline{E}$ input = high).
6. Resistance between terminal Y (one of Y1 to Y80) and terminal V (one of V_1, V_2, V_3, and V_4) when load current flows through one of the terminals Y1 to Y80. This value is specified under the following conditions:

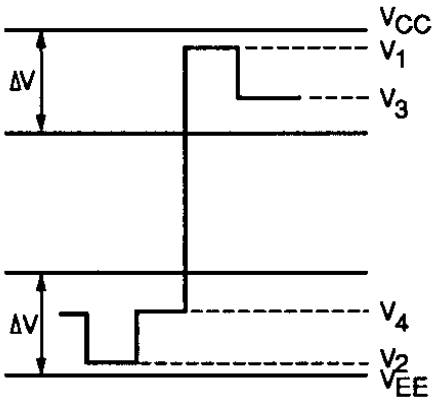
$V_{CC} - V_{EE} = 26$ V

$V_1, V_3 = V_{CC} - 2/10\ (V_{CC} - V_{EE})$

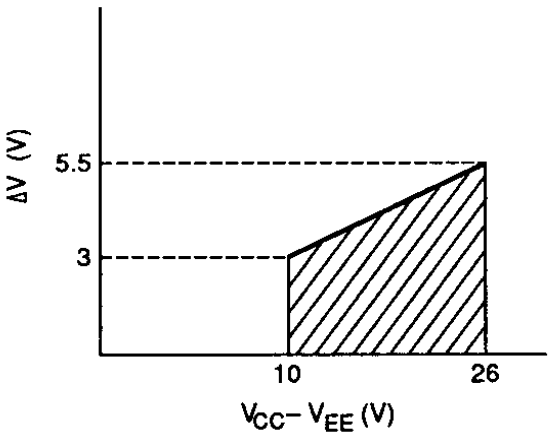
$V_2, V_4 = V_{EE} + 2/10\ (V_{CC} - V_{EE})$



The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V_1 and V_3, and negative voltage to V_2 and V_4, within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

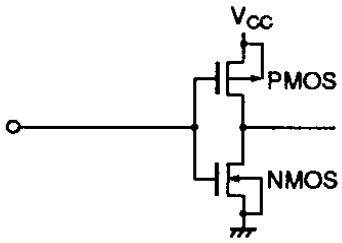


Correlation between Power Supply Voltage $V_{CC} - V_{EE}$ and ΔV

Terminal Configuration

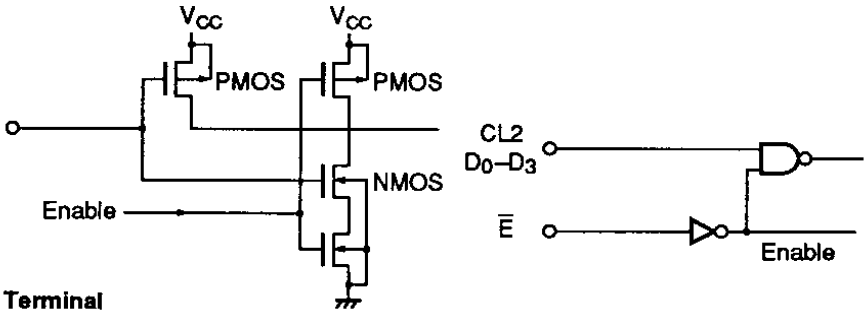
Input Terminal

Applicable Terminals : CL1, SHL, $\overline{E}$, M



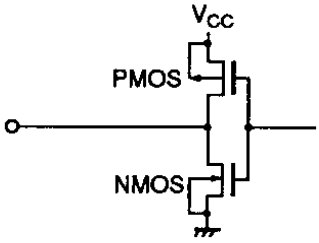
Input Terminal (controlled by Enable signal)

Applicable Terminals : CL2, D_0–D_3



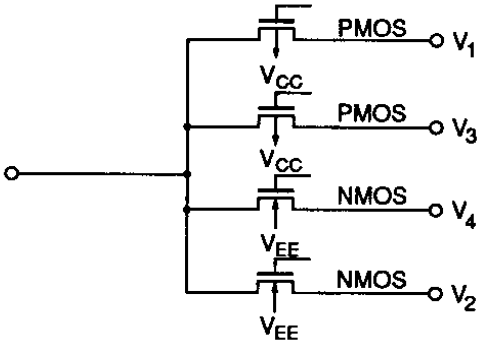
Output Terminal

Applicable Terminal : $\overline{CAR}$



Output Terminal

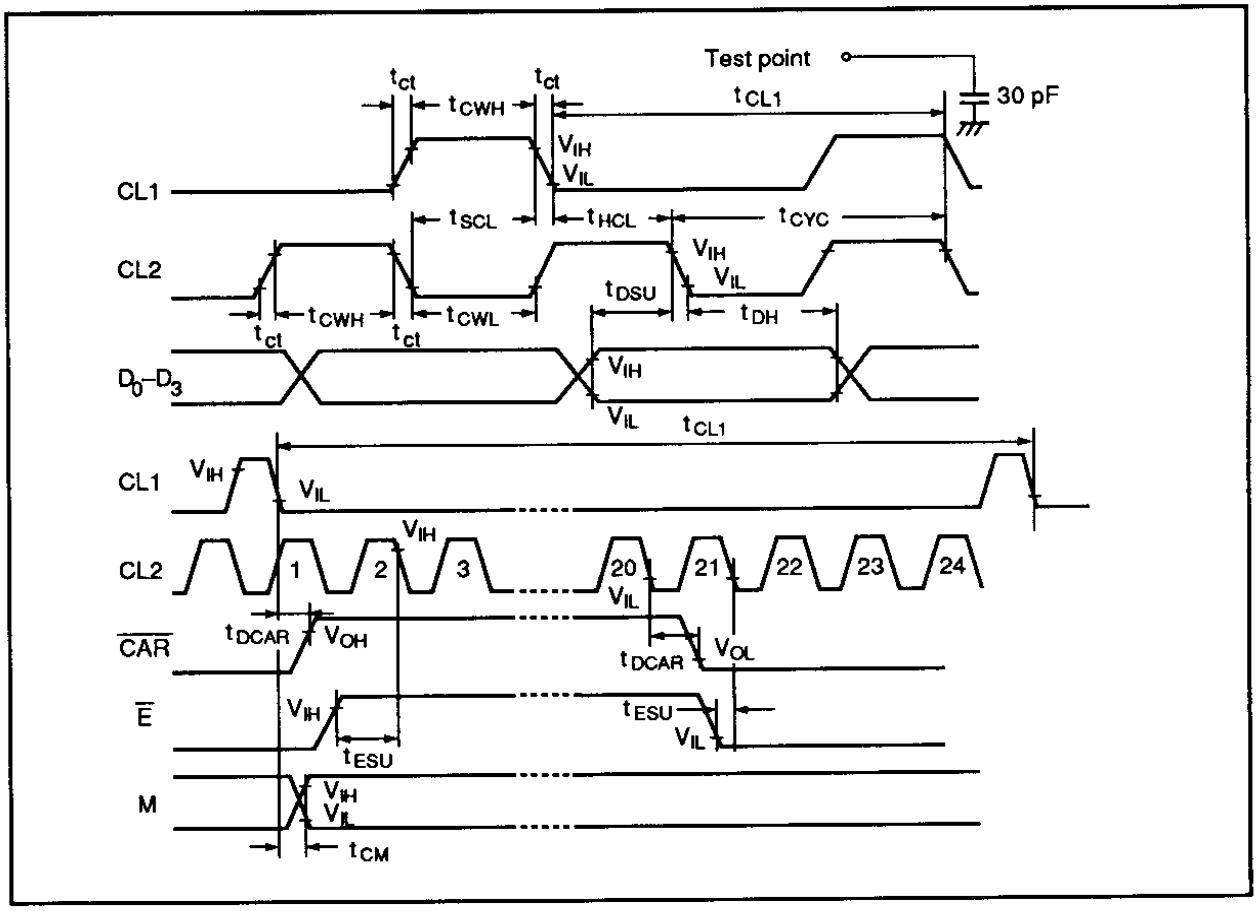
Applicable Terminals : Y1–Y80

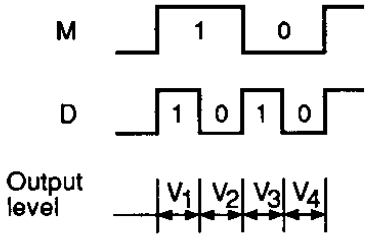


AC Characteristics
(V_{CC} = 5 V ± 10%, GND = 0 V, Ta = -20 to ±75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Clock cycle time	t_{CYC}	285	—	—	ns	
Clock high level width	t_{CWH}	110	—	—	ns	
Clock low level width	t_{CWL}	110	—	—	ns	
Clock setup time	t_{SCL}	80	—	—	ns	
Clock hold time	t_{HCL}	80	—	—	ns	
Clock rise/fall time	t_{CT}	—	—	30	ns	
Data setup time	t_{DSU}	80	—	—	ns	
Data hold time	t_{DH}	80	—	—	ns	
E setup time	t_{ESU}	75	—	—	ns	
Output delay time	t_{DCAR}	—	—	180	ns	1
M phase difference time	t_{CM}	—	—	300	ns	
CL1 cycle time	t_{CL1}	$t_{CYC} \times 10$	—	—	ns	

Note: 1. The following load circuit is connected for specification:



Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_1 V_2 V_3 V_4	4		Power supply	Power supply for liquid crystal drive. V_1, V_2: selection level V_3, V_4: non-selection level
Y1–Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V_1, V_2, V_3, and V_4. Relation among output level, M, and display data (D) is as follows: 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (falling edge triggered). Synchronized with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge triggered.
D_0–D_3	4	I	Controller	Input of 4-bit display data (D)

D	Liquid Crystal Driver Output	Liquid Crystal Display
1 (High level)	Selection level	On
0 (Low level)	Non-selection level	Off

Truth table (Positive logic)

SHL	Input data and latch circuit 1
0	$D_3 \rightarrow 1 \rightarrow 5 \rightarrow 9$ --- $\rightarrow 73 \rightarrow 77$
	$D_2 \rightarrow 2 \rightarrow 6 \rightarrow 10$ --- $\rightarrow 74 \rightarrow 78$
	$D_1 \rightarrow 3 \rightarrow 7 \rightarrow 11$ --- $\rightarrow 75 \rightarrow 79$
	$D_0 \rightarrow 4 \rightarrow 8 \rightarrow 12$ --- $\rightarrow 76 \rightarrow 80$

Terminal Name	Number of Terminals	I/O	Connected to	Functions
				Truth table (Positive logic) (cont) SHL — Input data and latch circuit 1 1 — $D_3 \rightarrow 80 \rightarrow 76 \rightarrow 72 \text{---} \rightarrow 8 \rightarrow 4$ $D_2 \rightarrow 79 \rightarrow 75 \rightarrow 71 \text{---} \rightarrow 7 \rightarrow 3$ $D_1 \rightarrow 78 \rightarrow 74 \rightarrow 70 \text{---} \rightarrow 6 \rightarrow 2$ $D_0 \rightarrow 77 \rightarrow 73 \rightarrow 69 \text{---} \rightarrow 5 \rightarrow 1$ ex: When SHL = 0, the data that is input to D_3 is latched to each bit of the latch circuit 1 in order of $1 \rightarrow 5 \rightarrow 9 \text{---} \rightarrow 77$.
SHL	1	I	V_{CC} or GND	Selects a shift direction of display data.
$\overline{E}$	1	I	GND or the terminal $\overline{CAR}$ of the HD61104	Enable input. The operation stops at high level, and is enabled at low level.
$\overline{CAR}$	1	O	Input terminal $\overline{E}$ of the HD61104	Enable output. Used for cascade connection.
NC	3			Unused. No wire should be connected.

Typical Application

Figure 1 is an LCD panel with 200 × 640 dots on which characters are displayed with 1/200 duty cycle dynamic drive.

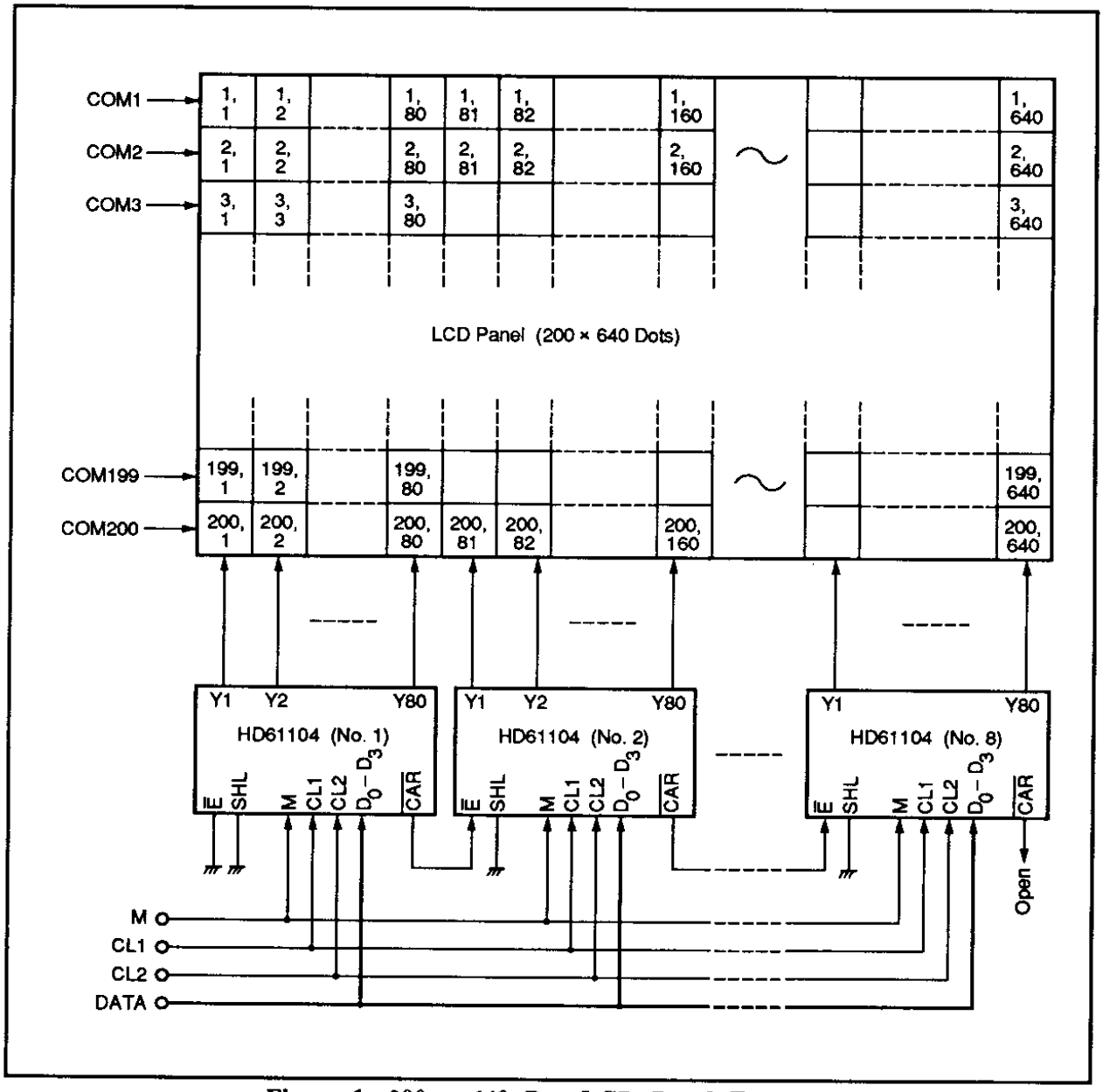


Figure 1 200 × 640 Dot LCD Panel Example

Cascade eight HD61104s. Input data to the D_0—D_3 terminals of Nos. 1–8. Connect $\overline{E}$ of No. 1 to GND. Connect no lines to $\overline{CAR}$ of No. 8 . Connect common signal terminals (COM1–COM200) to the common driver HD61105. (m,n) of LCD panel is the address corresponding to each dot. Figure 2 shows timing.

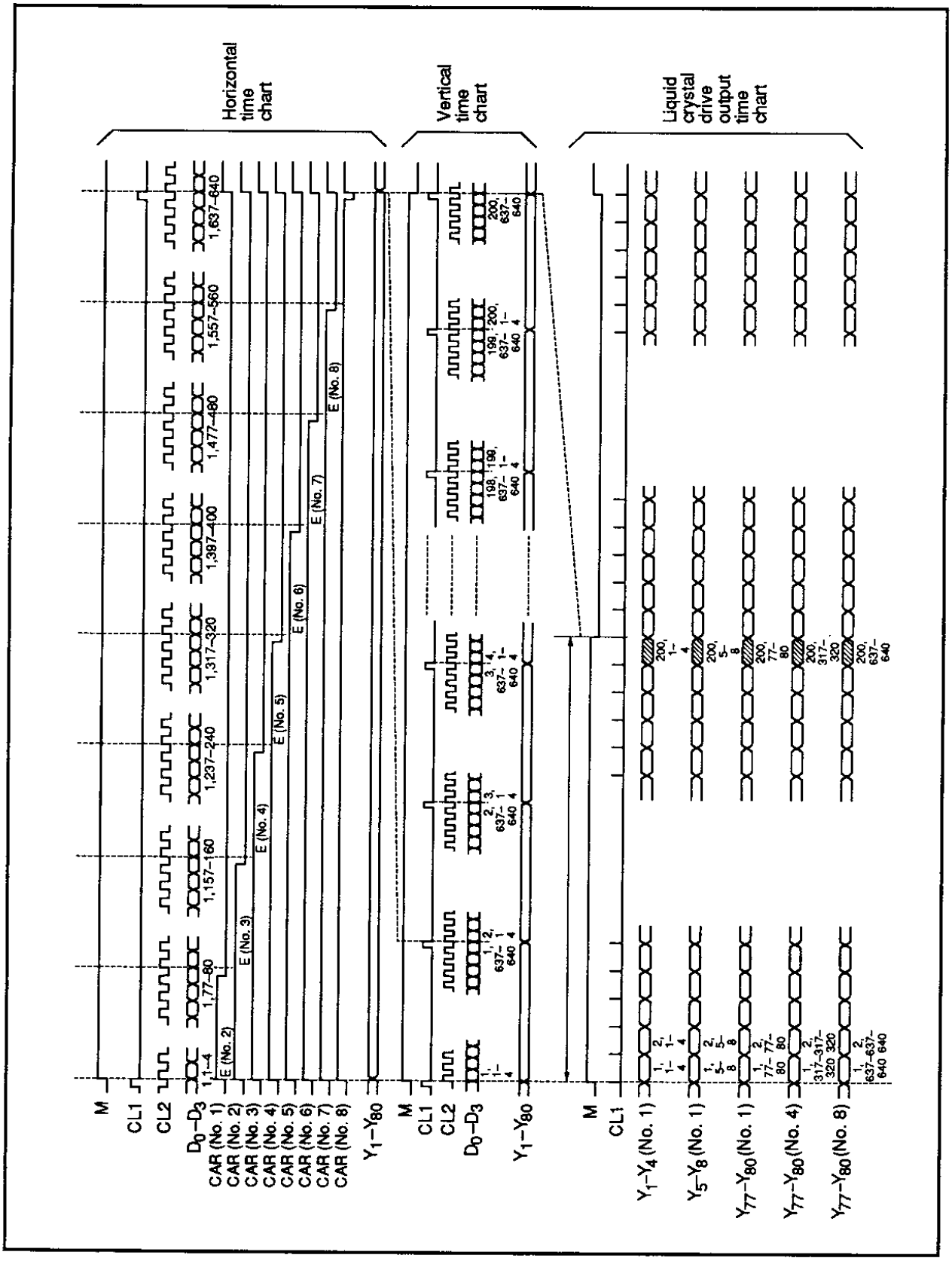


Figure 2 Waveform Example