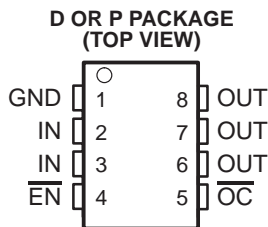


- **33-mΩ (5-V Input) High-Side MOSFET Switch**
- **Short-Circuit and Thermal Protection**
- **Overcurrent Logic Output**
- **Operating Range . . . 2.7 V to 5.5 V**
- **Logic-Level Enable Input**
- **Typical Rise Time . . . 6.1 ms**
- **Undervoltage Lockout**
- **Maximum Standby Supply Current . . . 10 μA**
- **No Drain-Source Back-Gate Diode**
- **Available in 8-pin SOIC and PDIP Packages**
- **Ambient Temperature Range, –40°C to 85°C**
- **2-kV Human-Body-Model, 200-V Machine-Model ESD Protection**
- **UL Listed – File No. E169910**



## description

The TPS202x family of power distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices are 50-mΩ N-channel MOSFET high-side power switches. The switch is controlled by a logic enable compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS202x limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ( $\overline{OC}$ ) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

The TPS202x devices differ only in short-circuit current threshold. The TPS2020 limits at 0.3-A load, the TPS2021 at 0.9-A load, the TPS2022 at 1.5-A load, the TPS2023 at 2.2-A load, and the TPS2024 at 3-A load (see Available Options). The TPS202x is available in an 8-pin small-outline integrated-circuit (SOIC) package and in an 8-pin dual-in-line (DIP) package and operates over a junction temperature range of –40°C to 125°C.

GENERAL SWITCH CATALOG			
<b>33 mΩ, single</b>  TPS201xA 0.2 A – 2 A <b>TPS202x</b> 0.2 A – 2 A TPS203x 0.2 A – 2 A	<b>80 mΩ, dual</b>  TPS2042 500 mA TPS2052 500 mA TPS2046 250 mA TPS2056 250 mA	<b>80 mΩ, triple</b>  TPS2043 500 mA TPS2053 500 mA TPS2047 250 mA TPS2057 250 mA	<b>80 mΩ, quad</b>  TPS2044 500 mA TPS2054 500 mA TPS2048 250 mA TPS2058 250 mA
<b>80 mΩ, single</b>  TPS2014 600 mA TPS2015 1 A TPS2041 500 mA TPS2051 500 mA TPS2045 250 mA TPS2055 250 mA	<b>260 mΩ</b>  TPS2100/1 IN1 500 mA IN2 10 mA TPS2102/3/4/5 IN1 500 mA IN2 100 mA		



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

# TPS2020, TPS2021, TPS2022, TPS2023, TPS2024 POWER-DISTRIBUTION SWITCHES

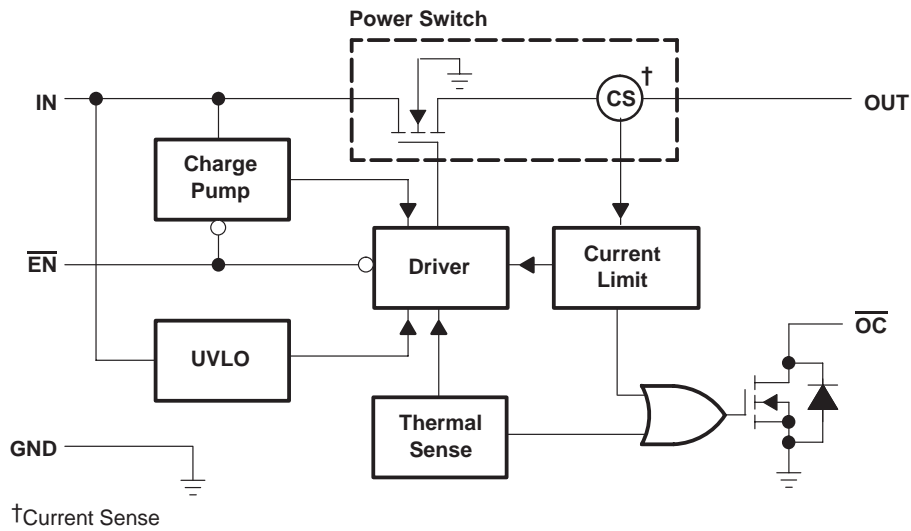
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## AVAILABLE OPTIONS

T <sub>A</sub>	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SMALL OUTLINE (D) <sup>†</sup>	PLASTIC DIP (P)
-40°C to 85°C	Active low	0.2	0.3	TPS2020D	TPS2020P
		0.6	0.9	TPS2021D	TPS2021P
		1	1.5	TPS2022D	TPS2022P
		1.5	2.2	TPS2023D	TPS2023P
		2	3	TPS2024D	TPS2024P

<sup>†</sup> The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2020DR)

## TPS2020 functional block diagram



## Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO. D OR P		
$\overline{\text{EN}}$	4	I	Enable input. Logic low turns on power switch.
GND	1	I	Ground
IN	2, 3	I	Input voltage
$\overline{\text{OC}}$	5	O	Overcurrent. Logic output active low
OUT	6, 7, 8	O	Power-switch output

---

## detailed description

### power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 50 m $\Omega$  ( $V_{I(IN)} = 5$  V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled.

### charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

### driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 9-ms range.

### enable ( $\overline{EN}$ )

The logic enable disables the power switch, the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10  $\mu$ A when a logic high is present on  $\overline{EN}$ . A logic zero input on  $\overline{EN}$  restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

### overcurrent ( $\overline{OC}$ )

The  $\overline{OC}$  open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

### current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver, in turn, reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

### thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

### undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

# TPS2020, TPS2021, TPS2022, TPS2023, TPS2024 POWER-DISTRIBUTION SWITCHES

SLVS175B – DECEMBER 1998 – REVISED MARCH 2004

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1)	–0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (see Note 1)	–0.3 V to $V_{I(IN)} + 0.3$ V
Input voltage range, $V_{I(EN)}$	–0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$	internally limited
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$	–40°C to 125°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Electrostatic discharge (ESD) protection: Human body model	2 kV
Machine model	200V
Charged device model (CDM)	750 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

## recommended operating conditions

		MIN	MAX	UNIT
Input voltage	$V_{I(IN)}$	2.7	5.5	V
	$V_{I(EN)}$	0	5.5	V
Continuous output current, $I_O$	TPS2020	0	0.2	A
	TPS2021	0	0.6	
	TPS2022	0	1	
	TPS2023	0	1.5	
	TPS2024	0	2	
Operating virtual junction temperature, $T_J$		–40	125	°C

# TPS2020, TPS2021, TPS2022, TPS2023, TPS2024 POWER-DISTRIBUTION SWITCHES

SLVS175B – DECEMBER 1998 – REVISED MARCH 2004

electrical characteristics over recommended operating junction temperature range,  $V_{I(IN)} = 5.5\text{ V}$ ,  $I_O = \text{rated current}$ ,  $\overline{EN} = 0\text{ V}$  (unless otherwise noted)

## power switch

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{I(IN)} = 5\text{ V}$ , $T_J = 25^\circ\text{C}$ , $I_O = 1.8\text{ A}$		33	36	m $\Omega$
		$V_{I(IN)} = 5\text{ V}$ , $T_J = 85^\circ\text{C}$ , $I_O = 1.8\text{ A}$		38	46	
		$V_{I(IN)} = 5\text{ V}$ , $T_J = 125^\circ\text{C}$ , $I_O = 1.8\text{ A}$		44	50	
		$V_{I(IN)} = 3.3\text{ V}$ , $T_J = 25^\circ\text{C}$ , $I_O = 1.8\text{ A}$		37	41	
		$V_{I(IN)} = 3.3\text{ V}$ , $T_J = 85^\circ\text{C}$ , $I_O = 1.8\text{ A}$		43	52	
		$V_{I(IN)} = 3.3\text{ V}$ , $T_J = 125^\circ\text{C}$ , $I_O = 1.8\text{ A}$		51	61	
		$V_{I(IN)} = 5\text{ V}$ , $T_J = 25^\circ\text{C}$ , $I_O = 0.18\text{ A}$		30	34	
		$V_{I(IN)} = 5\text{ V}$ , $T_J = 85^\circ\text{C}$ , $I_O = 0.18\text{ A}$		35	41	
		$V_{I(IN)} = 5\text{ V}$ , $T_J = 125^\circ\text{C}$ , $I_O = 0.18\text{ A}$		39	47	
		$V_{I(IN)} = 3.3\text{ V}$ , $T_J = 25^\circ\text{C}$ , $I_O = 0.18\text{ A}$		33	37	
		$V_{I(IN)} = 3.3\text{ V}$ , $T_J = 85^\circ\text{C}$ , $I_O = 0.18\text{ A}$		39	46	
$V_{I(IN)} = 3.3\text{ V}$ , $T_J = 125^\circ\text{C}$ , $I_O = 0.18\text{ A}$		44	56			
$t_r$	Rise time, output	$V_{I(IN)} = 5.5\text{ V}$ , $T_J = 25^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$ , $R_L = 10\ \Omega$		6.1		ms
		$V_{I(IN)} = 2.7\text{ V}$ , $T_J = 25^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$ , $R_L = 10\ \Omega$		8.6		
$t_f$	Fall time, output	$V_{I(IN)} = 5.5\text{ V}$ , $T_J = 25^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$ , $R_L = 10\ \Omega$		3.4		ms
		$V_{I(IN)} = 2.7\text{ V}$ , $T_J = 25^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$ , $R_L = 10\ \Omega$		3		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

## enable input ( $\overline{EN}$ )

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input voltage	$2.7\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$	2			V
$V_{IL}$	Low-level input voltage	$4.5\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$			0.8	V
		$2.7\text{ V} \leq V_{I(IN)} \leq 4.5\text{ V}$			0.5	
$I_I$	Input current	$\overline{EN} = 0\text{ V}$ or $\overline{EN} = V_{I(IN)}$	-0.5		0.5	$\mu\text{A}$
$t_{on}$	Turnon time	$C_L = 100\ \mu\text{F}$ , $R_L = 10\ \Omega$			20	ms
$t_{off}$	Turnoff time	$C_L = 100\ \mu\text{F}$ , $R_L = 10\ \Omega$			40	

## current limit

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT	
$I_{OS}$	Short-circuit output current	$T_J = 25^\circ\text{C}$ , $V_I = 5.5\text{ V}$ , OUT connected to GND, Device enable into short circuit	TPS2020	0.22	0.3	0.4	A
			TPS2021	0.66	0.9	1.1	
			TPS2022	1.1	1.5	1.8	
			TPS2023	1.65	2.2	2.7	
			TPS2024	2.2	3	3.8	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

# TPS2020, TPS2021, TPS2022, TPS2023, TPS2024 POWER-DISTRIBUTION SWITCHES

SLVS175B – DECEMBER 1998 – REVISED MARCH 2004

electrical characteristics over recommended operating junction temperature range,  $V_{I(IN)} = 5.5\text{ V}$ ,  $I_O = \text{rated current}$ ,  $\overline{EN} = 0\text{ V}$  (unless otherwise noted) (continued)

## supply current

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply current, low-level output	No Load on OUT	$\overline{EN} = V_{I(IN)}$	$T_J = 25^\circ\text{C}$	0.3	1	$\mu\text{A}$	
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		10		
Supply current, high-level output	No Load on OUT	$\overline{EN} = 0\text{ V}$	$T_J = 25^\circ\text{C}$	58	75	$\mu\text{A}$	
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	75	100		
Leakage current	OUT connected to ground	$\overline{EN} = V_{I(IN)}$	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	10		$\mu\text{A}$	

## undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-level input voltage		2		2.5	V
Hysteresis	$T_J = 25^\circ\text{C}$		100		mV

## overcurrent ( $\overline{OC}$ )

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output low voltage	$I_O = 10\text{ mA}$ , $V_{OL}(\overline{OC})$			0.4	V
Off-state current <sup>†</sup>	$V_O = 5\text{ V}$ , $V_O = 3.3\text{ V}$			1	$\mu\text{A}$

<sup>†</sup> Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

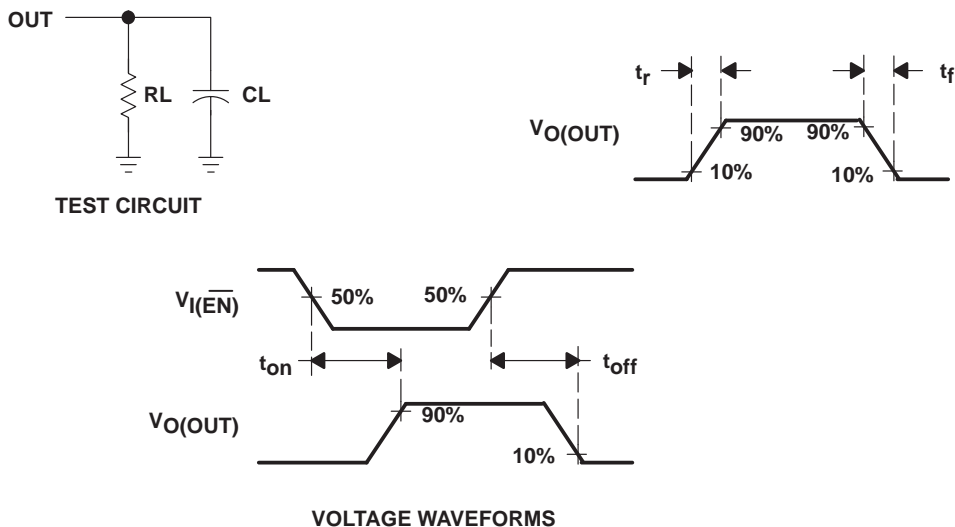


Figure 1. Test Circuit and Voltage Waveforms

Table of Timing Diagrams

	FIGURE
Turnon Delay and Rise Time	2
Turnoff Delay and Fall Time	3
Turnon Delay and Rise Time with 1- $\mu$ F Load	4
Turnoff Delay and Rise Time with 1- $\mu$ F Load	5
Device Enabled into Short	6
TPS2020, TPS2021, TPS2022, TPS2023, and TPS2024, Ramped Load on Enabled Device	7, 8, 9, 10, 11
TPS2024, Inrush Current	12
7.9- $\Omega$ Load Connected to an Enabled TPS2020 Device	13
3.7- $\Omega$ Load Connected to an Enabled TPS2020 Device	14
3.7- $\Omega$ Load Connected to an Enabled TPS2021 Device	15
2.6- $\Omega$ Load Connected to an Enabled TPS2021 Device	16
2.6- $\Omega$ Load Connected to an Enabled TPS2022 Device	17
1.2- $\Omega$ Load Connected to an Enabled TPS2022 Device	18
1.2- $\Omega$ Load Connected to an Enabled TPS2023 Device	19
0.9- $\Omega$ Load Connected to an Enabled TPS2023 Device	20
0.9- $\Omega$ Load Connected to an Enabled TPS2024 Device	21
0.5- $\Omega$ Load Connected to an Enabled TPS2024 Device	22

PARAMETER MEASUREMENT INFORMATION

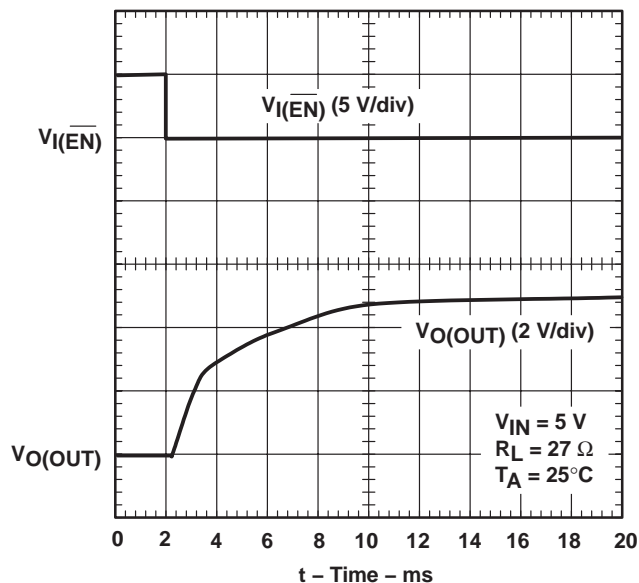


Figure 2. Turnon Delay and Rise Time

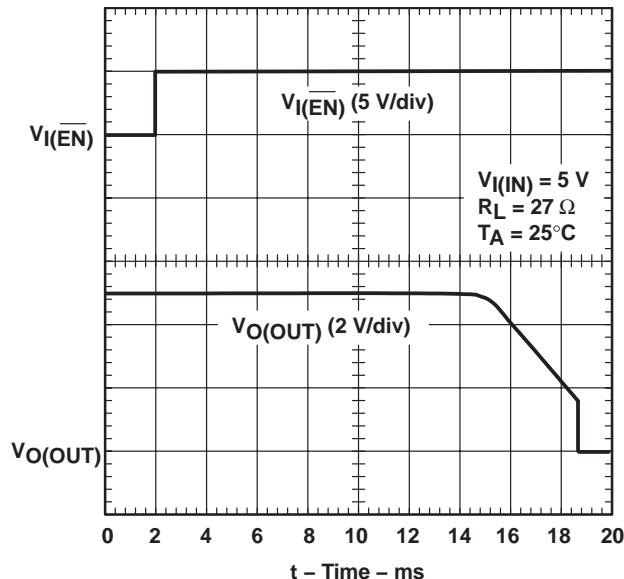


Figure 3. Turnoff Delay and Fall Time

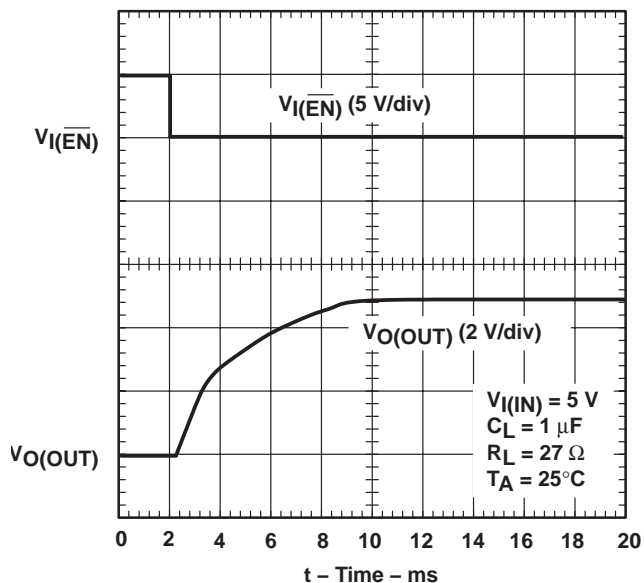


Figure 4. Turnon Delay and Rise Time  
 With 1-μF Load

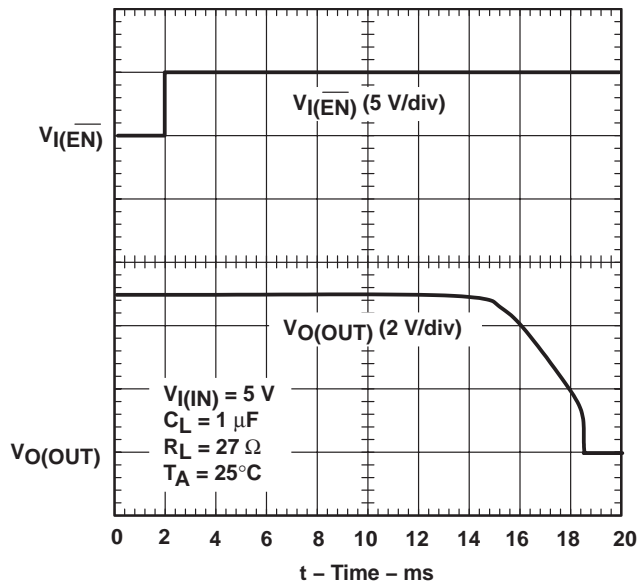


Figure 5. Turnoff Delay and Fall Time  
 With 1-μF Load



PARAMETER MEASUREMENT INFORMATION

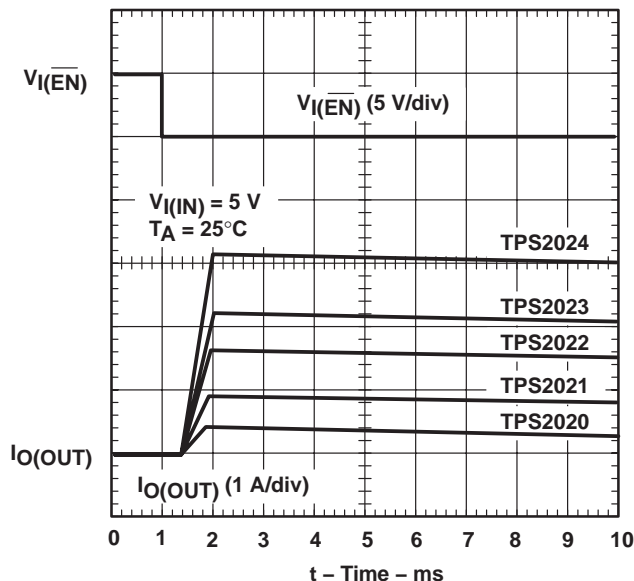


Figure 6. Device Enabled Into Short

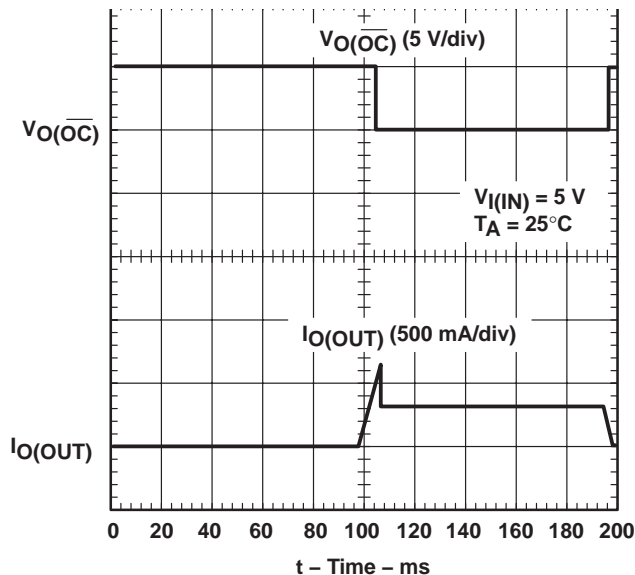


Figure 7. TPS2020, Ramped Load on Enabled Device

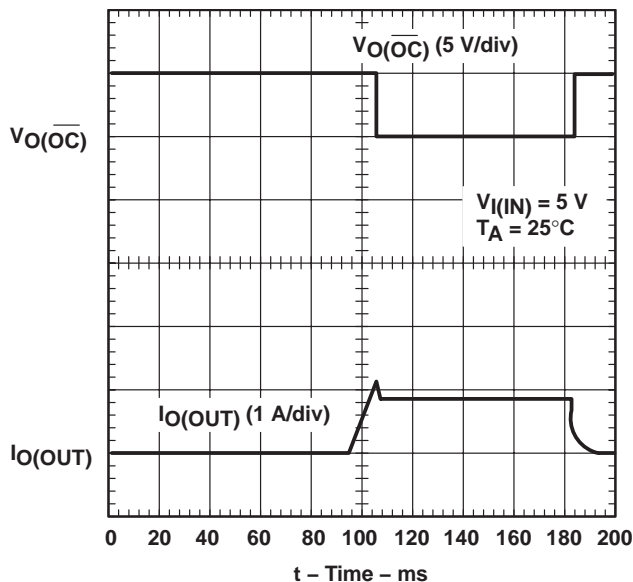


Figure 8. TPS2021, Ramped Load on Enabled Device

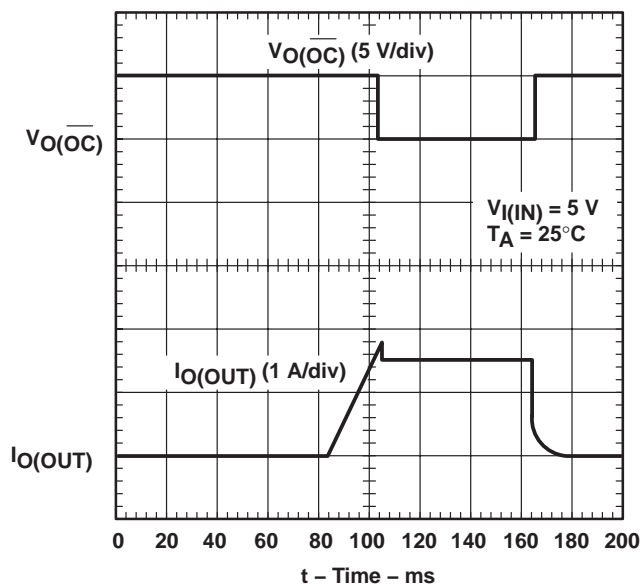


Figure 9. TPS2022, Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

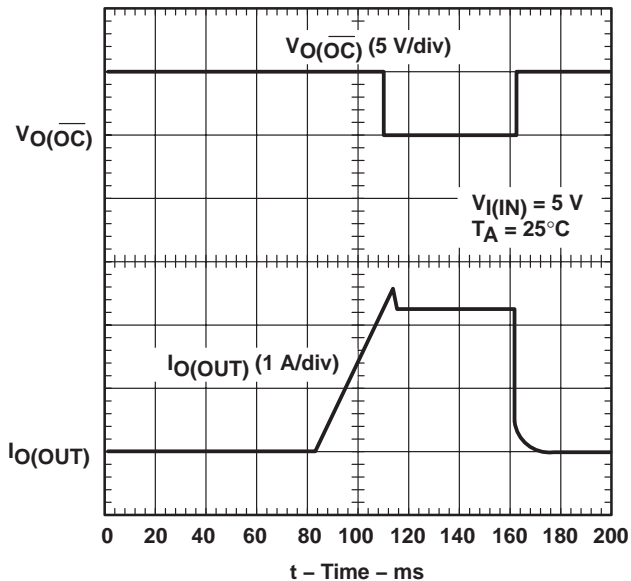


Figure 10. TPS2023, Ramped Load on Enabled Device

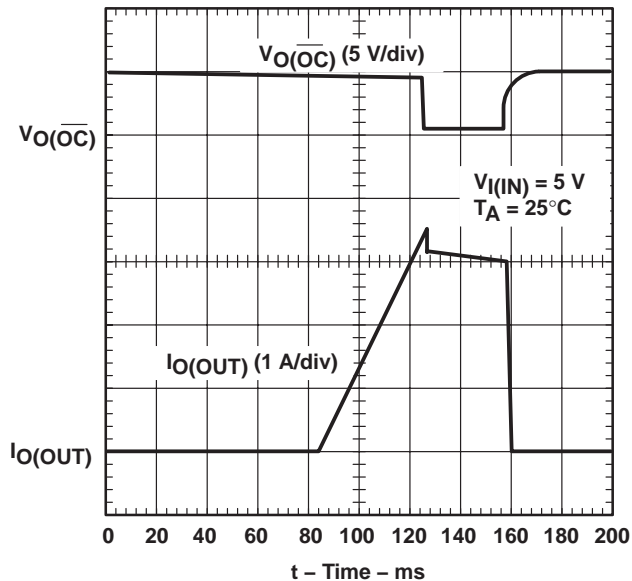


Figure 11. TPS2024, Ramped Load on Enabled Device

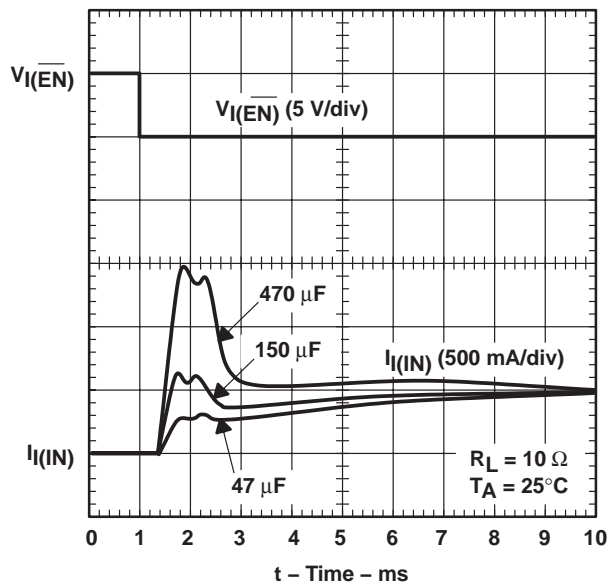


Figure 12. TPS2024, Inrush Current

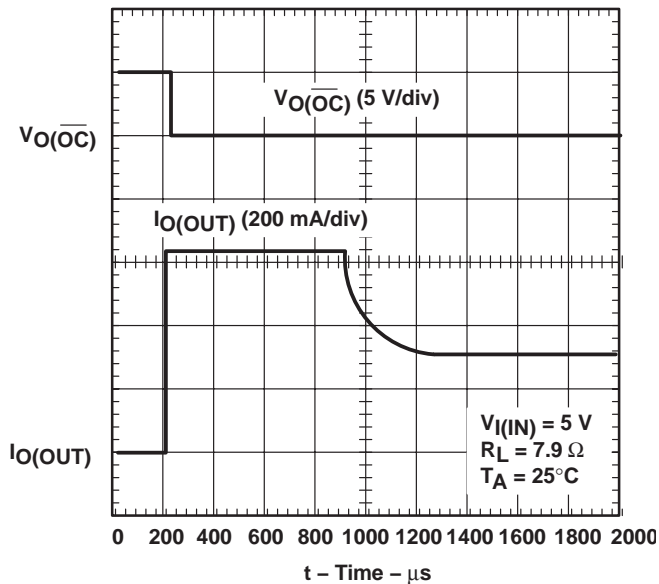


Figure 13. 7.9-Ω Load Connected to an Enabled TPS2020 Device

PARAMETER MEASUREMENT INFORMATION

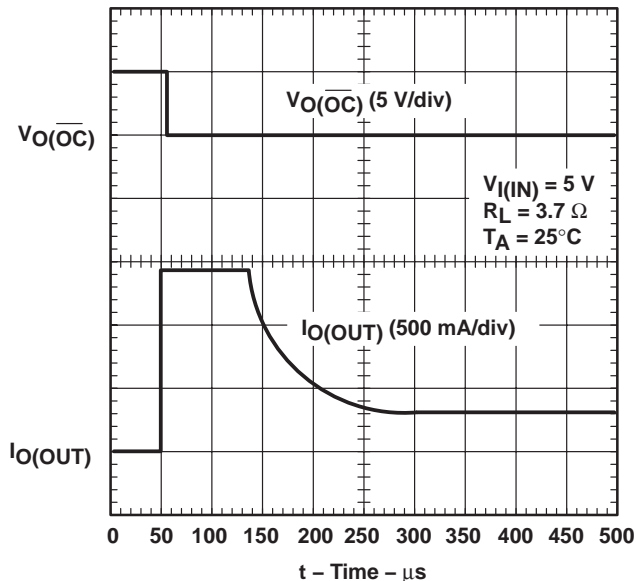


Figure 14. 3.7-Ω Load Connected to an Enabled TPS2020 Device

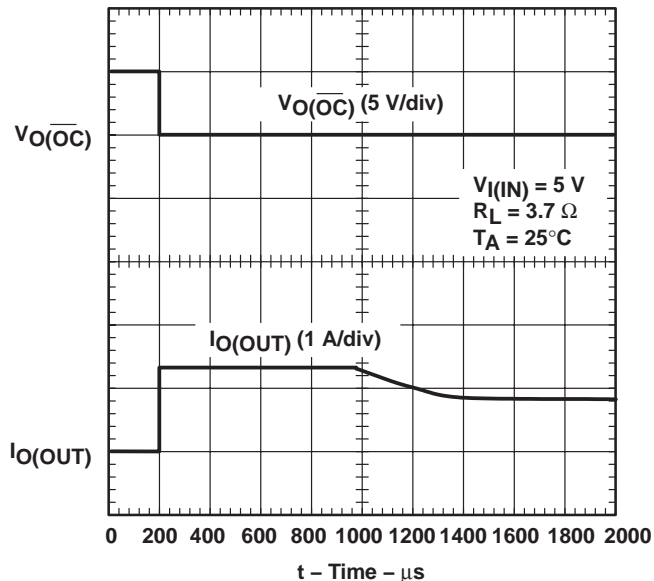


Figure 15. 3.7-Ω Load Connected to an Enabled TPS2021 Device

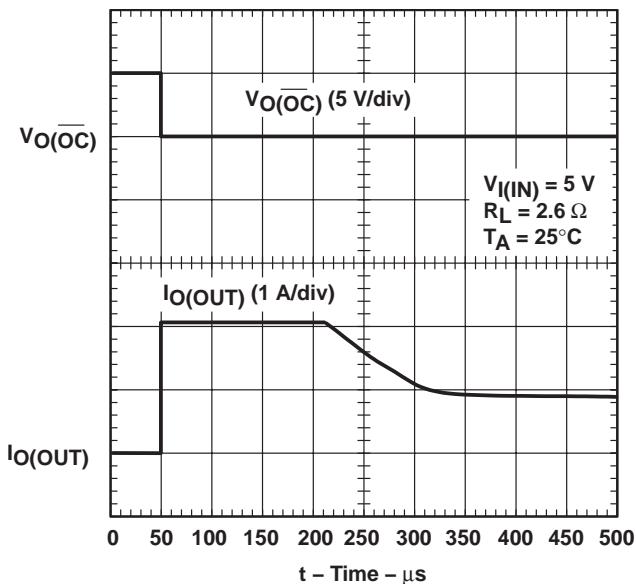


Figure 16. 2.6-Ω Load Connected to an Enabled TPS2021 Device

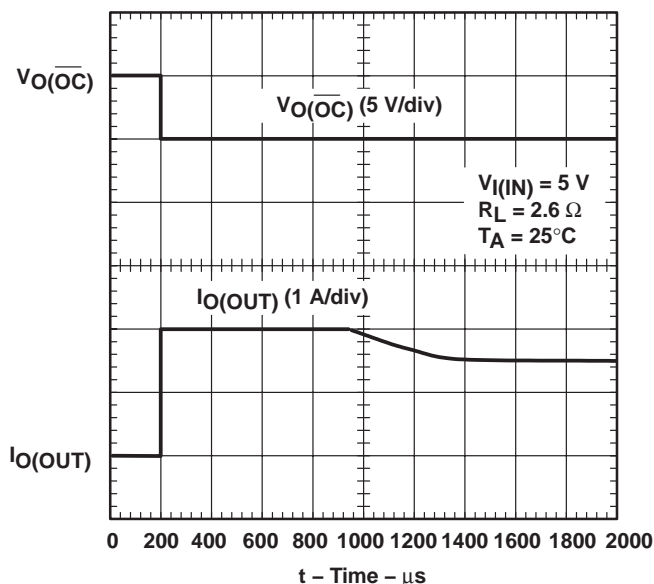
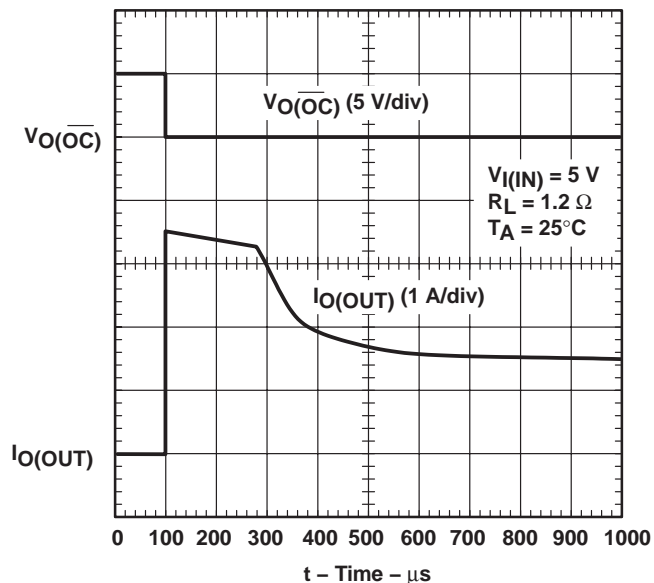
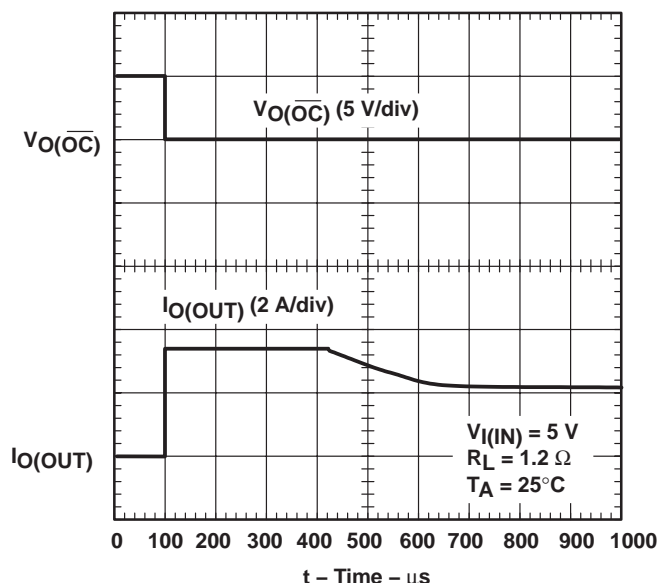


Figure 17. 2.6-Ω Load Connected to an Enabled TPS2022 Device

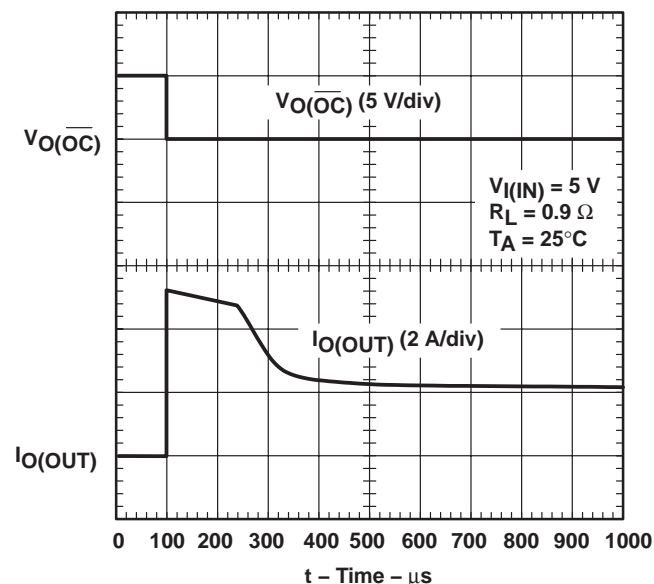
**PARAMETER MEASUREMENT INFORMATION**



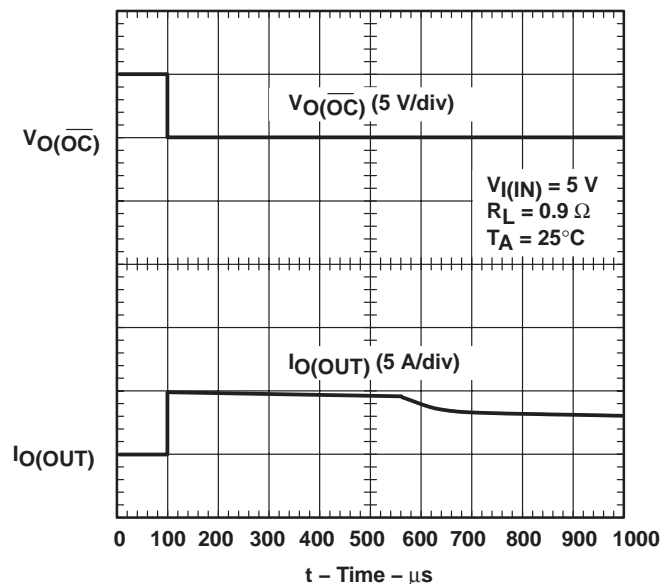
**Figure 18. 1.2-Ω Load Connected to an Enabled TPS2022 Device**



**Figure 19. 1.2-Ω Load Connected to an Enabled TPS2023 Device**



**Figure 20. 0.9-Ω Load Connected to an Enabled TPS2023 Device**



**Figure 21. 0.9-Ω Load Connected to an Enabled TPS2024 Device**

PARAMETER MEASUREMENT INFORMATION

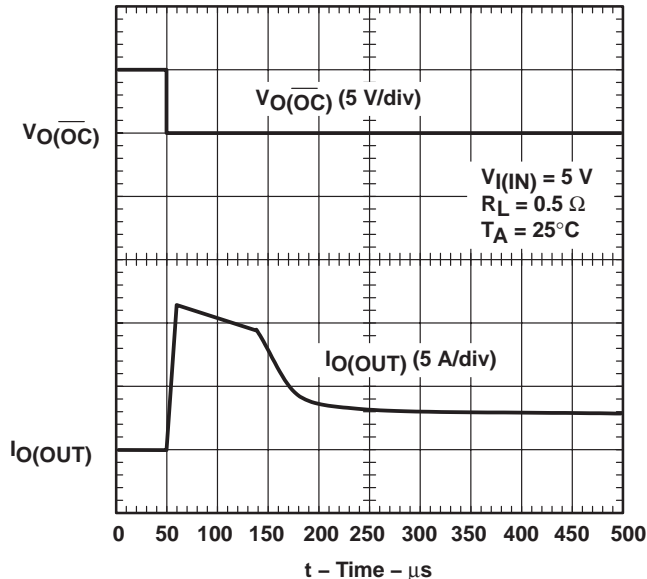


Figure 22. 0.5-Ω Load Connected to an Enabled TPS2024 Device

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$t_{d(on)}$	Turnon delay time	vs Output voltage	23
$t_{d(off)}$	Turnoff delay time	vs Input voltage	24
$t_r$	Rise time	vs Load current	25
$t_f$	Fall time	vs Load current	26
	Supply current (enabled)	vs Junction temperature	27
	Supply current (disabled)	vs Junction temperature	28
	Supply current (enabled)	vs Input voltage	29
	Supply current (disabled)	vs Input voltage	30
$I_{OS}$	Short-circuit current limit	vs Input voltage	31
		vs Junction temperature	32
$r_{DS(on)}$	Static drain-source on-state resistance	vs Input voltage	33
		vs Junction temperature	34
		vs Input voltage	35
		vs Junction temperature	36
$V_I$	Input voltage	Undervoltage lockout	37

TYPICAL CHARACTERISTICS

TURNON DELAY TIME  
vs  
OUTPUT VOLTAGE

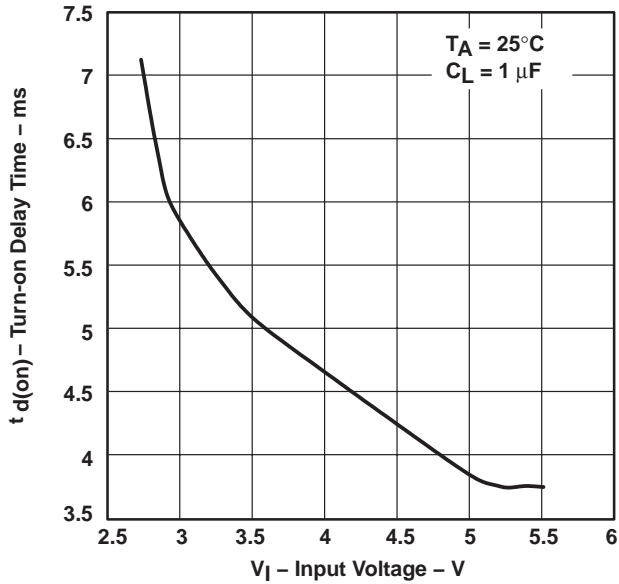


Figure 23

TURNOFF DELAY TIME  
vs  
INPUT VOLTAGE

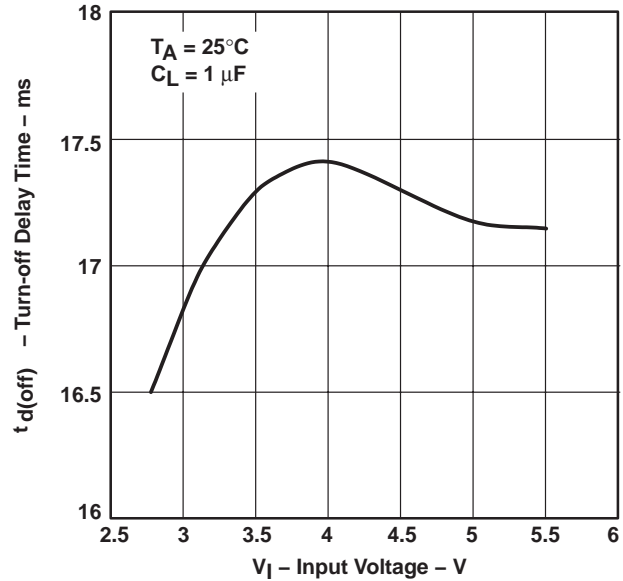


Figure 24

RISE TIME  
vs  
LOAD CURRENT

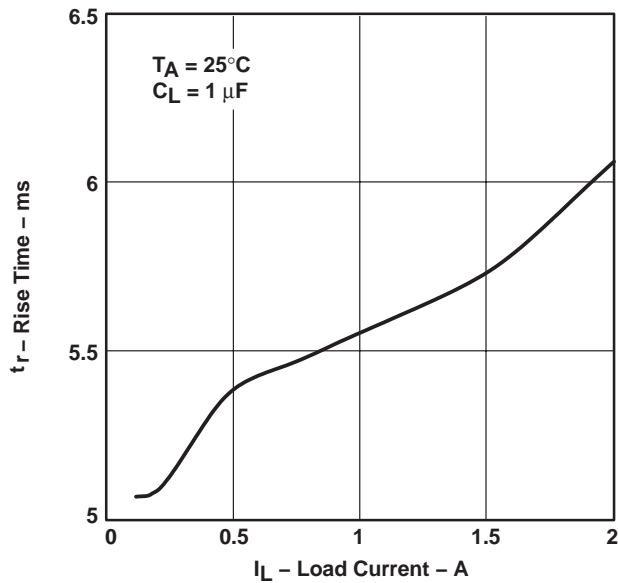


Figure 25

FALL TIME  
vs  
LOAD CURRENT

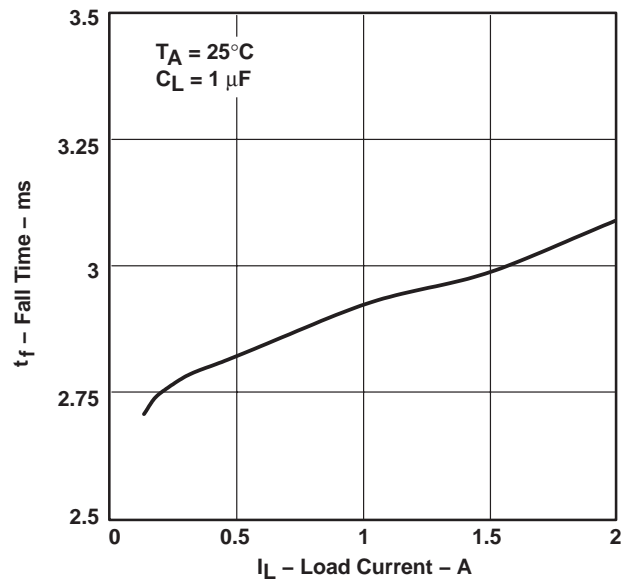


Figure 26

TYPICAL CHARACTERISTICS

SUPPLY CURRENT (ENABLED)  
vs  
JUNCTION TEMPERATURE

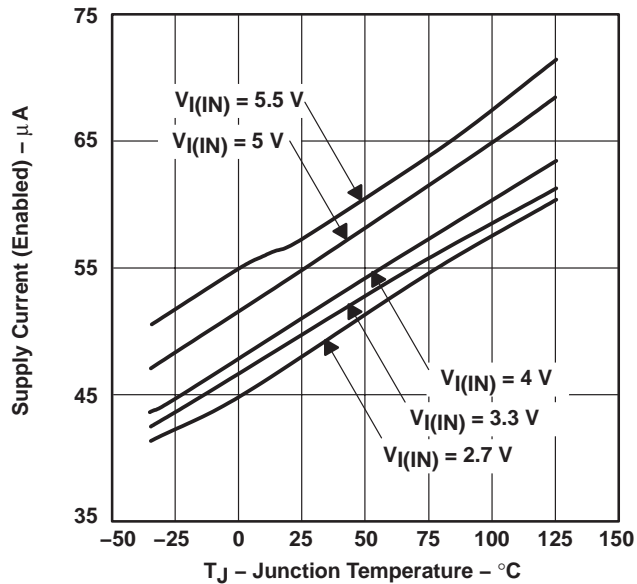


Figure 27

SUPPLY CURRENT (DISABLED)  
vs  
JUNCTION TEMPERATURE

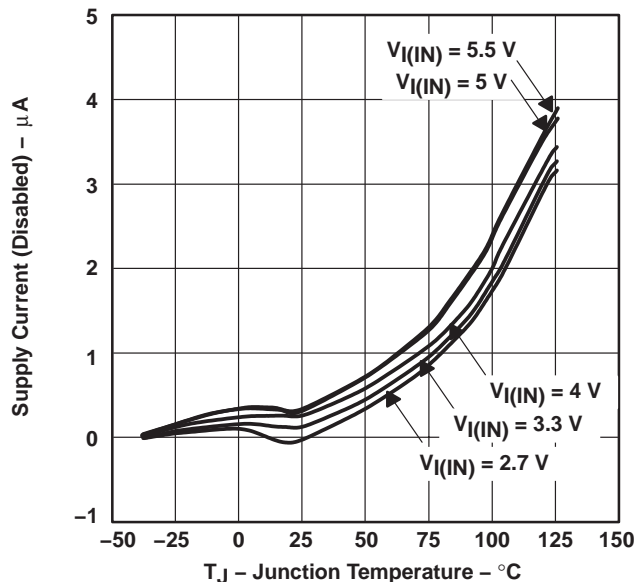


Figure 28

SUPPLY CURRENT (ENABLED)  
vs  
INPUT VOLTAGE

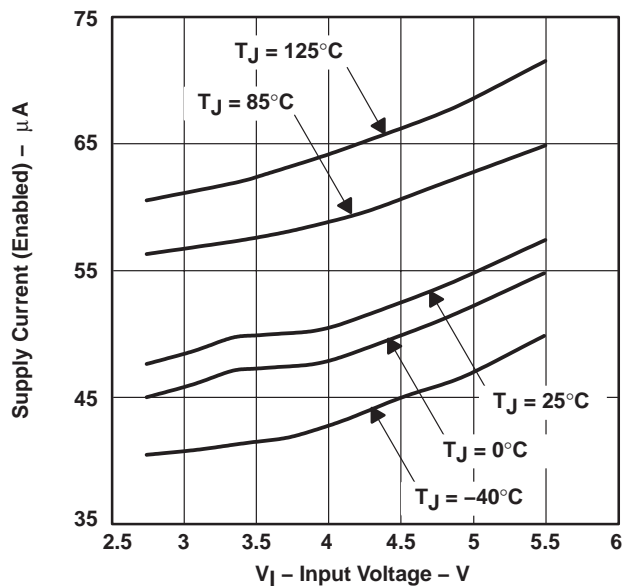


Figure 29

SUPPLY CURRENT (DISABLED)  
vs  
INPUT VOLTAGE

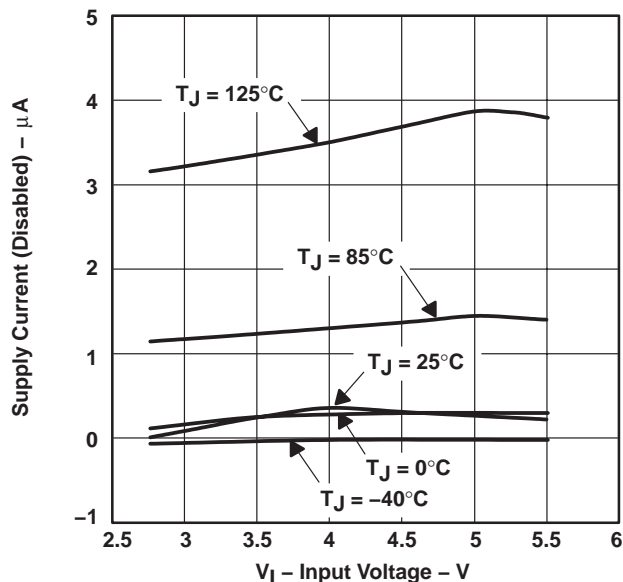


Figure 30

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT CURRENT LIMIT  
vs  
INPUT VOLTAGE

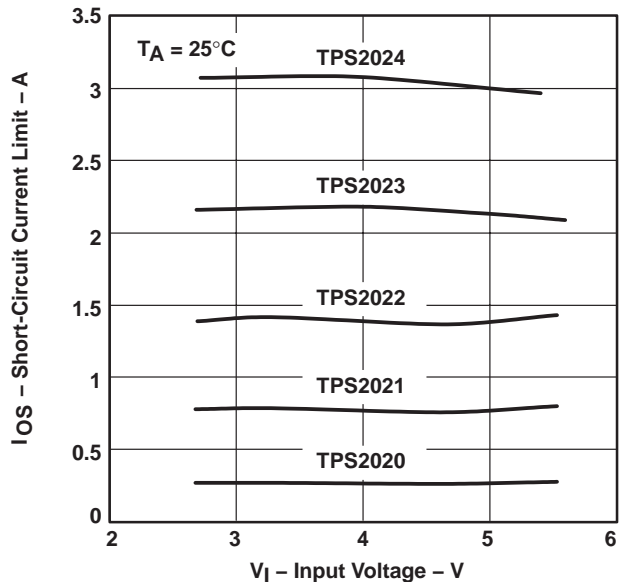


Figure 31

SHORT-CIRCUIT CURRENT LIMIT  
vs  
JUNCTION TEMPERATURE

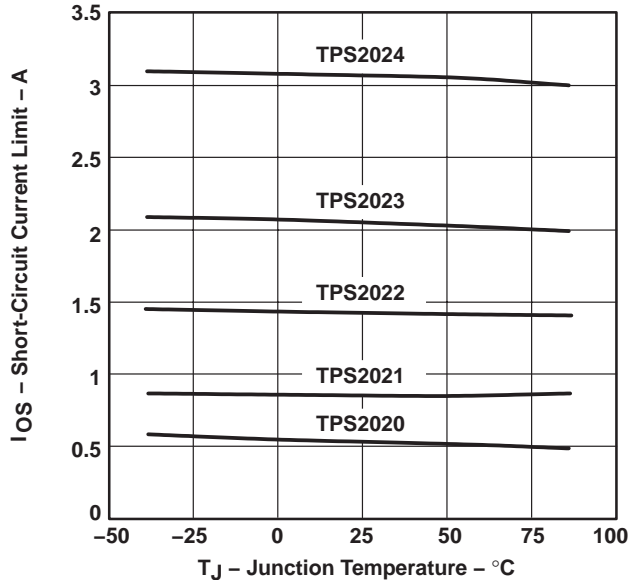


Figure 32

STATIC DRAIN-SOURCE ON-STATE RESISTANCE  
vs  
INPUT VOLTAGE

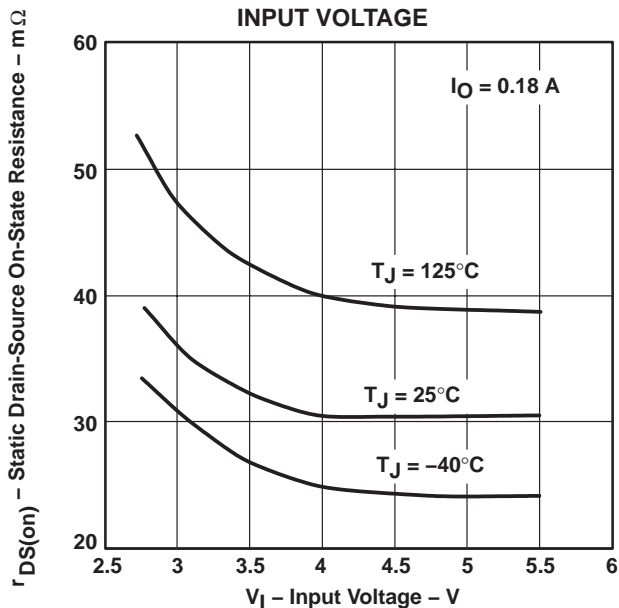


Figure 33

STATIC DRAIN-SOURCE ON-STATE RESISTANCE  
vs  
JUNCTION TEMPERATURE

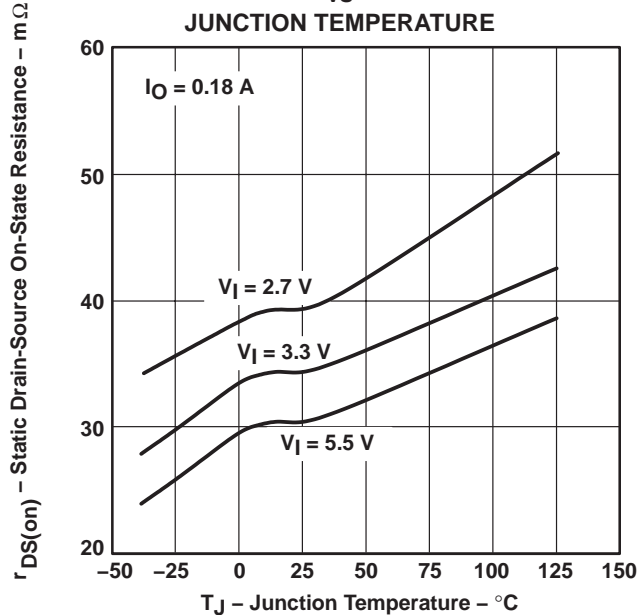


Figure 34



TYPICAL CHARACTERISTICS

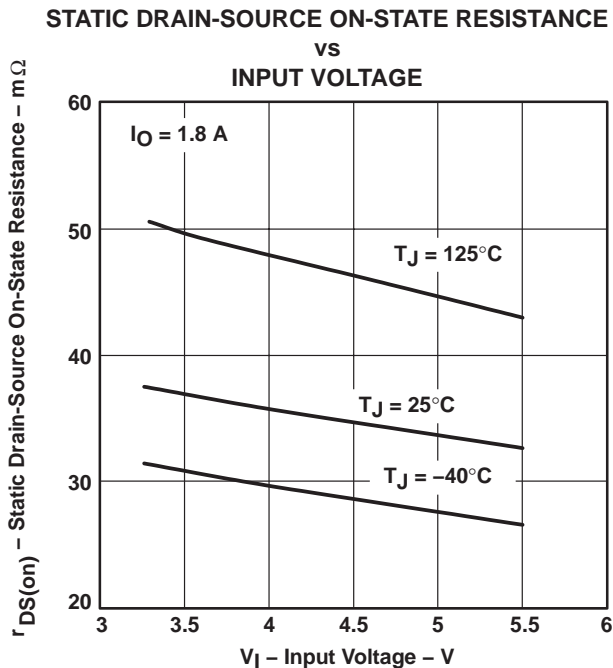


Figure 35

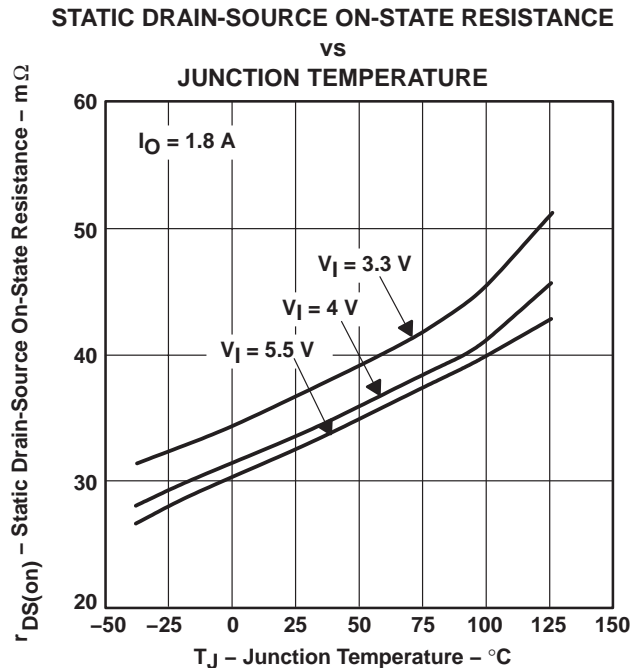


Figure 36

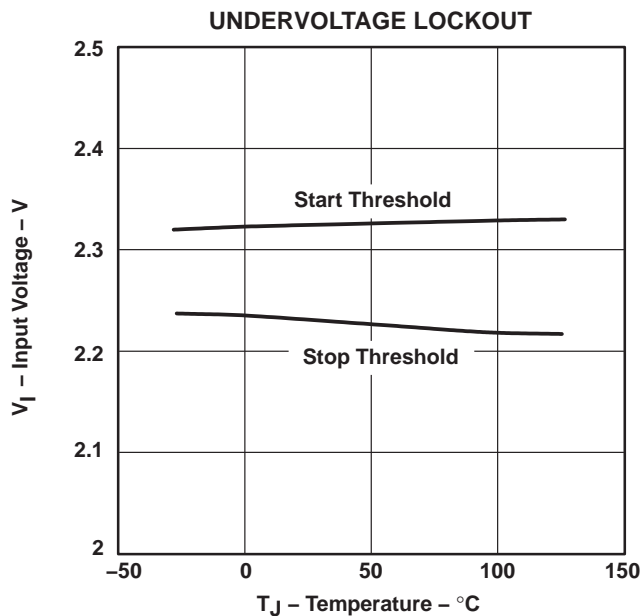


Figure 37

# TPS2020, TPS2021, TPS2022, TPS2023, TPS2024 POWER-DISTRIBUTION SWITCHES

SLVS175B – DECEMBER 1998 – REVISED MARCH 2004

## APPLICATION INFORMATION

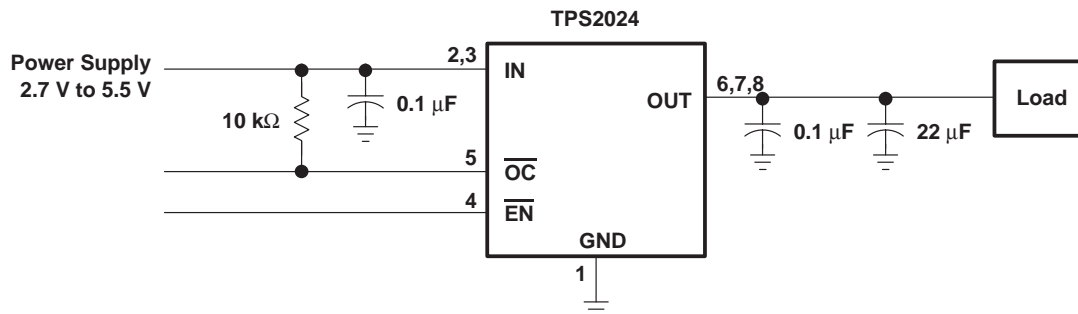


Figure 38. Typical Application

### power-supply considerations

A 0.01- $\mu\text{F}$  to 0.1- $\mu\text{F}$  ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output and input pins is recommended when the output load is heavy. This precaution reduces power supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- $\mu\text{F}$  to 0.1- $\mu\text{F}$  ceramic capacitor improves the immunity of the device to short-circuit transients.

### overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before  $V_{I(IN)}$  has been applied (see Figure 6). The TPS202x senses the short and immediately switches into a constant-current output.

In the second condition, the excessive load occurs while the device is enabled. At the instant the excessive load occurs, very high currents may flow for a short time before the current-limit circuit can react (see Figures 13–22). After the current-limit circuit has tripped (reached the overcurrent trip threshold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figures 7–11). The TPS202x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

### $\overline{\text{OC}}$ response

The  $\overline{\text{OC}}$  open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter can be connected to the  $\overline{\text{OC}}$  pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

APPLICATION INFORMATION

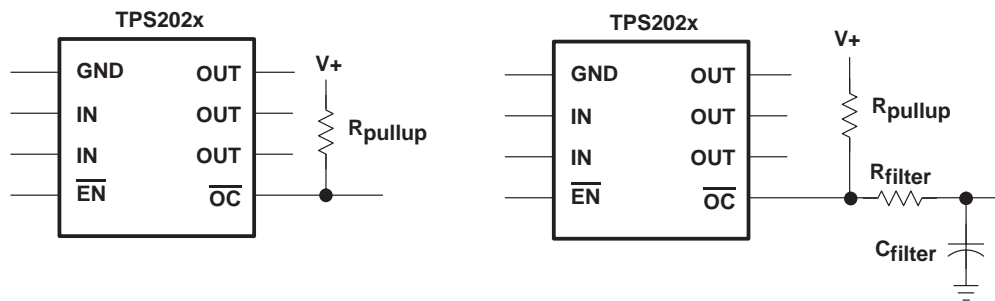


Figure 39. Typical Circuit for  $\overline{OC}$  Pin and RC Filter for Damping Inrush  $\overline{OC}$  Responses

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find  $r_{DS(on)}$  at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read  $r_{DS(on)}$  from Figures 33–36. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$  = Ambient Temperature °C

$R_{\theta JA}$  = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get an acceptable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS202x into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at powerup. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

# TPS2020, TPS2021, TPS2022, TPS2023, TPS2024 POWER-DISTRIBUTION SWITCHES

SLVS175B – DECEMBER 1998 – REVISED MARCH 2004

## APPLICATION INFORMATION

### generic hot-plug applications (see Figure 40)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Because of the controlled rise times and fall times of the TPS202x series, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS202x also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

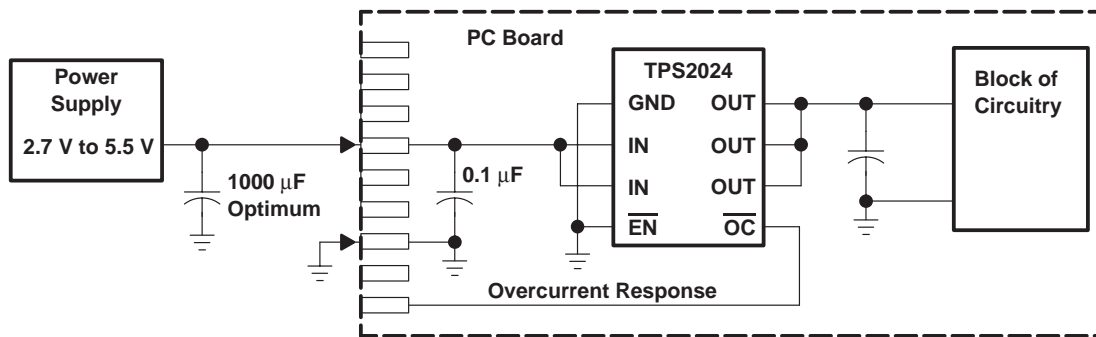


Figure 40. Typical Hot-Plug Implementation

By placing the TPS202x between the  $V_{CC}$  input and the rest of the circuitry, the input power will reach this device first after insertion. The typical rise time of the switch is approximately 9 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS2020D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2020DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2020DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2020DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2020P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2020PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2021D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2021DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2021DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2021DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2021P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2021PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2022D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2022DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2022DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2022DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2022P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2022PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2023D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2023DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2023DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2023DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2023P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2023PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2024D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS2024DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2024DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2024DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2024P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2024PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

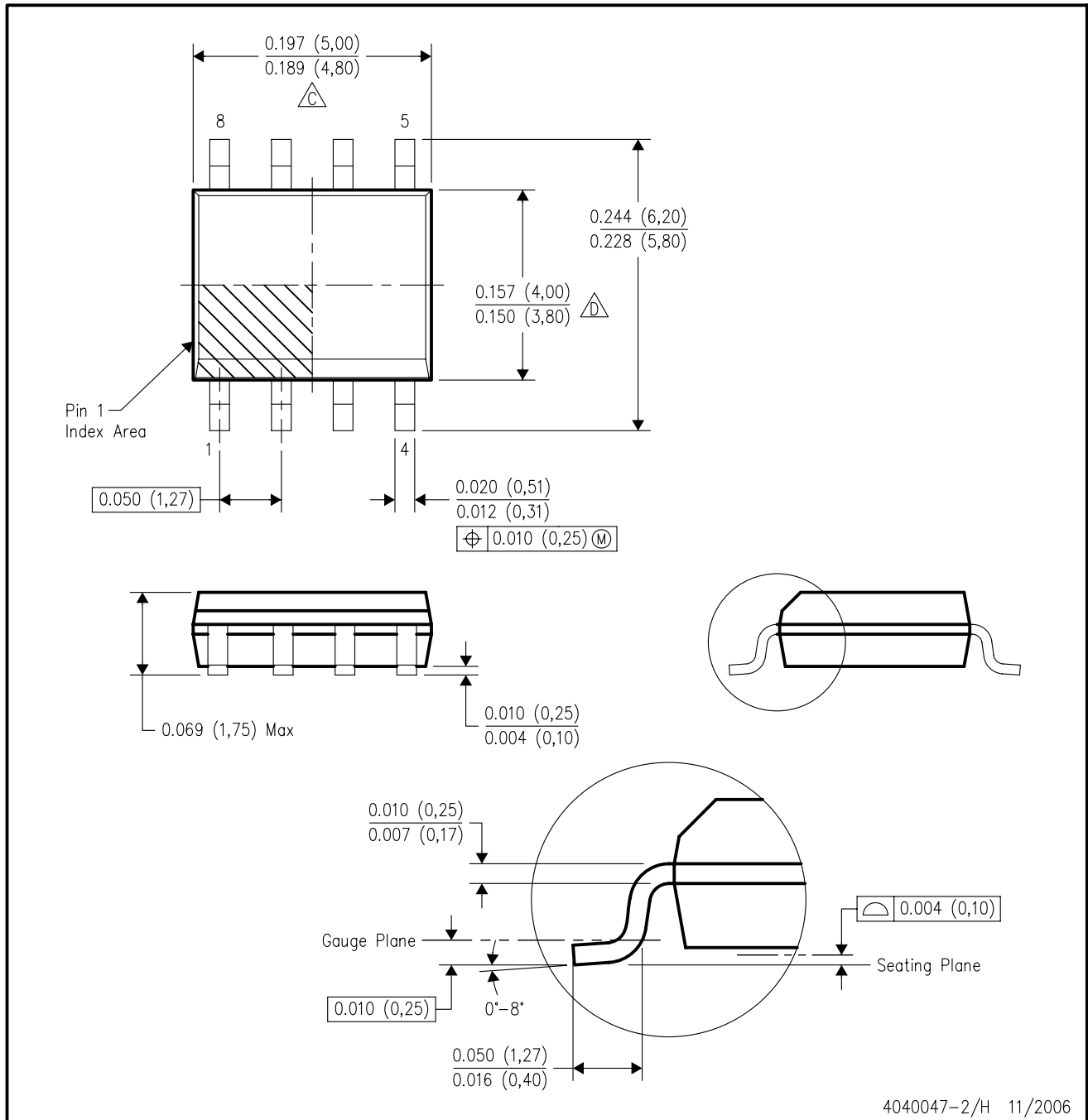
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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.



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