Issue 1: The ground plane – to split or not to split?

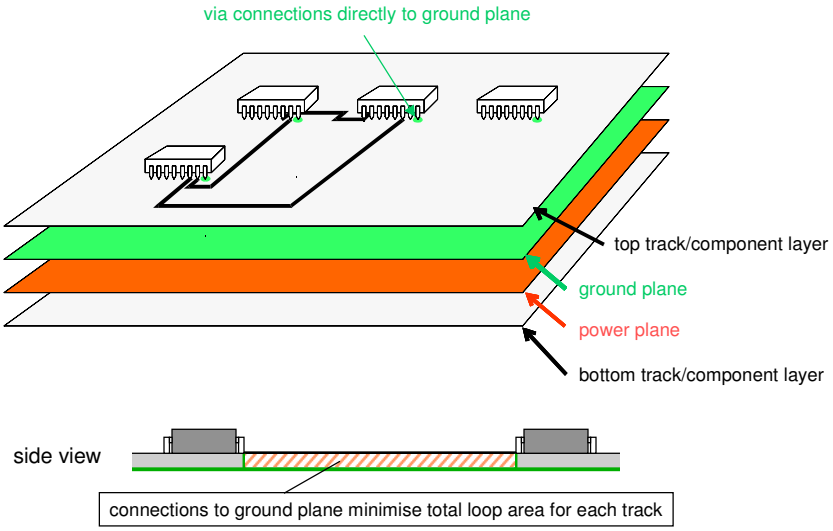
E MAC services

Outline

- The ground plane
- Why split the GP?
- What are the disadvantages of split GPs?
- What happens if you don't split?

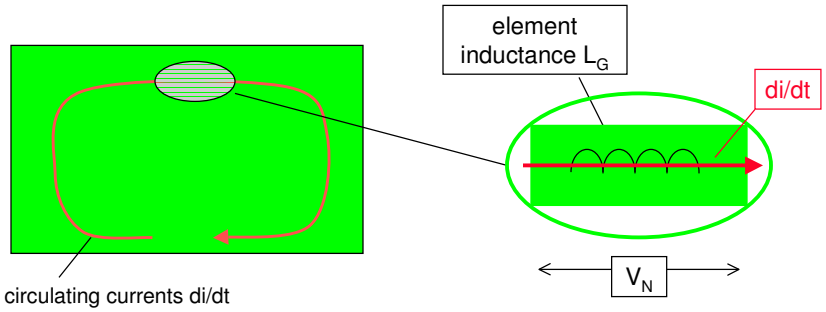
2

The purpose of the ground plane



3

Voltages developed across the GP

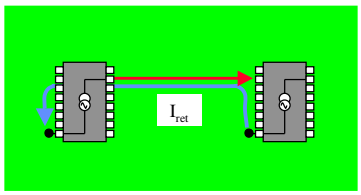


$V_N = -L_G \cdot di/dt$
total noise voltage = ΣV_N

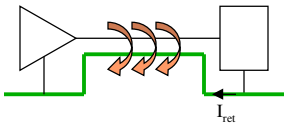
- maximum inductance L_G is at the edges of the ground plane, so ...
- don't cross the edges, and keep them free of high di/dt return currents

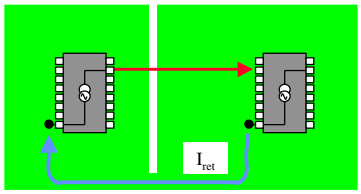
4

The effect of a discontinuity in I_{ret}

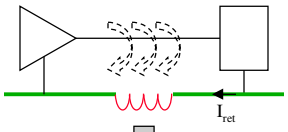


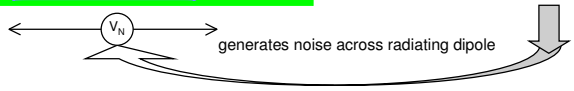
No split: high mutual inductance, low ground inductance





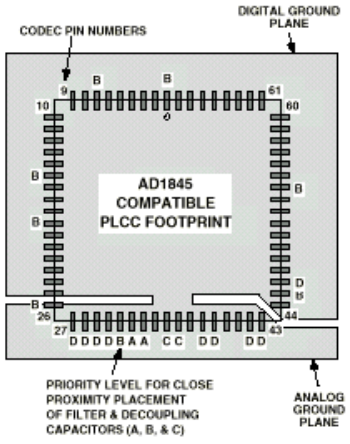
Extra return path adds ground inductance





5

Advice to split



Example

"...This layout separates the analog and digital ground planes with a 2 to 3 mm gap and connects them at one point beneath the codec with a single 3 to 4 mm wide link. ... The link between the planes, as close to the codec as possible, prevents any potential difference due to ESD or fault currents. Without the link, these currents could flow through the codec's substrate degrading performance. You should try to avoid running any digital or analog signal traces across the gap between the digital and analog planes…"

"… During PCB development, you may find it useful to provide removable links between the ground planes in several PCB locations, to permit debugging and testing for ground isolation…"

– Analog Devices AN-404

6

Why separate A & D ground planes?

- high frequency digital noise currents in DGND might pollute sensitive wideband circuits on AGND
  - common impedance coupling is a threat if there are mixed ground connections
- most application notes advise it
  - guards against inadequate layout practices in either analogue or digital section
- "we've always done it this way"
- if properly done, it gives good internal signal integrity, but it is a common cause of poor external EMC

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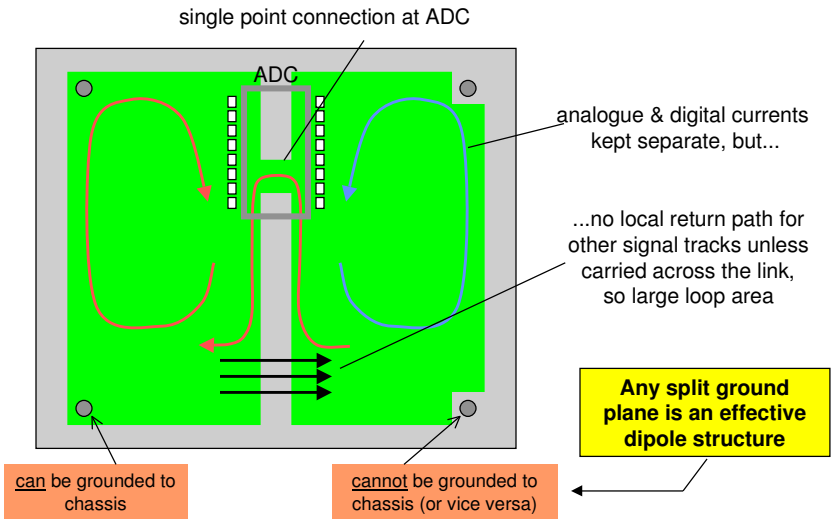
Effect of separate A & D ground planes



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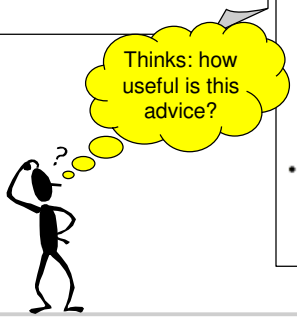
Multiple A-D devices

Question:

In my design I am using multiple codecs which are daisy chained together, and I was wondering about connecting the analog and digital planes. The data sheet has recommendations but I still need clarification on how to treat the power and ground planes in the case of using multiple codecs?

From Analog Devices Engineering Note EE-28



Answer:

The best method of determining where the planes get connected is as follows:

- Leave 3 places together on opposite sides of the planes.
- Use a direct link (small narrow trace or wire) or a ferrite bead to connect the two planes
- Of the 3 places to be linked, see which one gives you the best signal-to-noise ratio. Be prepared to do some measurements. To test for optimum performance, you can set up a test by generating a tone to the input of each codec, run an FFT on the DSP and view the results with a scope on the codec output. There is no solid proven method to yield the best result. The rule of thumb is to do an educated guess on which link between both planes gives you the best performance.
- Make sure that you only use one connection. Or else you are in danger of creating *ground loops*!

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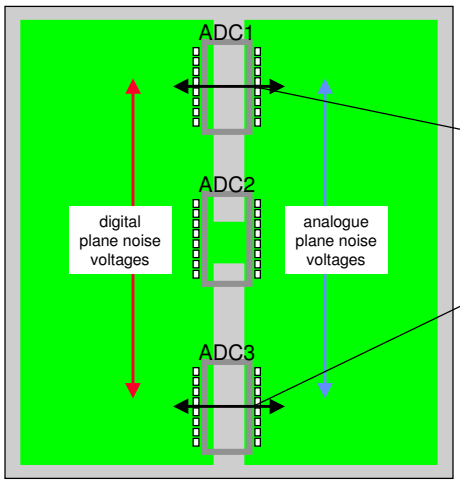
Multiple A-D packages: single link



Un-linked ADCs suffer excessive noise injection (both internal and externally caused) across the chip

Differences on-chip between AGND and DGND contribute to driving the radiating dipole

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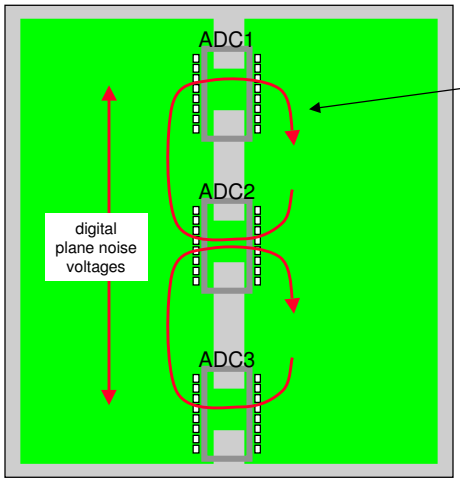
Multiple A-D packages: several links



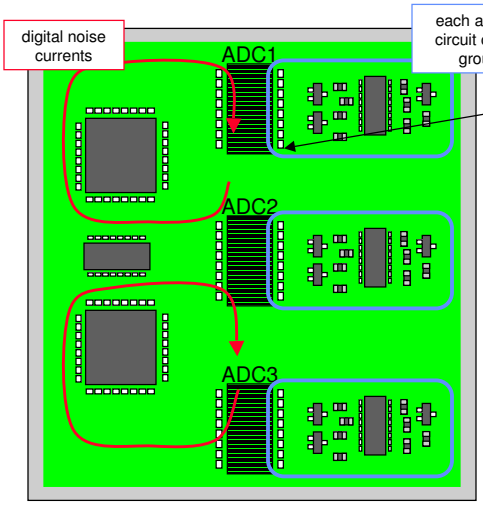
Each ADC is protected, but digital currents can now contaminate analogue circuits **(this is a ground loop)**

… but, will they, and, **how badly?**

… and anyway, implementing multiple links is nearly all the way to a full ground plane … **so why have splits at all?**

11

What happens with a single un-split GP?



- The solid structure gives no opportunity for an enhanced dipole
- but A and D ground currents could intermix, so…
- lay out the circuits as if there were separate ground planes: observe strict segmentation rules

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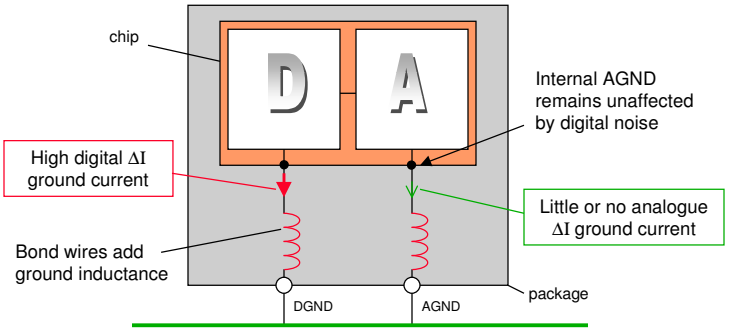
So why ...

- So, why do mixed-signal ICs have separate AGND and DGND pins if we're not going to use them?
- Because of bond wire inductance, that's why ...



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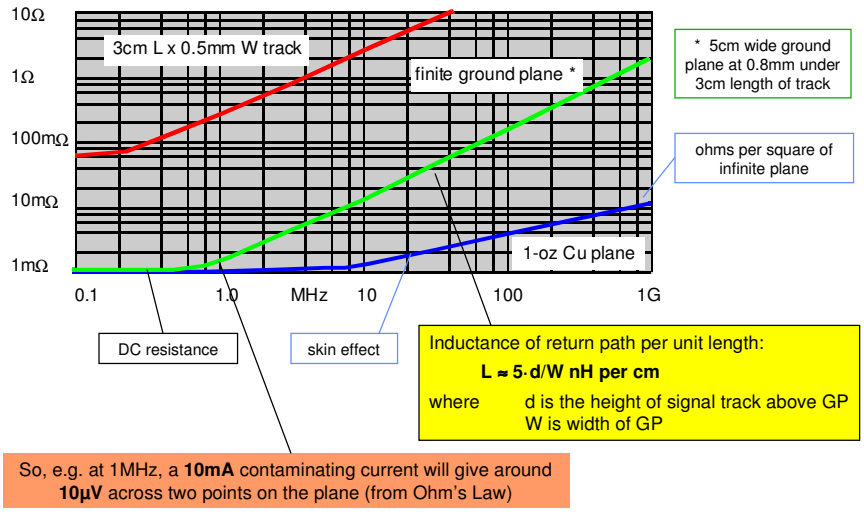
The impedance of ground planes



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Issue 2: Digital decoupling

EMAC services

Outline

- The purpose of decoupling
- Capacitor selection and layout
- Paralleling capacitors
- The planes as a transmission line
- Resistive damping
- Segmenting the power plane with inductors

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The purpose of decoupling

EMAC services

- ΔI currents from digital ICs cause ground bounce across power supply impedance
  - power source impedance is largely inductive
  - digital IC totem-pole switching gives high transient di/dt through power pins, and $\Delta V_{supply} \approx -L \cdot di/dt$
- decoupling capacitors stabilize the power rail voltage
  - voltage droop from an ideal capacitor $\Delta V = I \cdot t/C$
  - reduce radiated emissions since the loop area for high spectral content switching current is reduced

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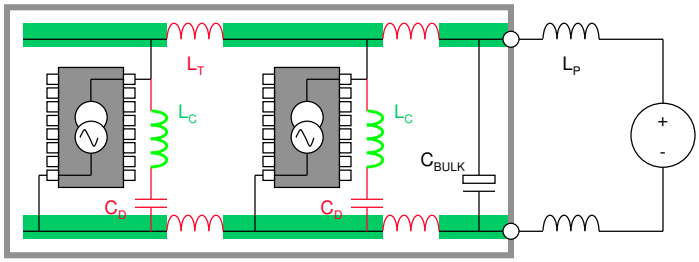
Decoupling regime vs frequency



LF/MF: power lead inductance L_P dominates, add C_{BULK}

HF: track inductance L_T dominates, add C_D

VHF: C_D lead inductance L_C becomes significant, so use power/ground planes to get distributed capacitance

UHF: power/ground planes become a transmission line ...

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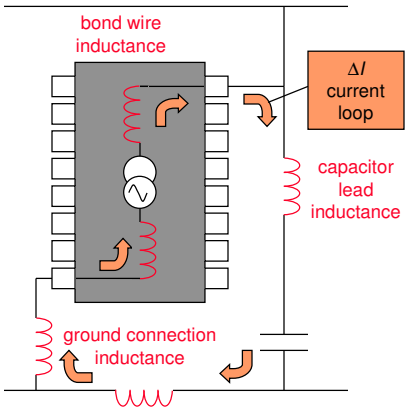
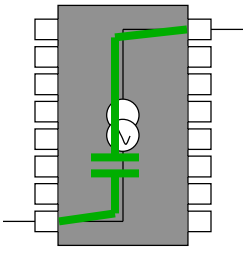
Capacitor positioning re. IC



- all local partial inductances compromise the effectiveness of C_D
- the best position for C_D is directly underneath the package to maximize mutual inductance of wires and traces



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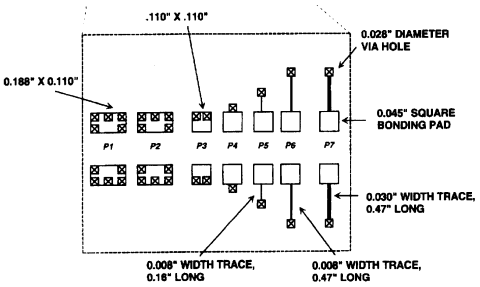
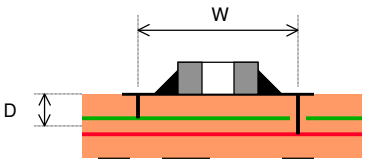
SM capacitor impedances (1)



Pad pattern	Resistance mΩ	Inductance nH
P2	12	0.61
P3	17	1.32
P4	22	2.00
P5	54	7.11
P6	95	15.7
P7	53	10.3



Via length D	Via spacing W	Inductance nH
0.263	0.34	11.0
0.223	0.21	7.2
0.173	0.21	5.7
0.163	0.14	4.2
0.057	0.22	2.2
0.037	0.17	1.2

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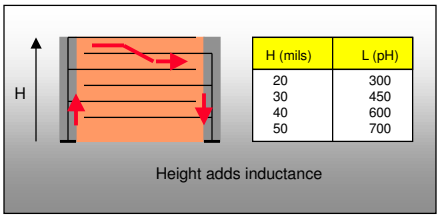
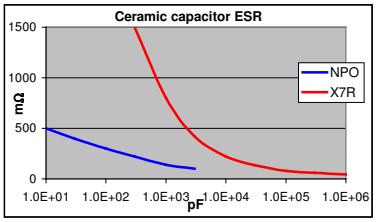
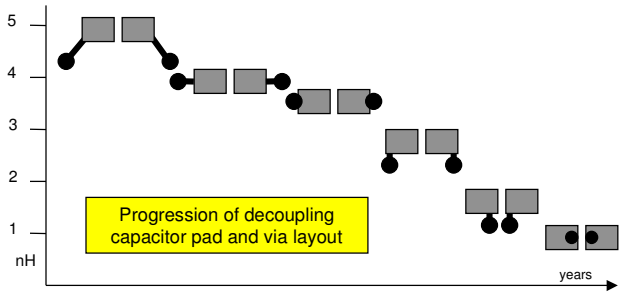
SM capacitor impedances (2)







Link to Murata capacitor data

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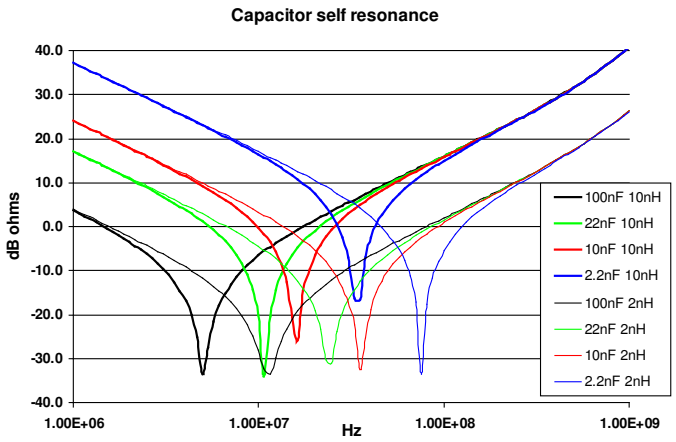
Capacitor value



- below self resonance, value is important – more capacitance = better decoupling
- above self resonance, value is unimportant – less inductance = better decoupling

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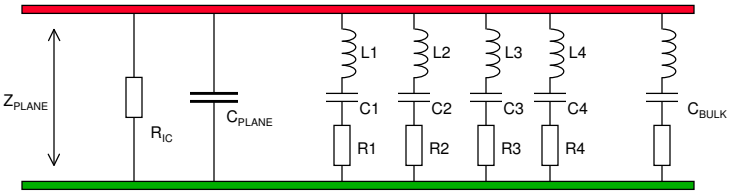
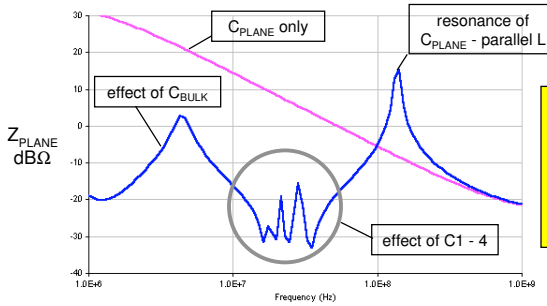
Multiple capacitors with P/G planes





Modelled with:
C1 - 4 = 22nF
L1 = 1nH, L2 = 2nH, L3 = 3nH, L4 = 4nH
C_{BULK} = 1µF, L = 15nH, R = 0.1Ω
R_{IC} = 50Ω
C_{PLANE} = 3nF

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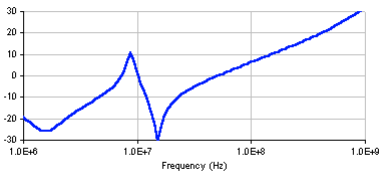
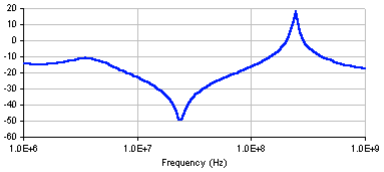
Parallel capacitors

- 2 capacitors of different values at one point are dangerous



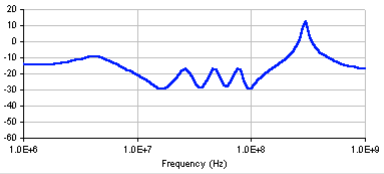
47nF // 1µF

- Multiple capacitors of the same value with power/ground planes are useful



9 x 22nF, 2nH

- Multiple capacitors of different values with power/ground planes give a wider low-Z bandwidth



Selection of different capacitors, 100nF to 220pF

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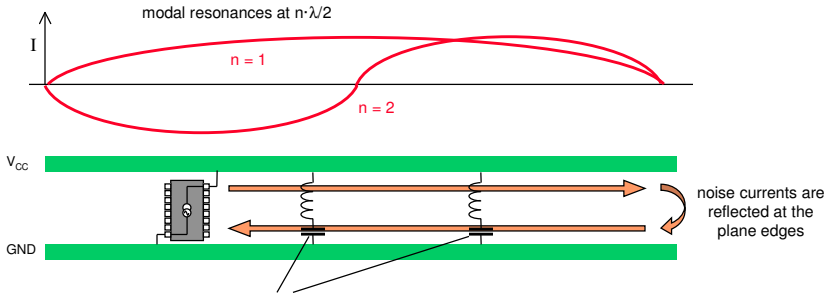
Power and ground planes as a TL

- The previous model assumed the board was small with respect to a wavelength (< $\lambda/10$)

but this is not true at UHF and above:
a quarter wavelength in FR4 ($\varepsilon_r \approx 4$) at 300MHz is **12.5cm**!

… the board then acts as a parallel-plate transmission line

$$\lambda = \frac{3 \cdot 10^8}{\sqrt{\varepsilon_r} \cdot \text{frequency}}$$



decoupling capacitors re-tune the resonances but don't eliminate them

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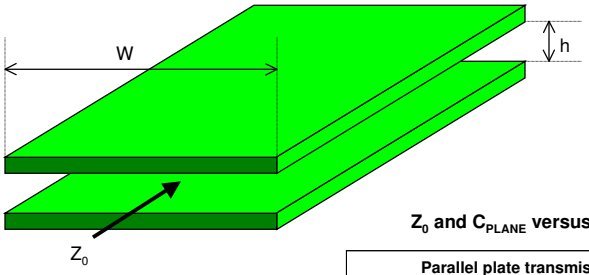
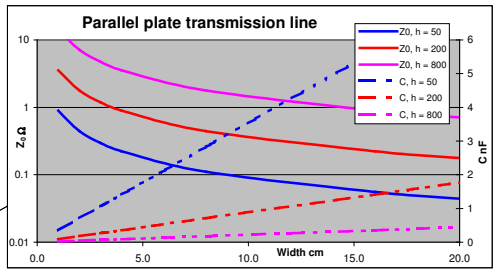
Transmission line impedance



$$Z_0 = 120 \cdot \pi \cdot \frac{h}{\sqrt{\varepsilon_r} \cdot W}$$

$$C\ (pF) = 0.0885 \cdot \frac{A\ (cm^2)}{h\ (cm)}$$

Z_0 and C_{PLANE} versus width and separation



For h = 50, 200 and 800 µm; capacitance for 20cm long line

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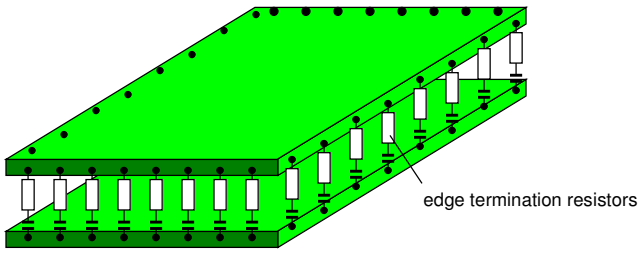
Dissipative edge termination

- effect of decoupling ESL is to re-tune plane resonances
- effect of decoupling ESR is to damp resonance and reduce Z_0
- because power plane Z_0 is low, a lot of capacitors are needed
- resonances can be reduced independently by adding resistance at the plane edges, across the planes (with DC blocking)
- resistance must be very low ESL and match Z_0, but not perfectly



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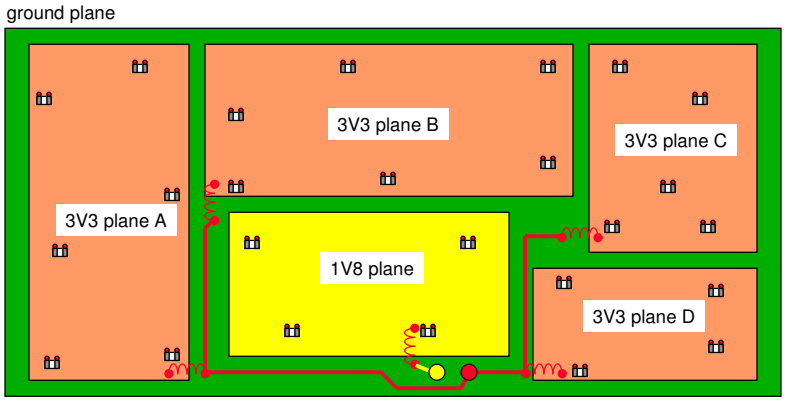
Segmenting the power plane



- splitting the power plane(s) (not the ground plane) into several segments, each decoupled by a choke, creates “islands” for noisy or sensitive circuits and reduces the impact of plane resonances

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Conclusions

- consider decoupling regimes for each part of the spectrum
- include capacitor stray inductance in all considerations
- at VHF, package and via inductance is more important than value
  - decoupling capacitor value and position can be modelled with a circuit simulator
- at UHF, board resonances are significant and can only be dealt with by resistive damping or segmentation
  - decoupling capacitor, damping resistor and IC positioning can be modelled by treating the plane as a network of distributed transmission lines

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Issue 3: Mode conversion in interface filters

EMAC services

Outline

- The purpose of an interface filter
- Typical circuits
- Model equivalent circuit for conducted immunity
- The problem of CM to DM conversion
- Some results and inferences

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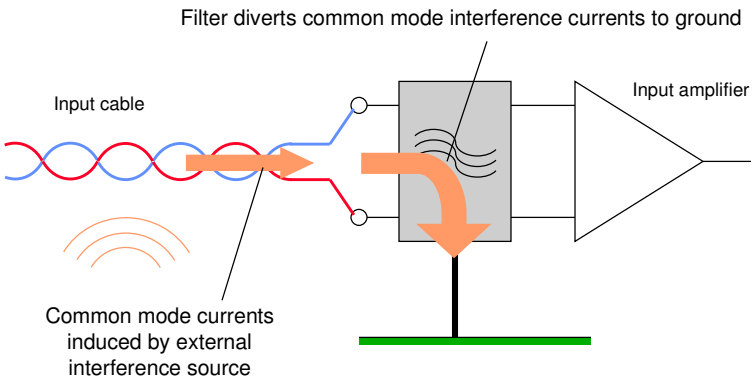
The purpose of an interface filter



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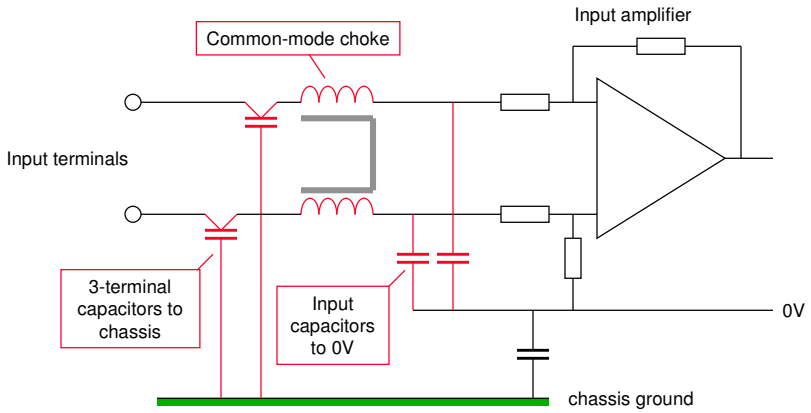
Typical filter circuit



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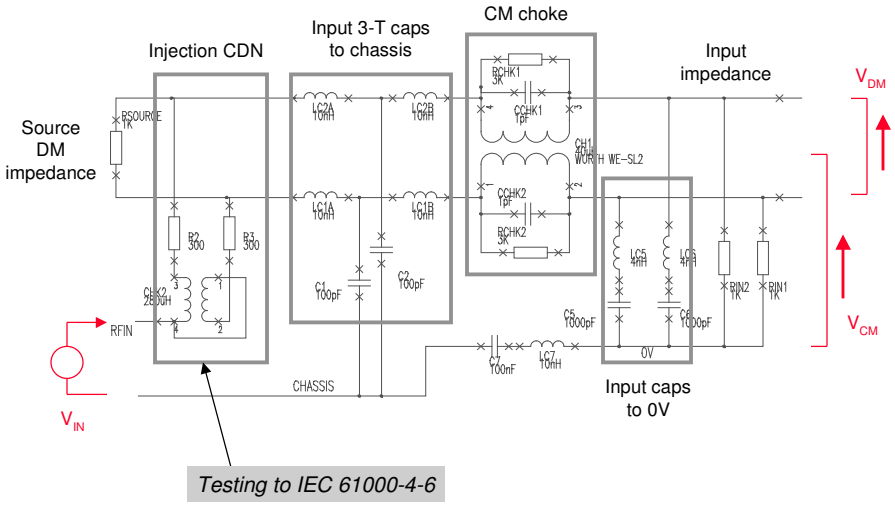
The equivalent circuit model



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Conversion from CM to DM

- If all the components (R, C and L) in the two halves of the differential circuit are exactly balanced, there is no CM-to-DM conversion:

$$|V_{DM}|/|V_{CM}| = 0$$

- but if there is any imbalance in any component in the two halves of the circuit, some differential mode voltage results:

$$|V_{DM}|/|V_{CM}| > 0$$

- the most likely source of imbalance is in the capacitor values, which can easily be ±20%

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Modelling

- The following graphs show model results for the previous equivalent circuit:
  - transfer function versus frequency, 100kHz – 100MHz
  - for differential mode (V_{DM}/V_{IN})
  - and common mode (V_{CM}/V_{IN}) (first slide only)
- for different conditions of balance and unbalance in various components in the equivalent circuit

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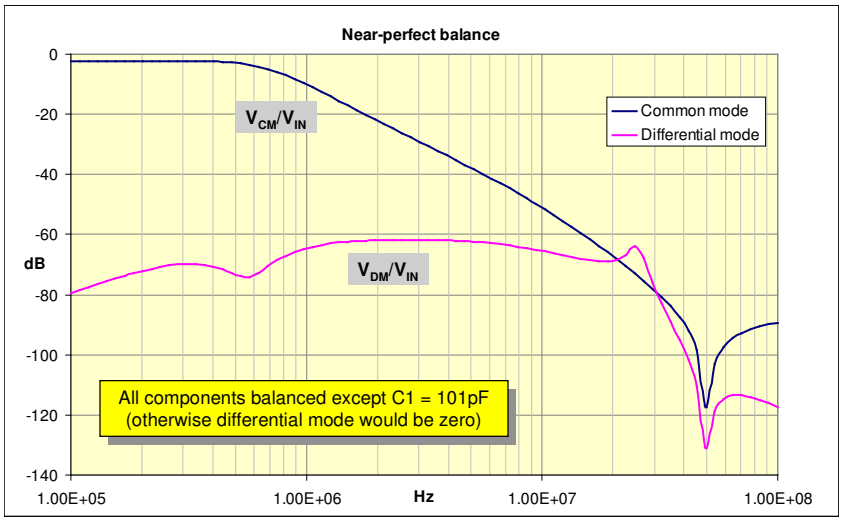
Model results: initial assumptions



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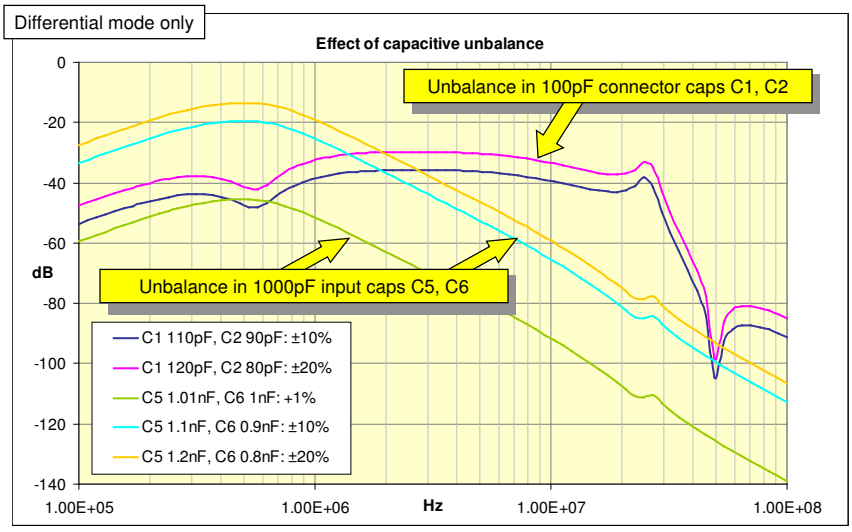
Model results: capacitive unbalance



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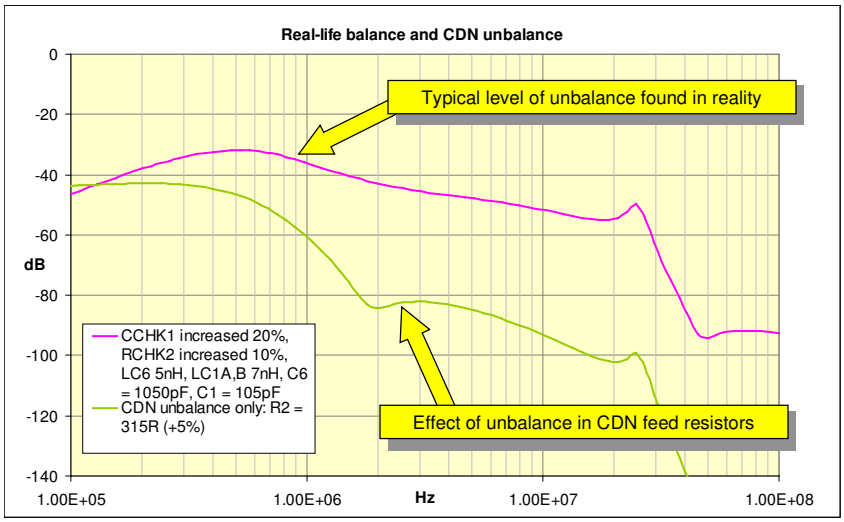
Model results: real life



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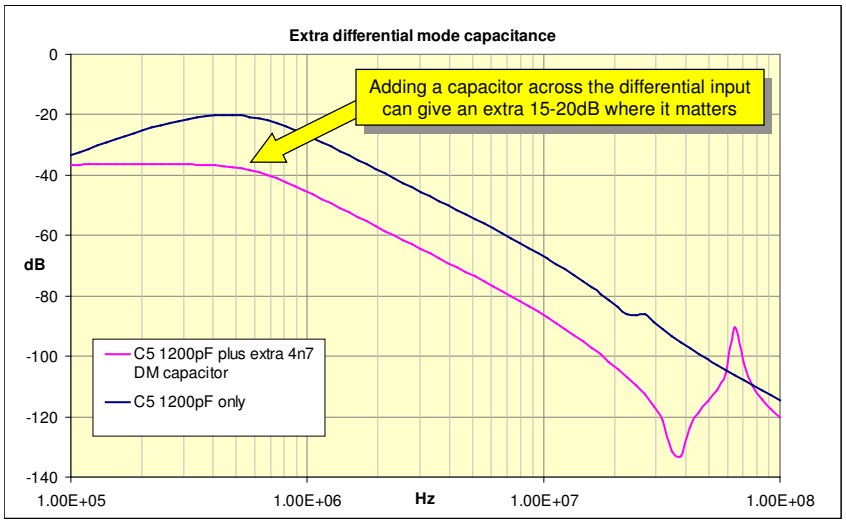
Model results: mitigation



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Conclusions

- Modelling shows that you have to be careful about imbalance in differential interface circuits, especially related to capacitor value tolerances
- Common mode attenuation is easily achievable but common to differential mode conversion may be significant
- Modelling the circuit to adjust the values is easy:

YOU CAN DO THIS AT HOME, KIDS!

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NEEDS 2006 workshop

End

Thanks for your attention!

Consultancy and training in electromagnetic compatibility

e-mail timw@elmac.co.uk web www.elmac.co.uk phone +44 (0)1929 558279

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