Application Report
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Interfacing the 3-V MSP430 to 5-V Circuits

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ABSTRACT

The interfacing of the 3-V MSP430x1xx and MSP430x4xx microcontroller families to circuits with a supply of 5 V or higher is shown. Input, output and I/O interfaces are given and explained. Worst-case design equations are provided, where necessary. Some simple power supplies generating both voltages are shown, too.

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1 Introduction

The modern MSP430s, such as the members of the MSP430x1xx family and the MSP430x4xx family, are available for the supply voltage range from 1.8 V to 3.6 V only. This is due to the manufacturing process used, and has the advantage of drawing even less current than with the 5-V supply used by the MSP430C3xx family.

If an interface to a 5-V system—or a system with an even higher voltage—is necessary, it can result in difficulties. This application report shows and explains 5-V interfaces for the MSP430 inputs, outputs and I/Os. Figure 1 shows examples of input, output, and I/O interfaces. The gray shaded boxes are the topic of this application report.

Note: In the following, the term MSP430 stands for the members of the MSP430x1xx and the MSP430x4xx families.

Note: The given formulas for the external supply voltage $V_{(sys)}$ also can be used for higher voltages than 5 V. They are useful for any external voltage, e.g., $V_{(sys)}$ = 12 V.

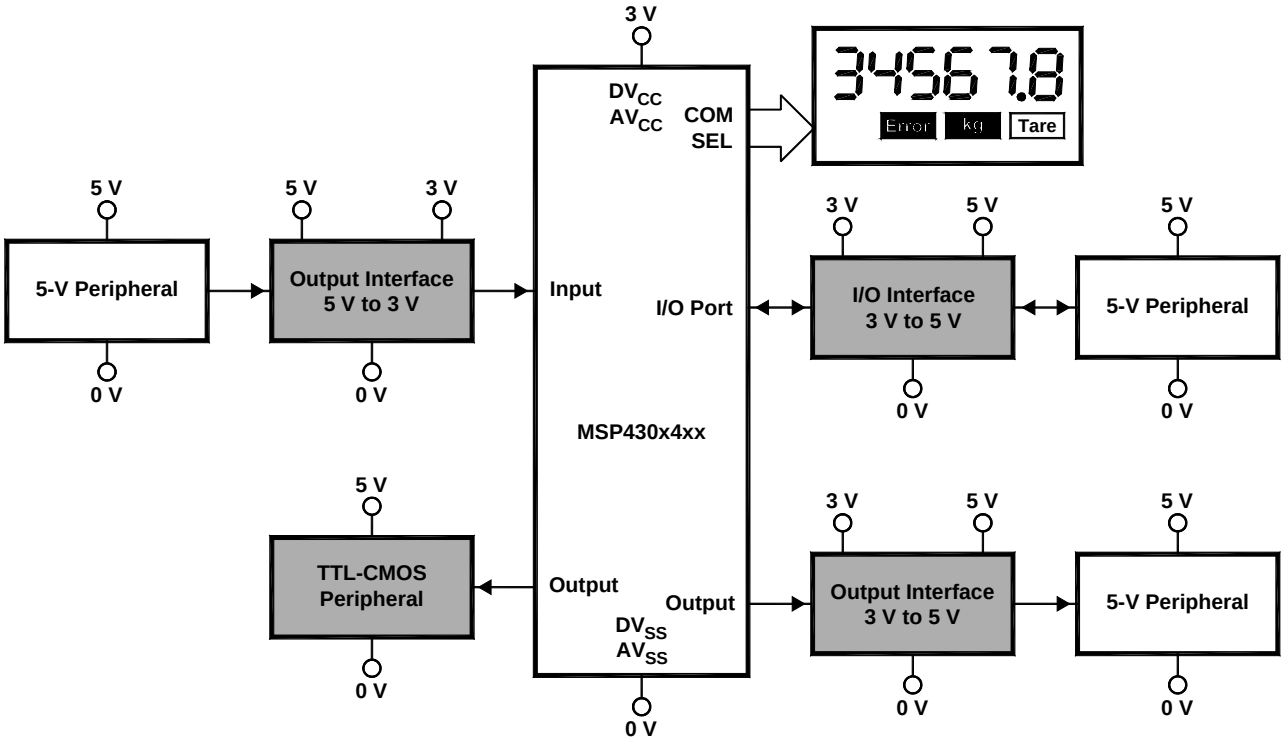

Figure 1. Interfaces Between the 3-V MSP430 and 5-V Systems

With the worst-case equations, the following simplifications are used for the calculation with small values of *ax* (like for the tolerance *p*):

$$\frac{1}{1+a_x} \approx (1-a_x) \qquad \frac{1}{1-a_x} \approx (1+a_x) \qquad \frac{1+a_x}{1-a_x} \approx (1+2a_x) \qquad \frac{1-a_x}{1+a_x} \approx (1-2a_x)$$

The resulting errors can be neglected if $|a_x| < 0.1$.

2 Definitions

2.1 MSP430 Specification Values

The numeric values for the worst-case design equations are taken from [4]. The indicated values are for DV_{CC} = 3 V:

$DV_{CC(min)}$	Minimum digital supply voltage of the MSP430x4xx	1.8 V
$DV_{CC(max)}$	Maximum digital supply voltage of the MSP430x4xx	3.6 V
$V_{IT(max)}$	Maximum high input threshold voltage of an MSP430 port	1.9 V
$V_{IT(min)}$	Minimum low input threshold voltage of an MSP430 port	0.9 V
$V_{OH(min)}$	Minimum high port output voltage @ I_O = –1.5 mA	DV_{CC} – 0.25 V
$V_{OL(max)}$	Maximum low port output voltage @ I_O = 1.5 mA	DV_{SS} + 0.25 V
I_{lkg}	Leakage current of an MSP430 input	±50 nA
	Absolute maximum current through the protection diodes of any MSP430 terminal (V_I < – 0.3 V or V_I > V_{CC}+ 0.3 V)	±2 mA

Note: The output impedance $r_{DS(on)}$ of an MSP430x4xx output is not taken into account, due to the choice of high resistor values with the design equations. The output impedance $r_{DS(on)}$ (max. 167 Ω) is very small compared to the resistors used.

2.2 External System Definitions

$V_{(sys)}$	Supply voltage of the external system	[V]
$V_{(sysH)}$	High output voltage from the external system	[V]
$V_{(sysL)}$	Low output voltage from the external system	[V]
$V_{(sys+)}$	High input voltage of the external system	[V]
p	Tolerance of the interface resistors	[%]
$DV_{CC(min)}$	Minimum supply voltage for the MSP430 with a DV_{CC} = 3.0 V ±10% (3.0 V × 0.9 = 2.7 V)	[V]

3 Input Interfaces

The input interfaces shown are primarily intended for the interfacing between 5-V and 3-V systems. However, they also can be used for external voltages higher than 5 V, e.g., the interfacing of a 12-V signal to the MSP430 input.

3.1 Resistor-Divider Input Interfaces

An external, digital input voltage $V_{I(sys)}$ is connected to the MSP430. The worst case equations for the two resistors R1 and R2 shown in Figure 2 are:

$$\frac{R1}{R2} < \frac{V_{(sysH)}\,\min - V_{IT(max)}}{V_{IT(max)} \times (1 + 2p)} \quad \text{and} \quad \frac{R1}{R2} > \frac{V_{(sysL)}\,\max - V_{IT(min)}}{V_{IT(min)} \times (1 - 2p)} \quad \text{and} \quad R1 \,||\, R2 << \frac{DV_{CC}}{|\,I_{lkg}\,|}$$

The first two equations ensure that the input voltage $V_{I(430)}$ at the MSP430 input is above (when $V_{I(sys)}$ is high) or below (when $V_{I(sys)}$ is low) the worst case input threshold voltages. The third equation ensures that the leakage current I_{lkg} of the input does not influence the voltage $V_{I(430)}$.

To avoid current into the input protection diodes of the MSP430 it is necessary that:

$$V_{(sysH)}\,\max \times \frac{R2\,\max}{R1\,\min + R2\,\max} < DV_{CC(min)} + 0.3 \quad \text{and} \quad V_{(sysL)}\,\min \times \frac{R2\,\min}{R1\,\max + R2\,\min} > -0.3$$

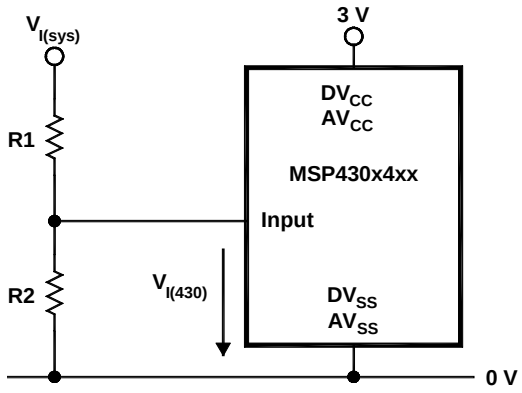

Figure 2. Resistor Input Interface From 5 V to the MSP430

EXAMPLE: the two input voltages from the system are $V_{(sysH)}$ = 5.0 V ±10% and

$V_{(sysL)}$ = 0.5 V ±0.5 V. The resistor tolerance is p = ±5%. The minimum supply voltage of the

MSP430 in this example is $DV_{CC(min)}$ = 2.7 V (3.0 V – 10%).

With the above specifications for the threshold voltages $V_{IT(max)}$ and $V_{IT(min)}$ this leads to the condition for the input voltage $V_{(sysH)}$min:

$$\frac{R1}{R2} < \frac{V_{(sysH)}\,min - V_{IT(max)}}{V_{IT(max)} \times (1 + 2p)} = \frac{4.5\,V - 1.9\,V}{1.9\,V \times (1 + 0.1)} \rightarrow \frac{R1}{R2} < 1.244$$

The condition for the low input voltage $V_{(sysL)}max$ is:

$$\frac{R1}{R2} > \frac{V_{(sysL)}\,max - V_{IT(min)}}{V_{IT(min)} \times (1 - 2p)} > \frac{1.0\,V - 0.9\,V}{0.9\,V \times (1 - 0.1)} \rightarrow \frac{R1}{R2} > 0.1234$$

To ensure negligible influence of the leakage current I_{lkg}:

$$R1 \,||\, R2 << \frac{DV_{CC}}{|I_{lkg}|} = \frac{3\,V}{|\pm 50\,nA|} \rightarrow R1 \,||\, R2 << 60\,M\Omega$$

The three design equations above allow a wide range for R1 and R2. If R1/R2 is chosen to be 1.0 and R1||R2 to be 600 kΩ, then R1 = 1.2 MΩ and R2 = 1.2 MΩ.

To avoid current into the input protection diodes of the MSP430 it is necessary:

$$V_{(sysH)}\,max \times \frac{R2\,max}{R1\,min + R2\,max} < DV_{CC(min)} + 0.3 \quad \text{and} \quad V_{(sysL)}\,min \times \frac{R2\,min}{R1_{max} + R2\,min} > -0.3$$

$$5.5\,V \times \frac{1.26\,M\Omega}{1.14\,M\Omega + 1.26\,M\Omega} < 2.7\,V + 0.3 \rightarrow 2.8875\,V < 3.0\,V$$ the condition is true.

$$0.0\,V \times \frac{1.14\,M\Omega}{1.26\,M\Omega + 1.14\,M\Omega} > -0.3\,V \rightarrow +0.0\,V > -0.3\,V$$ the condition is also true.

The last two equations are not important if the current into the MSP430 input is far below ±2 mA (the absolute maximum rating value for an input current). This is the case for the example given: R1||R2 = 600 kΩ.

The above mentioned design equations are valid for the following MSP430 terminals, if switched to the input direction:

- All I/O ports (ports P1 to P6)
- Crystal inputs XIN and XT2IN: $V_{IL(X)}max = 0.2 \times DV_{CC}$, $V_{IH(X)}min = 0.8 \times DV_{CC}$
- RST/NMI input: $V_{IL}max = DV_{SS} + 0.6$ V, $V_{IH}min = 0.8 \times DV_{CC}$
- Comparator_A inputs CA0 and CA1
- UART/SPI inputs URXDx, SOMIx, SIMOx, UCLK
- Timer_A inputs TACLK, TA0 to TA2

- Timer_B inputs TBCLK, TB0 to TB6
- ADC12 inputs: the sample time $t_{(sample)}$ must be adapted to the impedance R1||R2 of the resistor divider. For more information, see the ADC12 chapter of [2] or [3].

3.2 Transistor Input Interface

The transistor-input interface is a very simple interface that can adapt many external systems to the MSP430 family. Figure 3 shows an example for an inverting input buffer. The resistor R_C can be switched off by an output to save current during low-power mode 3.

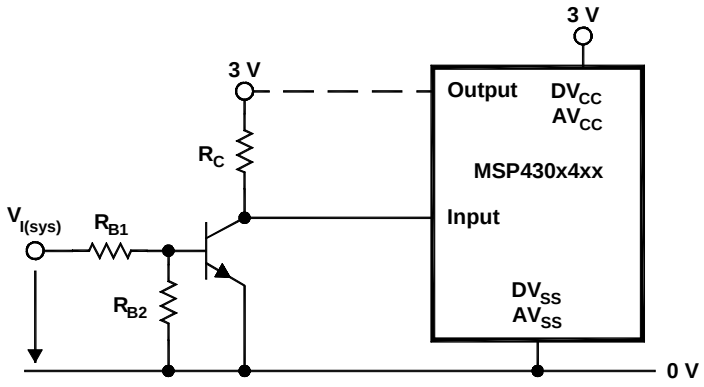

Figure 3. Transistor Input Interface From a 5-V Environment

The design equations for the resistors R_C, R_{B1} and R_{B2} are:

$$R_C < \frac{DV_{CC(min)} - V_{IT(max)}}{(1+p) \times (I_{lkg} + I_{lkg(Tr)})}$$ ensures high potential at the MSP430 with leakage currents

$$\frac{R_{B1}}{R_{B2}} > \left(\frac{V_{(sysL)}\,max}{V_{BE(off)}} - 1 \right) \times (1+2p)$$ ensures turnoff of the transistor for input voltage $V_{(sysL)}$max

The third equation ensures the turnon of the transistor for the input voltage $V_{(sysH)}$min:

$$R_{B1} < \frac{V_{(sysH)}\,min - V_{BE(on)} \times \left(1 + \frac{R_{B1}}{R_{B2}} \times (1+2p)\right)}{DV_{CC(max)}} \times \beta\,min \times R_C\,min$$

Where $V_{BE(off)}$ Transistor base-emitter voltage for secure turnoff [V]

$V_{BE(on)}$ Transistor base-emitter voltage for secure turnon [V]

β Current amplification of the transistor

$I_{lkg(Tr)}$ Leakage current of the transistor [A]

Example: Input voltage $V_{I(sys)}$ is connected to an MSP430 input with $I_{lkg} = \pm 50$ nA. The minimum high-input level $V_{(sysH)}$min = 4.5 V, the maximum low-input level $V_{(sysL)}$max = 0.7 V. The resistor tolerance of all resistors is p = ±5%. The supply voltage is DV_{CC} = 3 V ±10%. The transistor properties are $V_{BE(on)}$ = 0.75 V, $V_{BE(off)}$ = 0.2 V, βmin = 100, $I_{lkg(Tr)}$ = 10 nA.

The maximum nominal value for R_C is:

$$R_C < \frac{DV_{CC(min)} - V_{IT(max)}}{(1+p)\times(I_{lkg} + I_{lkg(Tr)})} = \frac{2.7\,V - 1.9\,V}{(1+0.05)\times(50\,nA + 10\,nA)} = 12.7\,M\Omega \qquad \text{chosen } R_C = 2\ M\Omega$$

The minimum ratio for the nominal values of R_{B1} and R_{B2} is:

$$\frac{R_{B1}}{R_{B2}} > \left(\frac{V_{(sysL)}\,max}{V_{BE(off)}} - 1\right)\times(1+2p) = \left(\frac{0.7\,V}{0.2\,V} - 1\right)\times(1+0.1) = 2.75$$

The maximum nominal value for R_{B1} is:

$$R_{B1} < \frac{V_{(sysH)}\,min - V_{BE(on)} \times \left(1 + \frac{R_{B1}}{R_{B2}}\times(1+2p)\right)}{DV_{CC(max)}} \times \beta\,min \times R_C\,min$$

$$R_{B1} < \frac{4.5\,V - 0.75\,V \times [1 + 2.75\times(1+0.1)]}{DV_{CC(max)}} \times 100 \times 2\,M\Omega \times (1-0.05) = 85.3\,M\Omega \qquad \text{chosen } R_{B1} = 39\ M\Omega$$

With the value 39 MΩ for R_{B1} the resistor R_{B2} gets:

$$R_{B2} < \frac{R_{B1}}{2.75} = \frac{39\,M\Omega}{2.75} = 14.18\,M\Omega \qquad \text{chosen } R_{B2} = 10\ M\Omega$$

3.3 Op-Amp Input Interface

Op amps for the input interface are the best choice, if they are needed anyway for the system (as an integrator, comparator, amplifier, DAC, etc.). For the TLC27L4 it is necessary to limit the input voltages to a maximum of V_{DD} + 0.3 V. The minimum supply voltage of the TLC27L4 $V_{CC(min)}$ = 3 V.

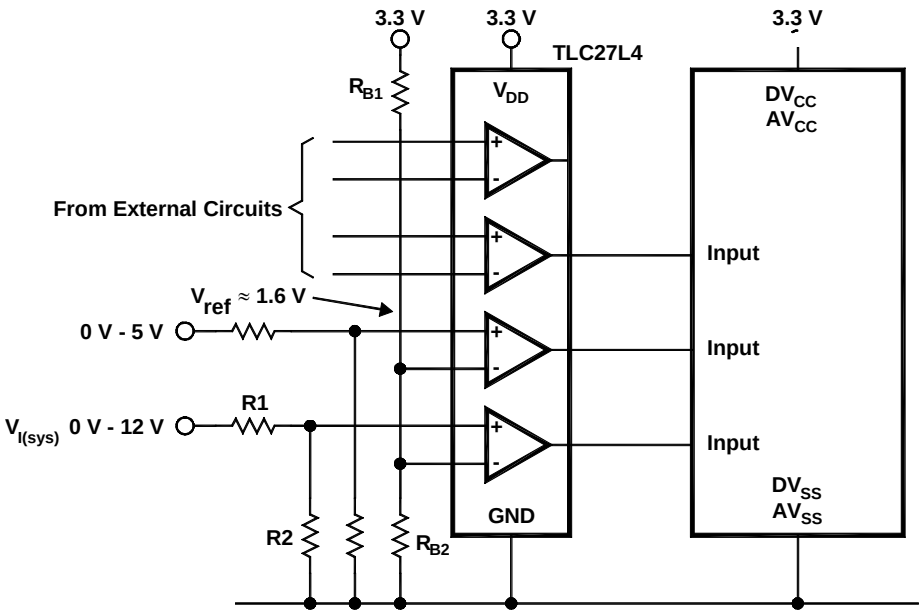

Figure 4. Input Interfaces With Op Amps

The worst case equations for the two resistors R1 and R2 shown in Figure 4 is:

$$\frac{R1}{R2} < \frac{V_{(sysH)}\,\min - V_{ref(max)}}{V_{ref(max)} \times (1+2p)} \quad \text{and} \quad \frac{R1}{R2} > \frac{V_{(sysL)}\,\max - V_{ref(min)}}{V_{ref(min)} \times (1-2p)} \quad \text{and} \quad R1 \,||\, R2 << \frac{DV_{CC}}{|I_{lkg}|}$$

where $V_{ref(max)} = DV_{CC(max)} \times \frac{R_{B2}\,\max}{R_{B1}\,\min + R_{B2}\,\max}$ and $V_{ref(min)} = DV_{CC(min)} \times \frac{R_{B2}\,\min}{R_{B1}\,\max + R_{B2}\,\min}$

A calculation example is given in *Resistor Divider Input Interface*, Section 3.1.

3.4 ULN2003A Input Interface

On the left side of Figure 7, three ULN2003A buffers are used for the input interfacing to 5-V and 12-V systems. The series resistor R_V (p = ±5%) for the 12-V input signal ($V_{(sysH)}$min = 11 V) is:

$$R_V < \frac{V_{(sysH)}\,\min - V_{I(on)}\,\min}{(1+p) \times I_{I(on)}\,\max} = \frac{11\,V - 2.4\,V}{1.05 \times 1.35\,mA} \rightarrow R_V\,\max < 6.06\,k\Omega \qquad \text{chosen } R_V = 6.0\ k\Omega$$

The pullup resistor R_p at the MSP430 input is:

$$R_p < \frac{V_{CC} - V_{IT(max)}}{(1+p) \times I_{CE}\,\max} = \frac{3\,V - 1.9\,V}{1.05 \times 50\,\mu A} \rightarrow R_{p\,max} < 20.9\,k\Omega \qquad \text{chosen } R_p = 20\ k\Omega$$

To avoid current consumption, the resistors R_p are switched to DV_{CC} only when necessary.

3.5 Integrated-Circuit Input Interface

For a 5-V to 3.3-V input interface, any CMOS-circuit can be used which fulfills the following two conditions:

- It is built for a supply voltage of 3.3 V or lower.
- It is explicitly allowed to use input voltages higher than 3.3 V.

The AHC and LVC families fulfill both conditions. They share the 3.3-V supply of the MSP430.

Note: A check is necessary to determine if an input voltage V_I higher than the 3.3-V supply is really allowed. This means, in the data sheet under *absolute maximum ratings* the following entry appears:

Input voltage range VB_I……0.5 V to 7 V

And not as usual with other CMOS circuits:

Input voltage range V_I……0.5 V to V_{CC}+0.5 V

or

Input clamp current I_{IK} (V_I < 0 or V_I > V_{CC}) …±20 mA

3.6 Analog Input Interface

The same resistor divider solution as shown for the digital interfaces above is possible for the analog ADC12 inputs. Figure 5 shows the connection of a 5-V Hall-sensor current interface to the ADC12 input Ax. The worst case equations for the resistor divider can be seen in *Resistor Divider Input Interfaces,* Section 3.1.

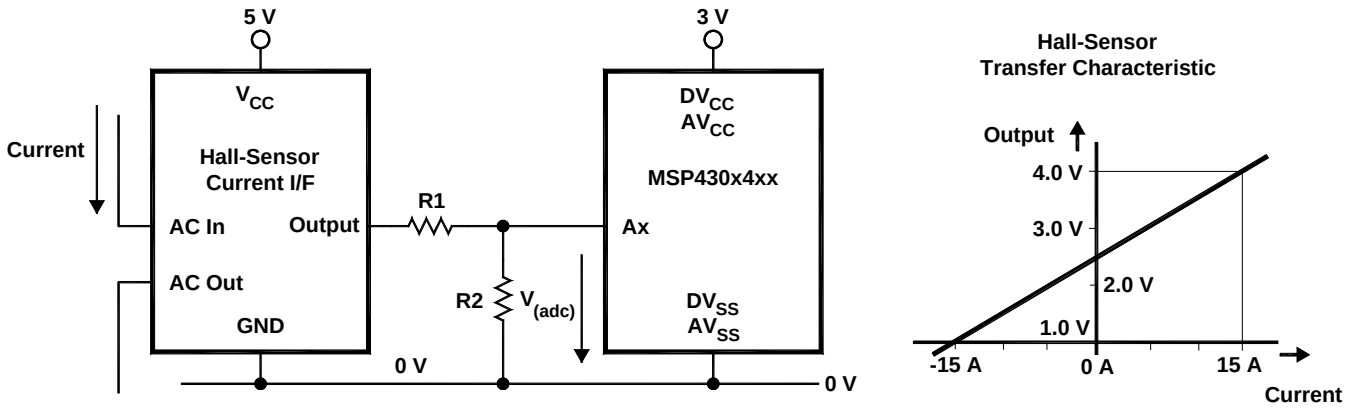

Figure 5. Analog ADC12 Input Interface From 5 V to 3 V

If the external peripheral cannot deliver the current for the resistor divider, a unity-gain op amp can be placed between the peripheral output and resistor R1.

The ADC12 sample time $t_{(sample)}$ must be adapted to the impedance R1||R2 of the resistor divider. For more information, see the ADC12 chapter of [2] or [3].

4 Output Interfaces

No interface is needed for LCDs and for passive sensors. They are directly connected to the MSP430 in the usual way. See [2].

4.1 Transistor Output Interface

A simple interface to systems with higher supplies than 3 V is shown in Figure 6. The transistor load R_L can be nearly anything: resistors, fans, heating coils, relays, etc. The base resistor R_B can be calculated with the equation:

$$R_B < \frac{R_L\,\text{min} \times \beta\,\text{min} \times \left(V_{OH(\text{min})} - V_{BE(on)}\right)}{(1+p) \times V_{(sys)}\,\text{max}}$$

Where	$R_L$min	Minimum load resistor	[Ω]
	βmin	Minimum current amplification of the transistor	
	$V_{(sys)}$max	Maximum supply voltage of the external system	[V]
	$V_{BE(on)}$	Transistor base-emitter voltage for turnon	[V]

Due to the low output voltage of the MSP430 port, no resistor from the transistor base to 0 V is necessary.

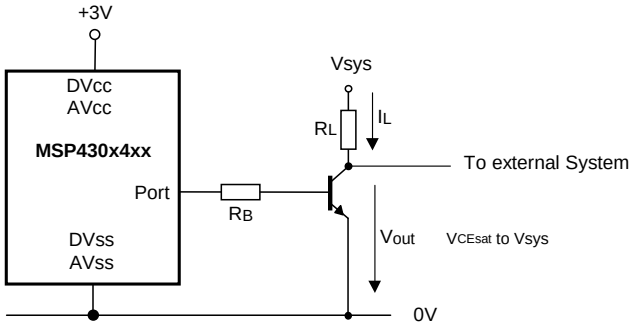

Figure 6. Transistor Output Interface to a 5-V Environment

Example: a load R_L = 100 Ω ±3% is connected to $V_{(sys)}$ = 5 V ±10%. The resistor tolerance of R_B is p = ±10%. The minimum supply voltage in this example is $DV_{CC(min)}$ = 2.7 V (3.0 V – 10%). The transistor properties are $V_{BE(on)}$ = 0.7 V and βmin = 100.

$$R_B < \frac{100\Omega \times (1-0.03) \times 100 \times (2.7\text{V} - 0.25\text{V} - 0.7\text{V})}{(1+0.1) \times 5\text{V} \times (1+0.1)} \quad \rightarrow \quad R_B < 2805.8\Omega \qquad \text{chosen } R_B = 2.7\ \text{k}\Omega$$

4.2 Interface to CMOS-TTL Inputs

All integrated circuits with TTL-CMOS inputs can be used as output circuits for the MSP430x1xx and MSP430x4xx. The input voltages of these ICs are:

V_{IH}min	Minimum high-level input voltage	2.0 V
V_{IL}max	Maximum low-level input voltage	0.8 V

Both voltages are within the output voltage range of an MSP430 output: DV_{CC} – 0.25 V and DV_{SS} + 0.25 V for DV_{CC} = 2.7 V to 3.6 V. No interface circuit is necessary; the TTL-CMOS ICs contain the 3-V/5-V interface on-chip.

4.3 Interface to ULN2003 Inputs

For high output currents or to drive up to seven 5-V output ports, the ULN2003A output buffer can be used. The properties of the ULN2003A are:

$I_L$max	Maximum output current	500 mA
$V_L$max	Maximum output voltage	50 V
$V_{I(on)}$max	Maximum input voltage (I_L = 200 mA)	2.4 V
$I_{I(on)}$max	Maximum input current (V_I = 3.85 V)	1.35 mA
I_{CE}max	Maximum output leakage current (V_{CE} = 50 V)	50 μA

On the right side of Figure 7, the ULN2003A is used for the output buffering to 5-V and 12-V peripherals. The common free-wheeling diodes of the ULN2003A used for the 12-V peripherals do not influence the 5-V signals.

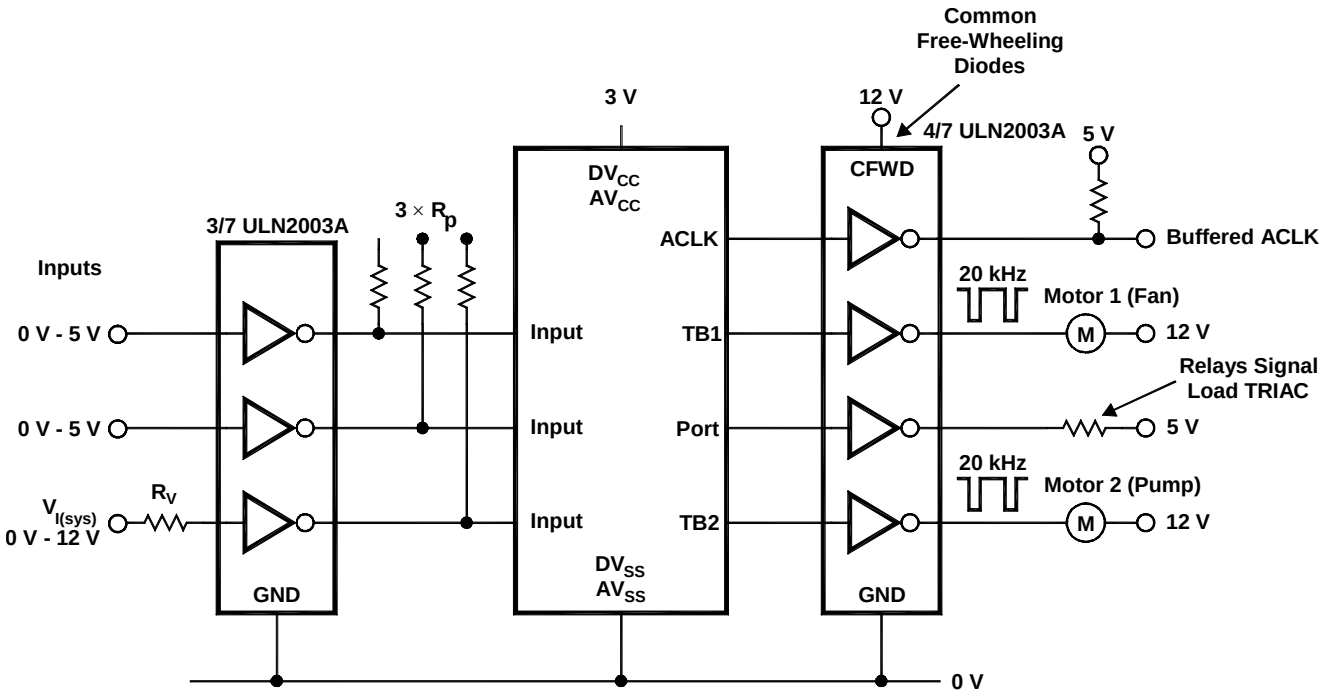

Figure 7. Interfaces With High-Current Output Buffers ULN2003

The input interface on the left side of Figure 7 is described in *ULN2003A Input Interface*, Section 3.4.

4.4 Op-Amp Output Interface

With the quad op amp TLC27L4, an interface to system voltages $V_{(sys)}$ of up to 16 V can be realized. The resistor divider at the inverting inputs of the TLC27L4 generates a voltage of approximately 1.5 V. The values for R_{B1} and R_{B2} must fulfill the equation:

$$R_{B1} \parallel R_{B2} << \frac{DV_{CC}}{\sum I_{lkg(Op)}} = \frac{3V}{4 \times 0.7nA} = 1.07G\Omega$$

This allows resistors with 10 MΩ resistance.

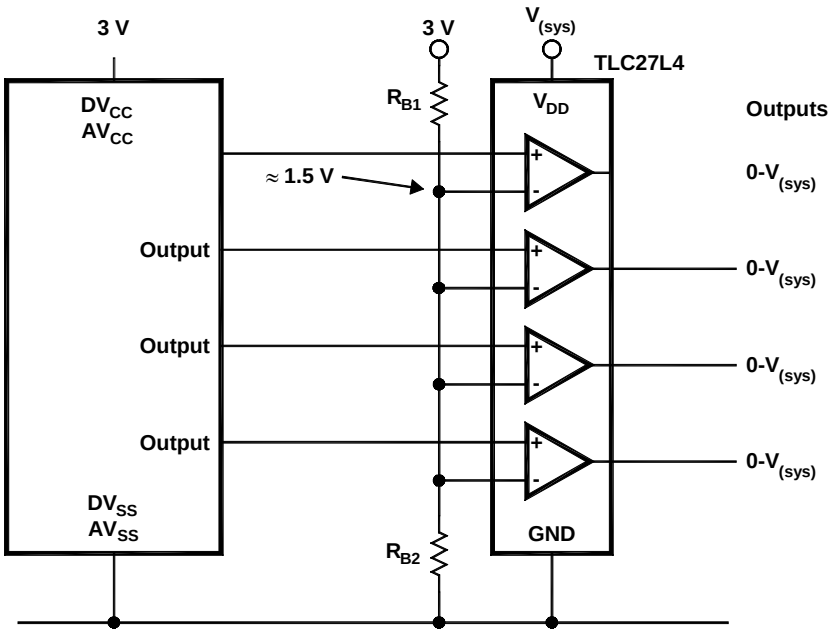

Figure 8. Output Interfaces With Op Amps

4.5 Integrated-Circuit Output Interface

Nearly all TTL-compatible ICs, such as the HCT and AHCT families, can be used for 3-V to 5-V output interfaces. The same is true for all bipolar circuits.

If the 5-V supply is switched off during the time when the 3-V supply is still on (e.g., during a power down of the 5-V supply as shown in Figure 11), then only circuits that do not have built-in ESD protection diodes can be used for the input to the V_{CC} connection. Otherwise, a current flows from the 3-V supply to ground via this protection diode. This means that only AHCT and bipolar circuits can be used in this case.

5 Bidirectional Interfaces

5.1 Simple, Bidirectional Op-Amp Interface

If true I/O performance is needed between the MSP430 and a 5-V system, then the interface circuit shown in Figure 9 can be used. The op amp works as a flip-flop: the I/O pin currently working as an output controls the state of this flip-flop. The other I/O pin must be an input.

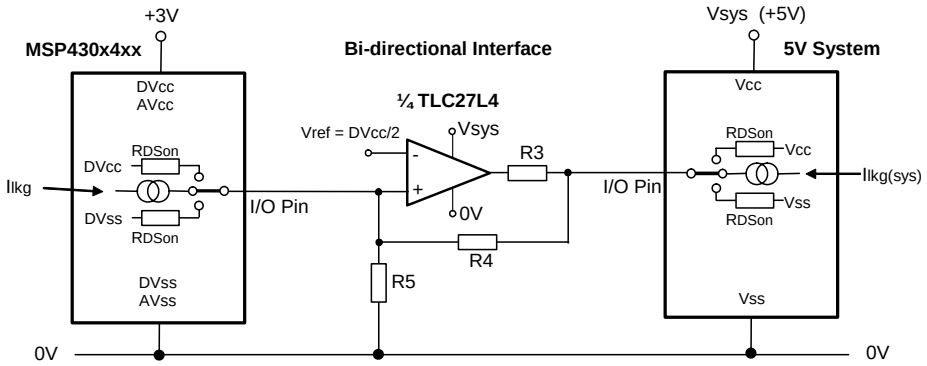

Figure 9. Bidirectional Interface Between 3-V and 5-V Systems

The worst-case design equations for the resistors R3, R4 and R5 are:

$$\frac{R4}{R5} < (1-2p)\times\left(\frac{V_{(sysH)}\,\min}{V_{ref(max)}}-1\right)$$ ensures a high level at the MSP430 input

$$\frac{R4}{R5} > (1+2p)\times\left(\frac{V_{(sysH)}\,\max}{DV_{CC(min)}}-1\right)$$ prevents voltages higher than DV_{CC} at the MSP430 input

The next equation ensures high level at the MSP430 input with the MSP430 and op amp leakage currents I_{lkg} and $I_{lkg(Op)}$:

$$R4 < \frac{V_{(sysH)}\,\min - V_{ref(max)}\times\left(1+\frac{R4}{R5}\times(1+2p)\right)}{\left(I_{lkg}+I_{lkg(Op)}\right)\times(1+p)}$$

The last equation ensures a high level at the external system input with its leakage current $I_{lkg(sys)}$:

$$R3 < \frac{V_{(sys)}\,\min - V_{(sys+)}\,\min}{(1+p)\times\left(I_{lkg(sys)}+\frac{V_{(sys+)}\,\min - V_{ref(min)}}{R4\times(1+p)}\right)}$$

Where	V_{ref}	Reference voltage for the input level decision	[V]
	I_{lkg}	Input leakage current of an MSP430 input	[A]
	$I_{lkg(Op)}$	Input leakage current of the opamp input	[A]
	$I_{lkg(sys)}$	Input leakage current of the system input	[A]

Example: bidirectional interface for the following data: $V_{(sys)}$ = 5 V ±10%, $V_{(sysH)}$min = 4 V, $V_{(sys+)}$max = 3.5 V, $I_{lkg(sys)}$ = ±1 µA, $I_{lkg(Op)}$ = ±700 pA, I_{lkg} = ±50 nA, V_{ref} = 1.5 V ±5%. The resistor tolerance is p = ±5%. The minimum supply voltage of this example is $DV_{CC(min)}$ = 2.7 V (3.0 V – 10%).

$$\frac{R4}{R5} < (1-2p)\times\left(\frac{V_{(sysH)}min}{V_{ref(max)}}-1\right) = (1-2\times 0.05)\times\left(\frac{4\,V}{1.575\,V}-1\right) = 1.386$$

$$\frac{R4}{R5} > (1+2p)\times\left(\frac{V_{(sysH)}max}{DV_{CC(min)}}-1\right) = (1+2\times 0.05)\times\left(\frac{5.5\,V}{2.7\,V}-1\right) = 1.14$$

The medium value of the two R4/R5 limits is taken: $\frac{R4}{R5} = \frac{1.38+1.14}{2} = 1.26$

$$R4 < \frac{V_{(sysH)}\,min - V_{ref(max)}\times\left(1+\frac{R4}{R5}\times(1+2p)\right)}{\left(I_{lkg}+I_{lkg(Op)}\right)\times(1+p)} = \frac{4.0\,V - 1.575\,V\times(1+1.26\times(1+2\times 0.05))}{(50\,nA+700\,pA)\times(1+0.05)} = 4.55\,M\Omega$$

R4 is chosen to be 2 MΩ. Resistor R5 is calculated as: $R5 = \frac{R4}{1.26} = \frac{2\,M\Omega}{1.26} = 1.59\,M\Omega$

$$R3 < \frac{V_{(sys)}min - V_{(sys+)}\,max}{(1+p)\times\left(I_{lkg(sys)}+\frac{V_{(sys+)}\,max - V_{ref(min)}}{R4\times(1+p)}\right)} = \frac{4.5\,V - 3.5\,V}{(1+0.05)\times\left(1\mu A+\frac{3.5\,V-1.425\,V}{2\,M\Omega\times(1+0.05)}\right)} = 479\,k\Omega$$

The three chosen resistors are: R3 = 330 kΩ, R4 = 2 MΩ, R5 = 1.6 MΩ

5.2 Integrated-Circuit I/O Interface

Dedicated level converters like the SN74LVCC4245A can be used for a bidirectional I/O interface. It is an 8-bit wide level converter, which can convert the I/O levels to 5 V for a complete MSP430 port. Figure 10 shows an application with this IC.

The MSP430 determines the data direction of the interface with the DIR terminal. If needed, bus A can be isolated from bus B with the $\overline{OE}$ terminal.

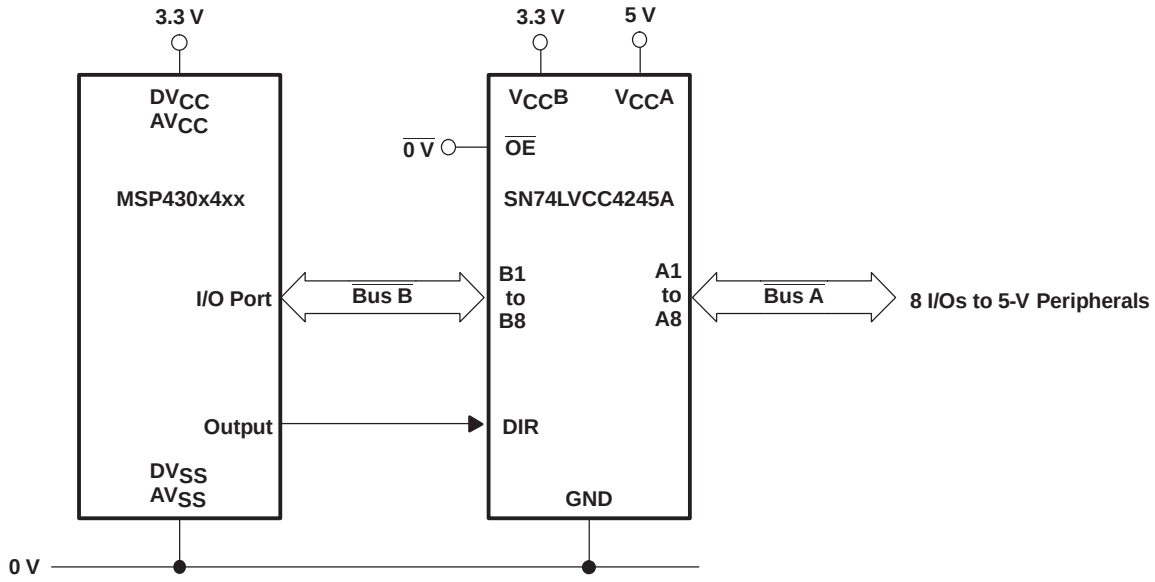

Figure 10. Integrated-Circuit I/O Interface

6 Power Supplies

Note: the design equations for the power supplies below are given in the *Power Supplies for MSP430 Systems* chapter of [1]. This chapter also describes other kinds of power supplies, e.g., transformer driven supplies, with their design equations.

Figure 11 shows a capacitor power supply for two output voltages, V_{CC1} = 3 V and V_{CC2} = 5 V. If the output current of the TLC27L4s is not sufficient, an NPN output buffer can be used as shown in Figure 12.

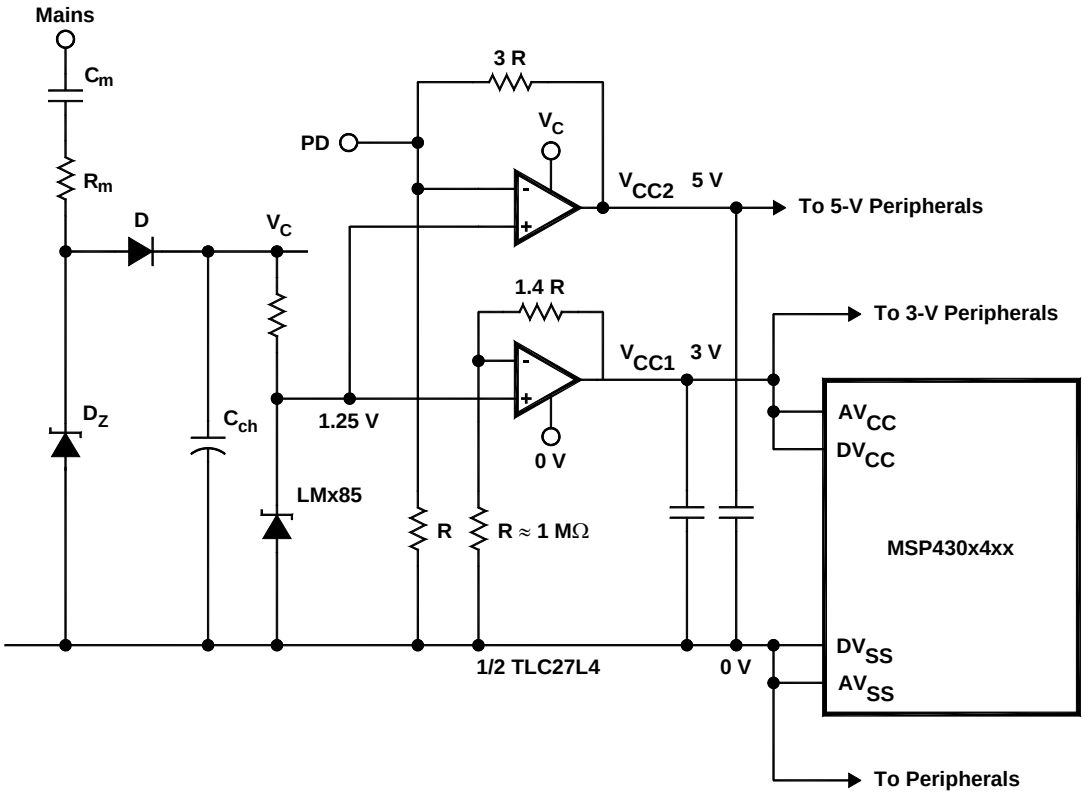

Figure 11. Capacitor Power Supply for Two Output Voltages

Using the power-down output, PD, the MSP430 can switch off the 5-V supply during low power periods (LPM3):

- Active mode: the MSP430 PD output is switched to the high-impedance mode.
- LPM3: the MSP430 output PD is switched to DV_{CC}. The 5-V regulator outputs a voltage near 0 V.

Figure 12 shows a power supply for two output voltages V_{CC1} = 3 V and V_{CC2} = 5 V. The 3-V supply is buffered with an NPN transistor to allow a higher current.

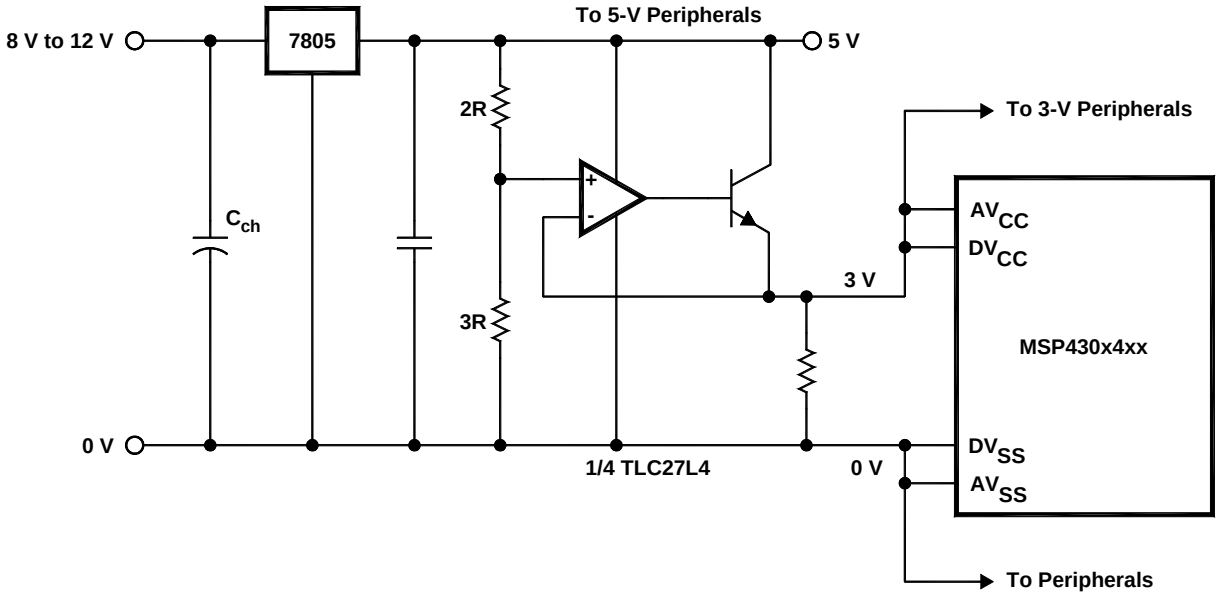

Figure 12. Power Supply for Two Output Voltages

7 Summary

As this application report showed, it is possible to build cost-effective interfaces for the connection of the 3-V MSP430 families to a 5-V environment. In some cases, the external 5-V peripherals already contain the necessary interface. Thanks to Eilhard Haseloff for his very helpful hints.

References

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2. *MSP430x4xx Family User's Guide*, Literature Number SLAU056
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4. *MSP430x43x, MSP430x44x Mixed Signal Microcontroller* data sheet, Literature Number SLAS344
5. *TLC27L4, TLC27L4A, TLC27L4B,TLC27L4Y, TLC27L9 LinCMOS™ Precision Quad Operational Amplifiers* data sheet, Literature Number SLOS053
6. *ULN2001A, ULN2002A, ULN2003A, ULN2004A,ULQ2003A, ULQ2004A High-Voltage High-Current Darlington Transistor Array* data sheet, Literature Number SLRS027
7. *SN74LVCC4245A Octal Dual-Supply Bus Transceiver With Configurable Output Voltage and 3-State Outputs* data sheet, Literature Number SCAS584
8. *Selecting the Right Level-Translation Solutions* application report, Literature Number SCEA035