LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO28; SOT136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF2112T:

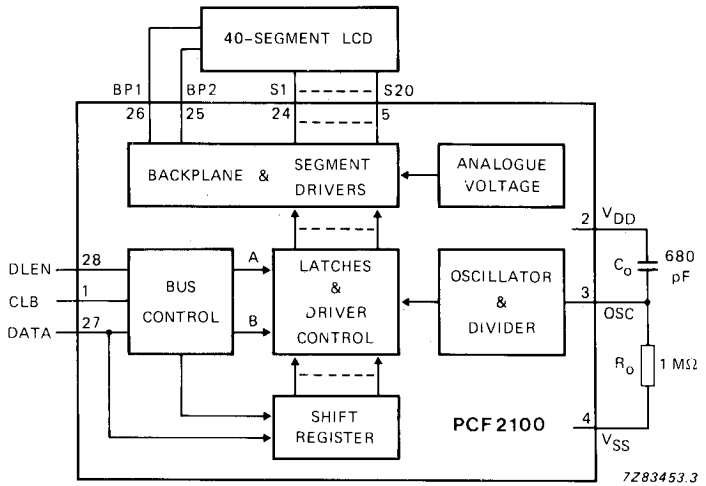


Fig. 1 Block diagram; PCF2100

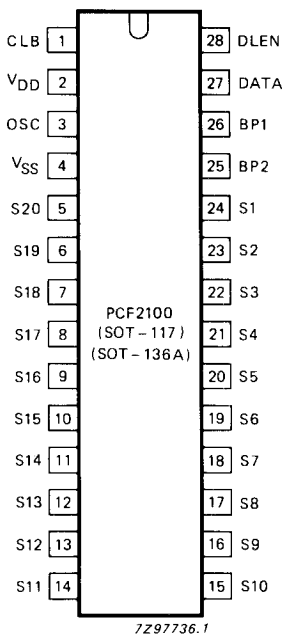


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
27	DATA	data line (CBUS)
28	DLEN	data line enable (CBUS)

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

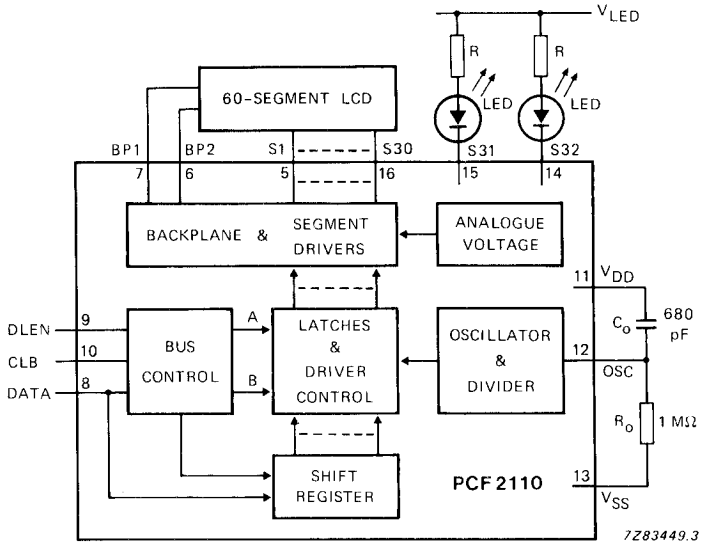


Fig. 3 Block diagram; PCF2110 (SOT-129).

DEVELOPMENT DATA

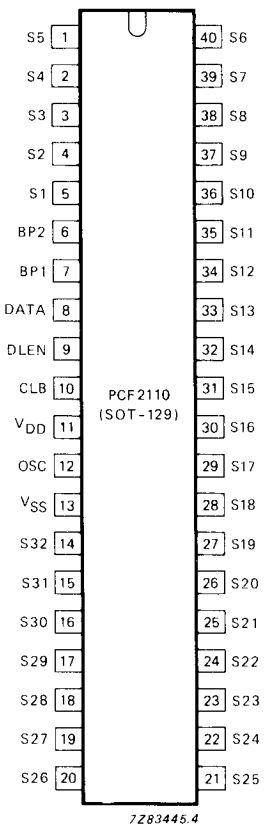


Fig. 4 Pinning diagram; PCF2110

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply
13	V_{SS}	negative supply

Inputs

8	DATA	data line	CBUS
9	DLEN	data line enable	CBUS
10	CLB	clock burst	CBUS
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	backplane drivers (commons of LCD)
7	BP1	backplane drivers (commons of LCD)
14	S32	LED driver outputs
15	S31	LED driver outputs
16 to 40	S30 to S6	LCD driver outputs

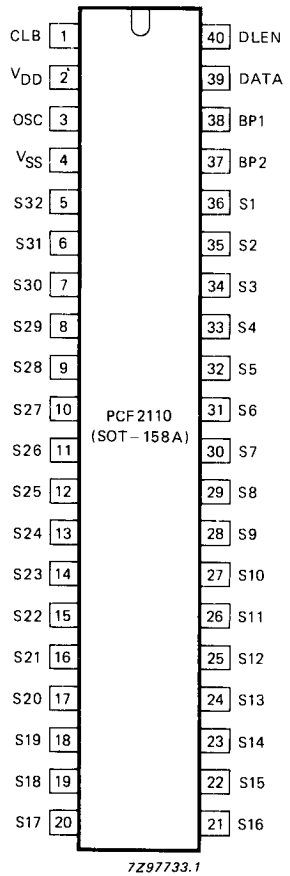


Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line (CBUS)
40	DLEN	data line enable (CBUS)

Outputs

5	S32	LED driver outputs
6	S31	LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	backplane drivers (commons of LCD)
38	BP1	backplane drivers (commons of LCD)

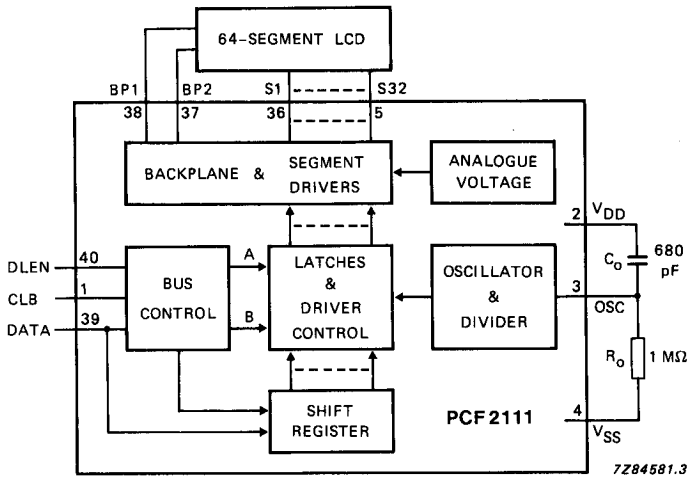


Fig. 6 Block diagram; PCF2111

DEVELOPMENT DATA

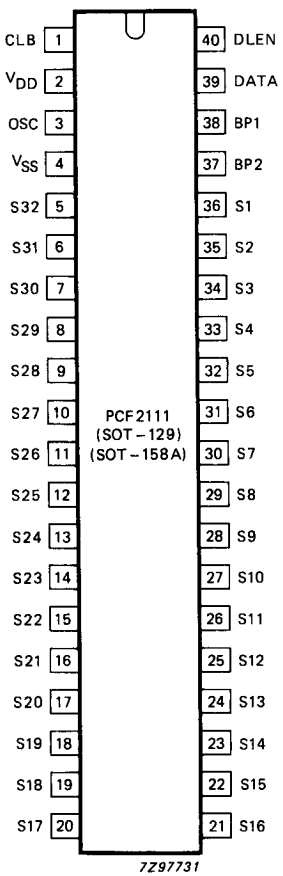


Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	backplane drivers (commons of LCD)
37	BP2	backplane drivers (commons of LCD)

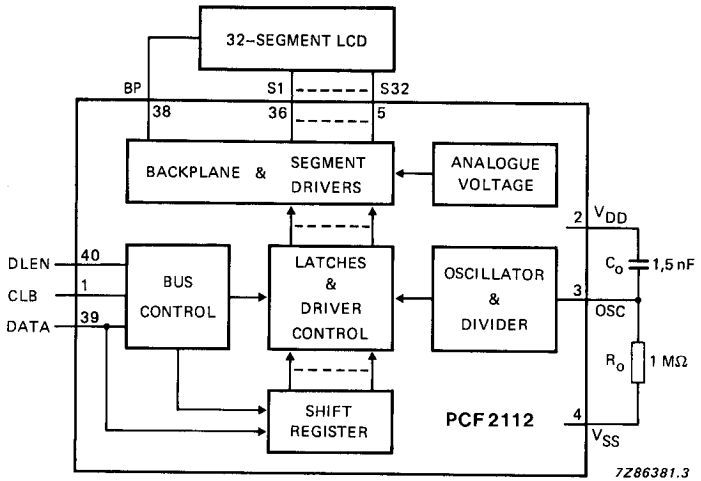


Fig. 8 Block diagram; PCF2112

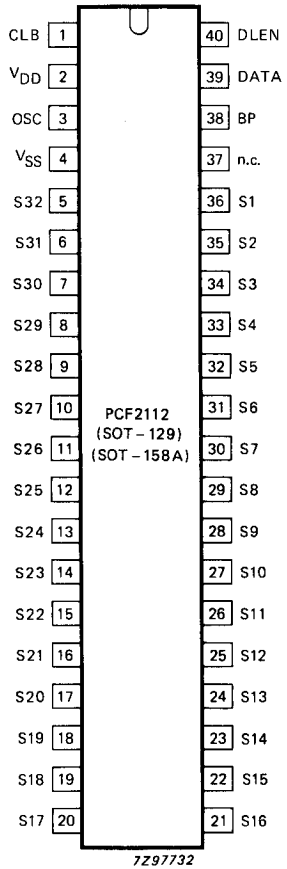


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA-bit is HIGH.

PCF2100

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded. CLB-pulse 23 transfers data from the shift register to the selected latches.

PCF2110

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2111

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2112

When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

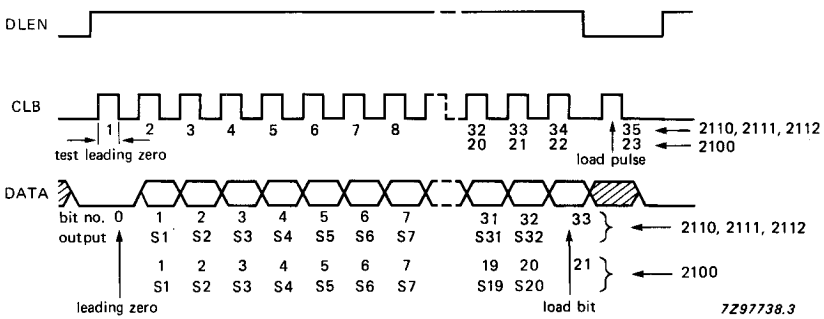


Fig. 10 CBUS data format.

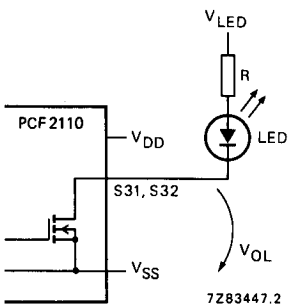


Fig. 11 LED driver circuitry.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

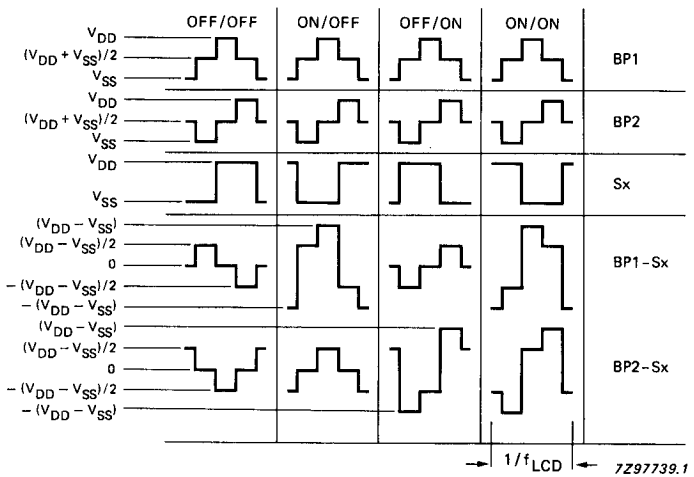


Fig. 12 Timing diagram (except PCF2112).

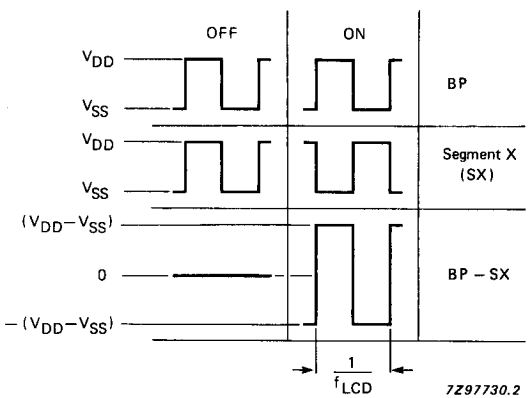


Fig. 13 Timing diagram for PCF2112.

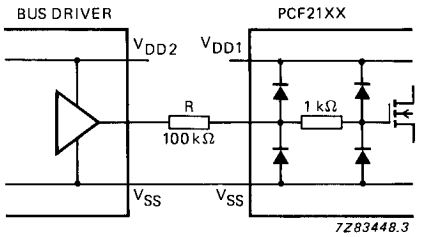
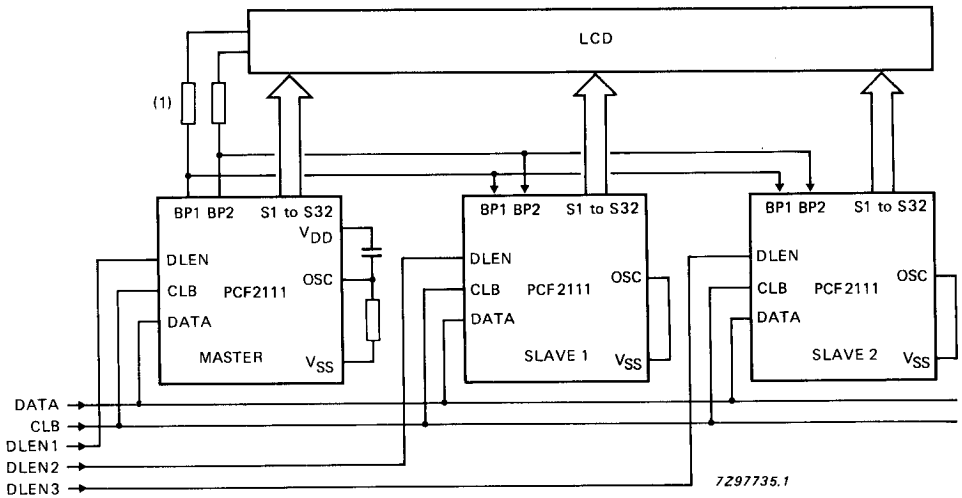


Fig. 14 Input circuitry.

Note to Fig. 14

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leqslant 40\,\mu$A.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be $> 2{,}7$ kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 15 Diagram showing expansion possibility (using PCF2111).

Note to Fig. 15

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XX family up to the BP drive capability of the master. The PCF2112 can only function as a master for other PCF2112s.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	9,0	V
Input voltage range DLEN, CLB, DATA and OSC		V_I	V_{SS}−0,5	V_{DD}+0,5	V
Output voltage range BP1, BP2 and S1 to S32		V_O	V_{SS}−0,5	V_{DD}+0,5	V
Supply current		$\pm I_{DD}$, $\pm I_{SS}$	−	50	mA
DC input current		$\pm I_I$	−	20	mA
DC output current		$\pm I_O$	−	25	mA
Total power dissipation per package	note 1	P_{tot}	−	500	mW
Power dissipation per output		P_O	−	100	mW
Storage temperature range		T_{stg}	−65	+150	°C

Note to the ratings

1. Derate by 7,7 mW/°C when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2,25	–	6,5	V
Supply current	note 1	I_{DD1}	–	20	50	μA
Supply current	note 1; T_{amb} = −25 to + 85 °C	I_{DD2}	–	20	30	μA
Power-on reset level	note 2	V_{POR}	–	1,0	1,4	V
Inputs CLB, DATA DLEN						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,0	–	–	V
Leakage current	$V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	10	pF
Input OSC						
Oscillator start-up current	$V_I = V_{SS}$	I_{OSC}	0,5	1,2	5,0	μA
LCD outputs						
DC component of backplane drivers		$\pm V_{BP}$	–	20	–	mV
Backplane driver output impedance	note 4; V_{DD} = 5 V	R_{BP}	–	0,5	5	kΩ
Segment driver output impedance	note 4; V_{DD} = 5 V	R_S	–	1	7	kΩ
LED outputs (S31 and S32 in PCF2110)						
Output current LOW	V_{OL}=0,4 V; V_{DD}=5 V	I_{OL}	8	14	–	mA
Output leakage current	$V_O = V_{DD}$	$\pm I_O$	–	–	1	μA
Load current		I_{LED}	–	–	20	mA

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs CLB, DATA DLEN						
Data set-up time		t_{SUDA}	3	–	–	μs
Data hold time		t_{HDDA}	3	–	–	μs
Leading zero set-up time		t_{SULZ}	3	–	–	μs
Enable set-up time		t_{SUEN}	1	–	–	μs
Disable set-up time		t_{SUDI}	2	–	–	μs
Load pulse set-up time		t_{SULD}	2,5	–	–	μs
Busy time		t_{BUSY}	3	–	–	μs
CLB HIGH time		t_{WH}	1	–	–	μs
CLB LOW time		t_{WL}	5	–	–	μs
CLB period		t_{CLB}	10	–	–	μs
Rise and fall times		t_r, t_f	–	–	10	μs
LCD timing						
LCD frame frequency		f_{LCD}	60	75	100	Hz
LCD frame frequency for PCF2112	C_O = 1,5 nF	f_{LCD}	30	35	50	Hz
Transfer time with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
Driver delay with test loads	V_{DD} = 5 V	t_{PLCD}	–	20	100	μs

Notes to the characteristics

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

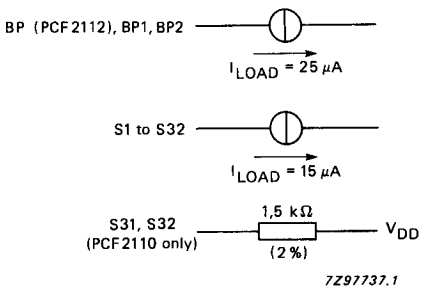


Fig. 16 Test loads.

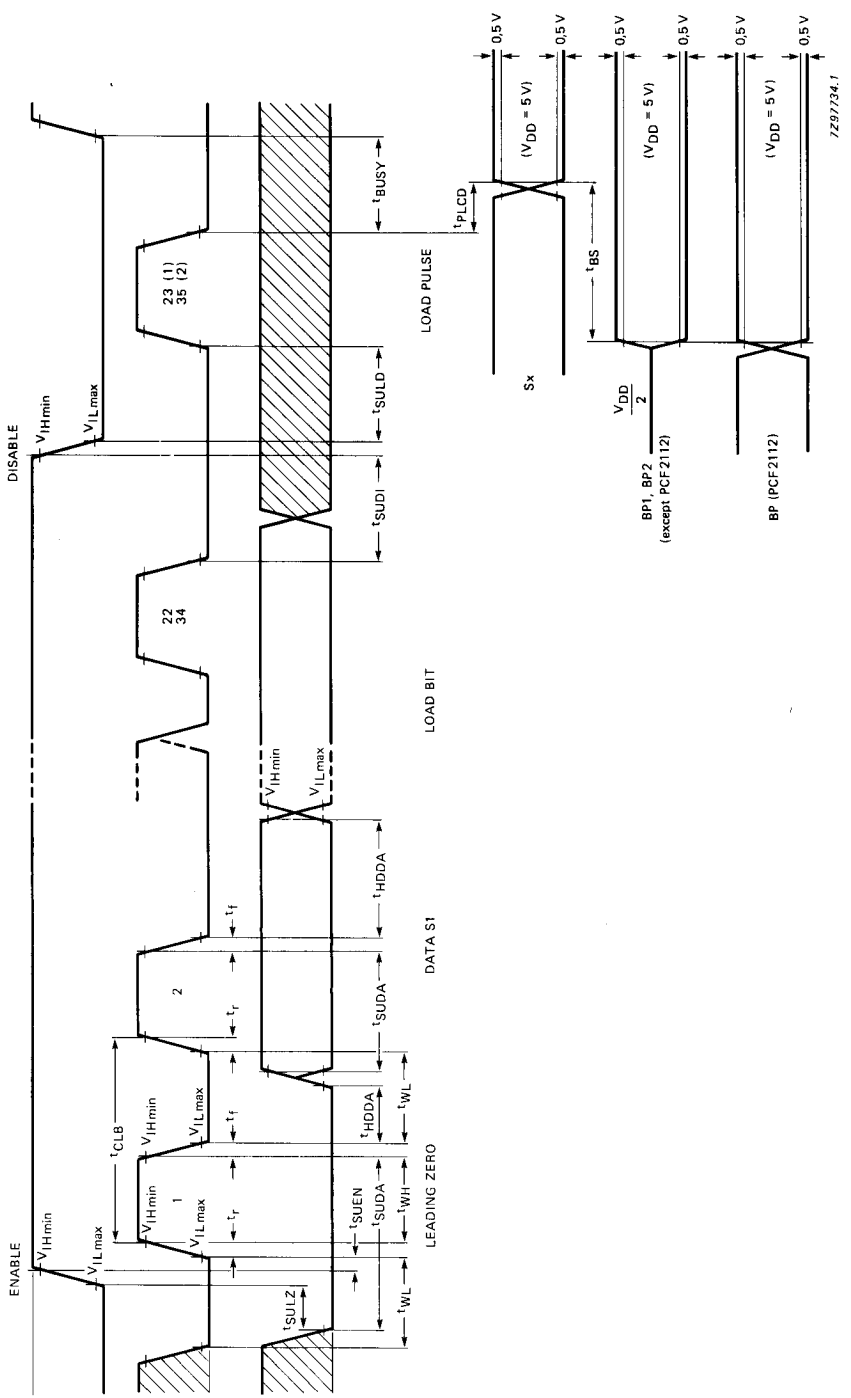


Fig. 17 CBUS timing.

(1) Load pulse 23 (for PCF2100).
(2) Load pulse 35 (for PCF2110, PCD2111 and PCF2112; see Fig. 10).

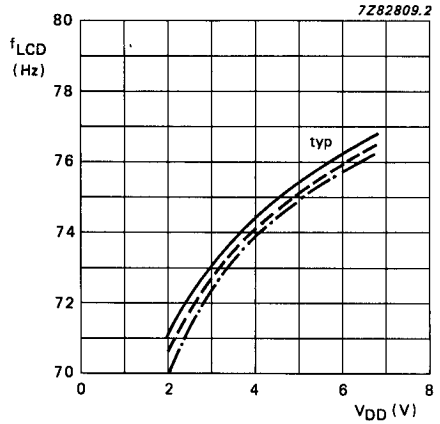


Fig. 18 Displays frequency as a function of supply voltage; C_O = 680 pF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

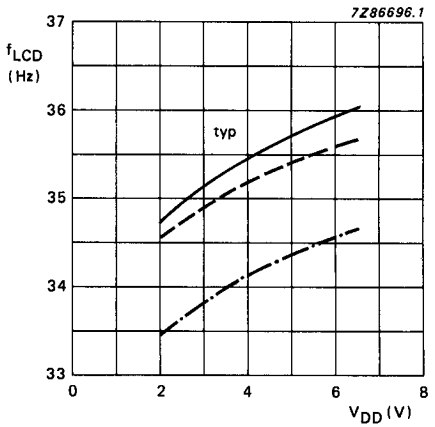


Fig. 19 Display frequency as a function of supply voltage; C_O = 1,5 nF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

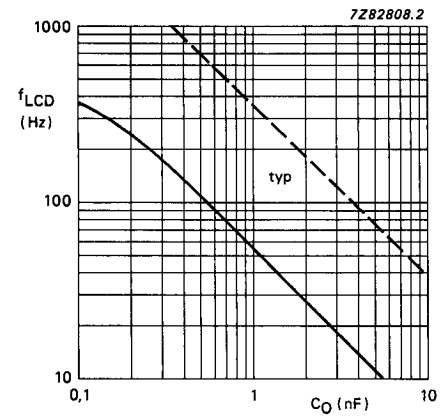


Fig. 20 Display frequency as a function of R_O and C_O; T_{amb} = + 25 °C; V_{DD} = 5 V.
——— R_O = 1 MΩ;
– – – – R_O = 100 kΩ.

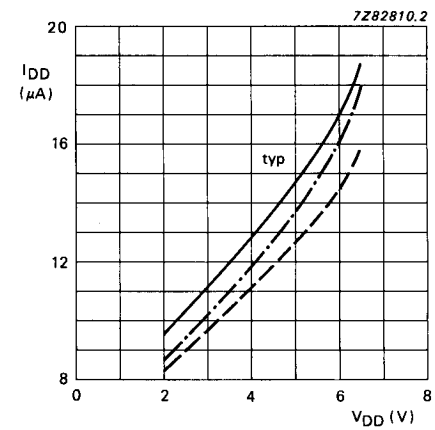


Fig. 21 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

DEVELOPMENT DATA

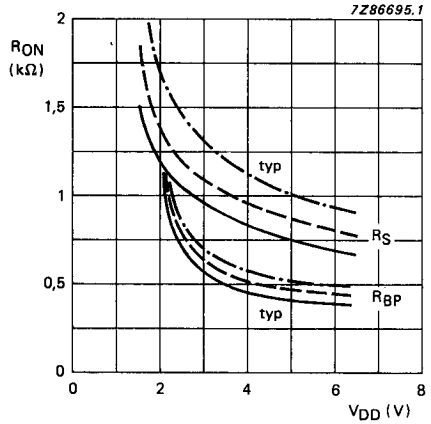


Fig. 22 Output resistance of backplane and segments.
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

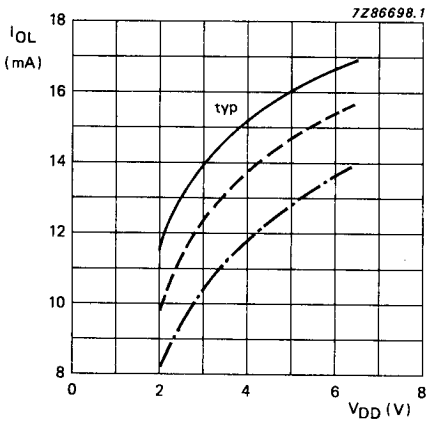


Fig. 23 Output current as a function of supply voltage (only PCF2112).
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.