

M16C/65 Group

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Three-phase Motor Control Timer Function (Sawtooth Wave Modulation)

1. Abstract

The M16C/65 Groups allow users to select the operation mode of the three-phase motor control timer function, depending on the user system.

This application note describes microcomputer (MCU) operation when the marked functions in Table 1 are selected.

Table 1. Settings

Item	Settings	
Modulation mode	0	Sawtooth wave modulation mode
		Triangular wave modulation mode
Timer A11, A21, and A41 control	0	Timers A11, A21, and A41 not used (three-phase mode 0)
(three-phase mode)		Timers A11, A21, and A41 used (three-phase mode 1)
Output polarity	0	Low active of an output waveform
		High active of an output waveform

When the INV06 bit is set to 1 (sawtooth wave modulation mode), set the INV11 bit to 0 (three-phase mode 0).

2. Introduction

This application note applies to the M16C/65 Group MCU.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Detailed Description

3.1 Sawtooth Wave Modulation Mode

- A) Set each register in the three-phase motor control timer function to sawtooth wave modulation mode, timers A11, A21 and A41 not used (three-phase mode 0).
- B) Set bits TAiS and TB2S in the TABSR register to 1 (count started) to decrement the timer B2 counter value (i = 4, 1, 2).
- C) A one-shot pulse is output from timer Ai when the timer B2 counter underflows.
- D) Registers IDB0 and IDB1 determine each phase output signal level at the falling edge of the timer Ai one-shot pulse.

Figure 1 shows an example diagram of the sawtooth wave modulation.

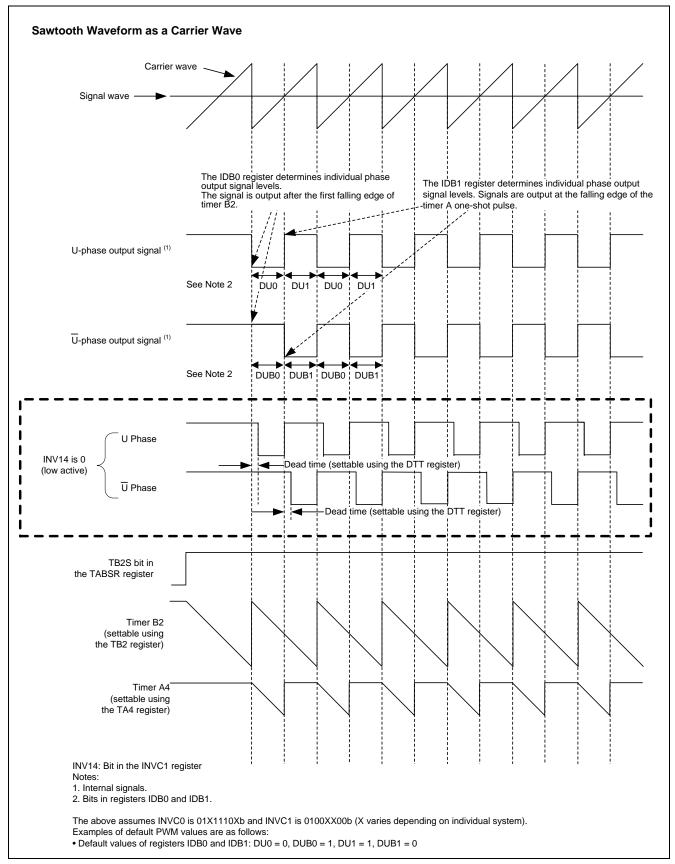


Figure 1. Sawtooth Wave Modulation Operation

3.2 Dead Time

The signal to switch between low active and high active has dead time. Set the INV14 bit in the INVC1 register to select low active or high active.

Figure 2 shows the dead time when low active logic is selected.

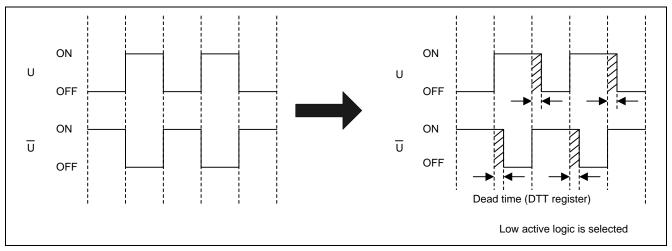


Figure 2. Dead Time

3.3 Three-phase Output Buffer Registers (Registers IDB0 and IDB1)

Figure 3 shows an example of U-phase output signal operation with registers IDB0 and IDB1 and each phase output signal.

When sawtooth wave modulation is selected, the individual phase output port reflects the IDB0 register setting as soon as the timer starts.

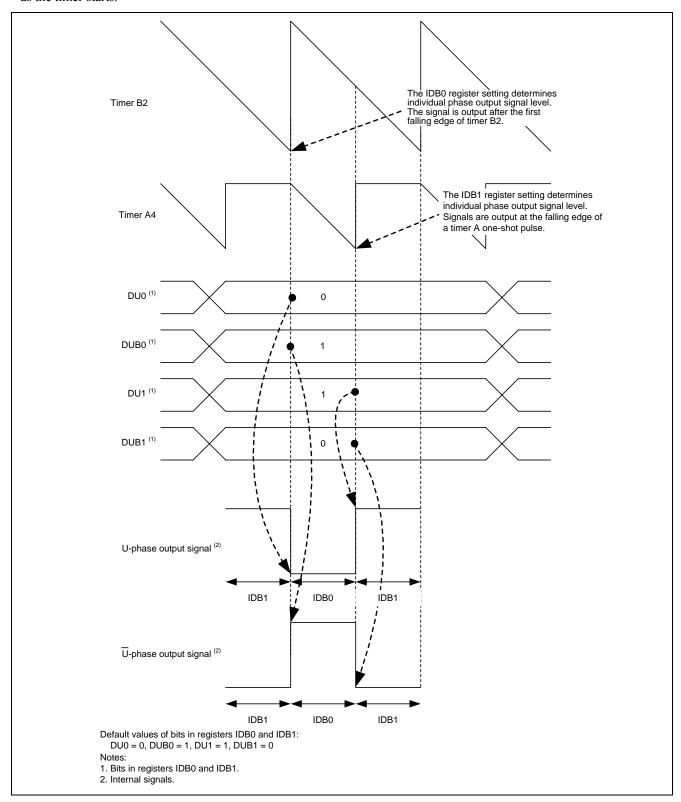


Figure 3. U-phase Output Signal Operation Example

4. Setting Procedure

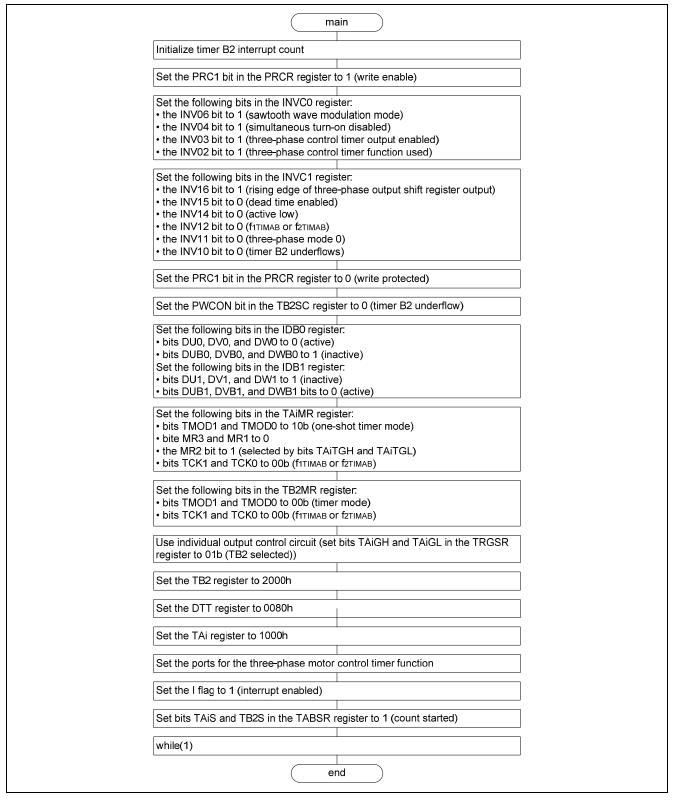


Figure 4. Sawtooth Wave Modulation Mode Flowchart

5. Sample Program

Note the following information when setting registers TAi and TAi1 (i = 4, 1, 2).

5.1 TAi Register Setting

Users must avoid setting the TAi register as follow except if necessary.

A) If the TAi register is set to 0000h (0000h or 0100h when the INV12 bit in the INVC register to 1 (f1TIMAB divided-by-2), the TAi timer counter will not start.

B) If the TAi register is set to a value larger than the TB2 register setting value (a value larger than "TB2 register setting value - 1" when the INV12 bit in the INVC register is 1 (f1TIMAB divided-by-2)), the TAi timer counter continues running the number of cycles determined by the TB2 register.

At the end of both events, the output signal level does not change since no falling edges occur.

5.2 Dead Time Timer Restart

Even if the TAi register setting causes the dead time timer to restart while the dead time timer is counting, the dead time timer does not restart counting.

If the following conditions are met, the dead time timer will not restart counting:

• Triangular wave modulation mode (three-phase mode 0): f1TIMAB selected as count source for the dead time timer

((TB2 register setting value + 1) - TAi1 register setting value at an even number of times) + TA1 register setting value at an odd number of times < setting value of dead time timer

TAi1 register setting value at an even number of times + ((TB2 register setting value+1) – TAi register setting value at an odd number of times) < setting value of dead time timer

• Triangular wave modulation mode (three-phase mode 1): f1TIMAB selected as count source for the dead time timer

((TB2 register setting value + 1) – TAi1 register setting value) + TAi register setting value < setting value < setting value of dead time timer

TAi1 register setting value + ((TB2 register setting value + 1) – TAi register setting value) < setting value of dead time timer

Sawtooth wave modulation mode: flTIMAB selected as count source for the dead time timer

((TB2 register setting value+1) – TAi register setting value) – 1 < setting value of dead time timer

TAi register setting value $-1 \le$ setting value of dead time timer

6. Reference Documents

M16C/65 Group User's Manual: Hardware (Hardware Manual) Rev.1.10

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

M16C Series/R8C Family C Compiler Package V.5.45 C Compiler User Manual Rev.2.00

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	M16C/65 Group
Revision History	Three-phase Motor Control Timer Functions
	(Sawtooth Wave Modulation)

Rev.	Date	Description		
	Date	Page	Summary	
1.00	2010.08.20	_	First edition issued	

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

- The state of the product is undefined at the moment when power is supplied.
- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
 - In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

- After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

- Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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